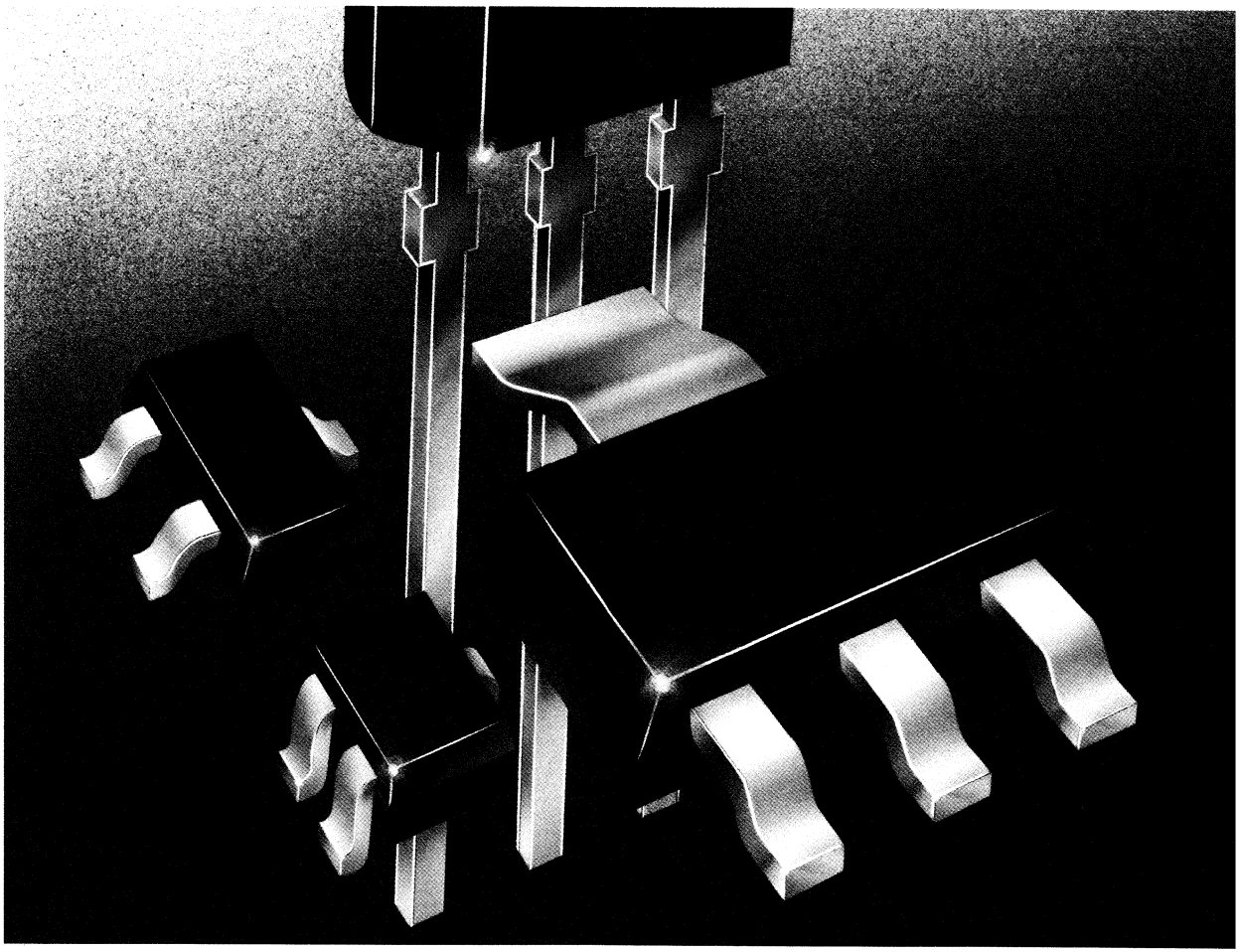
Small-signal Field-effect Transistors



1995

DATA HANDBOOK SC07

Philips
Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Small-signal Field-effect Transistors

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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ALPHANUMERIC INDEX

Types added to the range since the last issue of Handbook SC07 (1994 issue) are shown in bold print.

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SELECTION GUIDE

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS

TYPE NUMBER	PACKAGE	$\pm V_{DS}$ (V)	CHARACTERISTICS					PAGE
			I_G (mA)	I_{DSS} min - max (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. (mS)	C_{rs} (pF)	
Hi-fi amplifiers and AF equipment								
BC264A	TO-92 variant	30	10	2 to 4.5	>0.5	2.5	1.2	71
BC264B	TO-92 variant	30	10	3.5 to 6.5	>0.5	3	1.2	71
BC264C	TO-92 variant	30	10	5 to 8	>0.5	3.5	1.2	71
BC264D	TO-92 variant	30	10	7 to 12	>0.5	4	1.2	71
DC, LF and HF amplifiers								
BF245A	TO-92 variant	30	10	2 to 6.5	<8	3 to 6.5	1.1	77
BF245B	TO-92 variant	30	10	6 to 15	<8	3 to 6.5	1.1	77
BF245C	TO-92 variant.	30	10	12 to 25	<8	3 to 6.5	1.1	77
BF545A	SOT23	30	10	2 to 6.5	0.4 to 7.5	3 to 6.5	0.8	112
BF545B	SOT23	30	10	6 to 15	0.4 to 7.5	3 to 6.5	0.8	112
BF545C	SOT23	30	10	12 to 25	0.4 to 7.5	3 to 6.5	0.8	112
BF556A	SOT23	30	10	3 to 7	0.5 to 7.5	4.5	0.8	123
BF556B	SOT23	30	10	6 to 13	0.5 to 7.5	4.5	0.8	123
BF556C	SOT23	30	10	11 to 18	0.5 to 7.5	4.5	0.8	123
Preamplifiers for AM tuners in car radios								
BF851A	TO-92	25	10	2 to 6.5	0.2 to 2.0	12	2.5	131
BF851B	TO-92	25	10	6 to 15	0.2 to 2.0	16	2.5	131
BF851C	TO-92	25	10	12 to 25	0.2 to 2.0	20	2.5	131
BF861A	SOT23	25	10	2 to 6.5	0.2 to 2.0	12	2.5	139
BF861B	SOT23	25	10	6 to 15	0.2 to 2.0	16	2.5	139
BF861C	SOT23	25	10	12 to 25	0.2 to 2.0	20	2.5	139
VHF and UHF amplifiers and general purpose switching								
BF246A	TO-92 variant	25	10	30 to 80	0.6 to 14.5	8	3.5	89
BF246B	TO-92 variant	25	10	60 to 140	0.6 to 14.5	8	3.5	89
BF246C	TO-92 variant7.	25	10	110 to 250	0.6 to 14.5	8	3.5	89
BF247A	TO-92 variant	25	10	30 to 80	0.6 to 14.5	8	3.5	89
BF247B	TO-92 variant	25	10	60 to 140	0.6 to 14.5	8	3.5	89
BF247C	TO-92 variant.	25	10	110 to 250	0.6 to 14.5	8	3.5	89
VHF and UHF applications								
BF256A	TO-92 variant	30	10	3 to 7	<7.5	4.5	0.7	91
BF256B	TO-92 variant	30	10	6 to 13	<7.5	4.5	0.7	91
BF256C	TO-92 variant.	30	10	11 to 18	<7.5	4.5	0.7	91

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS (continued)

TYPE NUMBER	PACKAGE	$\pm V_{DS}$ (V)	CHARACTERISTICS					PAGE
			I_G (mA)	I_{DSS} min - max (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. (mS)	C_{rs} (pF)	
RF stages FM portables, car radios, mains radios and mixer stages								
BF410A	TO-92 variant	20(1)	10	0.7 to 3	typ. 0.8	2.5	0.5	103
BF410B	TO-92 variant	20(1)	10	2.5 to 7	typ. 1.5	4	0.5	103
BF410C	TO-92 variant.	20(1)	10	6 to 12	typ. 2.2	6	0.5	103
BF410D	TO-92 variant.	20(1)	10	10 to 18	typ. 3	7	0.5	103
BF510	SOT23	20(1)	10	0.7 to 3	typ. 0.8	2.5	0.3	107
BF511	SOT23	20(1)	10	2.5 to 7	typ. 1.5	4	0.3	107
BF512	SOT23	20(1)	10	6 to 12	typ. 2.2	6	0.3	107
BF513	SOT23	20(1)	10	10 to 18	typ. 3	7	0.3	107
Low level general purpose amplifiers								
BFR30	SOT23	25	5	4 to 10	<5	1 to 4	0.85	285
BFR31	SOT23	25	5	1 to 5	<2.5	1.5 to 4.5	0.85	285
General purpose amplifiers								
BFT46	SOT23	25	5	0.2 to 1.5	<1.2	1	0.85	295
AM input stages UHF/VHF amplifiers								
BFU308	TO-18	25	50	12 to 60	1 to 6.5	10	1.3	302
BFU309	TO-18	25	50	12 to 30	1 to 4	10	1.3	302
BFU310	TO-18	25	50	24 to 60	2 to 6.5	10	1.3	302
J308	TO-92	25	50	12 to 60	1 to 6.5	10	1.3	674
J309	TO-92	25	50	12 to 30	1 to 4	10	1.3	674
J310	TO-92	25	50	24 to 60	2 to 6.5	10	1.3	674
PMBF4416	SOT23	30	10	5 to 15	<6	4.5 to 7.5	<0.8	733
PMBF4416A	SOT23	35	10	5 to 15	2.5 to 6	4.5 to 7.5	<0.8	733
PMBF5484	SOT23	25	10	1 to 5	0.3 to 3	3	<1	739
PMBF5485	SOT23	25	10	4 to 10	0.5 to 4	3.5	<1	739
PMBF5486	SOT23	25	10	8 to 20	2 to 6	4	<1	739
PMBFJ308	SOT23	25	50	12 to 60	1 to 6.5	10	1.3	758
PMBFJ309	SOT23	25	50	12 to 30	1 to 4	10	1.3	758
PMBFJ310	SOT23	25	50	24 to 60	2 to 6.5	10	1.3	758
PN4416	SOT54	30	10	5 to 15	<6	4.5 to 7.5	<0.8	773
PN4416A	SOT54	35	10	5 to 15	2.5 to 6	4.5 to 7.5	<0.8	773
2N4416	TO-72	30	10	5 to 15	<6	4.5 to 7.5	<0.8	809
2N4416A	TO-72	35	10	5 to 15	2.5 to 6	4.5 to 7.5	<0.8	809
2N5484	SOT54	25	10	1 to 5	0.3 to 3	3	<1	825
2N5485	SOT54	25	10	4 to 10	0.5 to 4	3.5	<1	825

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS (continued)

TYPE NUMBER	PACKAGE	$\pm V_{DS}$ (V)	CHARACTERISTICS					PAGE
			I_G (mA)	I_{DSS} min - max (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. (mS)	C_{rs} (pF)	
2N5486	SOT54	25	10	8 to 20	2 to 6	4	<1	825
Broadband amplifier up to 300 MHz and differential amplifier								
BFW10	TO-72	30	10	8 to 20	<8	3.5 to 6.5	0.6	313
BFW11	TO-72	30	10	4 to 10	<6	3 to 6.5	0.6	313
Low current, low voltage applications								
BFW12	TO-72	30	5	1 to 5	<2.5	2	0.8	325
BFW13	TO-72	30	5	0.2 to 1.5	<1.2	1	0.8	325

Note

1. Asymmetrical.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS FOR SWITCHING

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		R_{DSon} max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
BSR56	SOT23	40	50	50	–	4	10	25	–	9	25	537
BSR57	SOT23	40	50	20	100	2	6	40	5	10	50	537
BSR58	SOT23	40	50	8	80	0.8	4	60	–	20	100	537
BSV78	TO-18	40	50	50	–	3.75	11	25	–	10	10	651
BSV79	TO-18	40	50	20	–	2	7	40	5	18	16	651
BSV80	TO-18	40	50	10	–	1	5	60	–	30	32	651
J108	TO-92	25	50	80	–	3	10	8	15	typ. 4	typ. 6	664
J109	TO-92	25	50	40	–	2	6	12	15	typ. 4	typ. 6	664
J110	TO-92	25	50	10	–	0.5	4	18	15	typ. 4	typ. 6	664
J111	TO-92	40	50	20	–	3	10	30	typ. 3	typ. 13	typ. 35	668
J112	TO-92	40	50	5	–	1	5	50	typ. 3	typ. 13	typ. 35	668
J113	TO-92	40	50	2	–	0.5	3	100	typ. 3	typ. 13	typ. 35	668
PMBF4391	SOT23	40	50	50	150	4	10	30	–	15	20	729
PMBF4392	SOT23	40	50	25	75	2	5	60	3.5	15	35	729
PMBF4393	SOT23	40	50	5	30	0.5	3	100	–	15	50	729
PMBFJ108	SOT23	25	50	80	–	3	10	8	15	typ. 4	typ. 6	746
PMBFJ109	SOT23	25	50	40	–	2	6	12	15	typ. 4	typ. 6	746
PMBFJ110	SOT23	25	50	10	–	0.5	4	18	15	typ. 4	typ. 6	746
PMBFJ111	SOT23	40	50	20	–	3	10	30	typ. 3	typ. 13	typ. 35	750
PMBFJ112	SOT23	40	50	5	–	1	5	50	typ. 3	typ. 13	typ. 35	750

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS FOR SWITCHING (continued)

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		R_{DSon} max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
PMBFJ113	SOT23	40	50	2	–	0.5	3	100	typ. 3	typ. 13	typ. 35	750
PN4391	TO-92 var.	40	50	50	150	4	10	30	5	15	20	769
PN4392	TO-92 var.	40	50	25	100	2	5	60	5	15	35	769
PN4393	TO-92 var.	40	50	5	60	0.5	3	100	5	15	50	769
PZFJ108	SOT223	25	50	80	–	3	10	8	15	typ. 4	typ. 6	779
PZFJ109	SOT223	25	50	40	–	2	6	12	15	typ. 4	typ. 6	779
PZFJ110	SOT223	25	50	10	–	0.5	4	18	15	typ. 4	typ. 6	779
2N4091	TO-18	40	10	30	–	5	10	30	5	25	40	795
2N4092	TO-18	40	10	15	–	2	7	50	5	35	60	795
2N4093	TO-18	40	10	8	–	1	5	80	5	60	80	795
2N4391	TO-18	50	50	50	150	4	10	30	3.5	15	20	805
2N4392	TO-18	50	50	25	75	2	5	60	3.5	15	35	805
2N4393	TO-18	50	50	5	30	0.5	3	100	3.5	15	50	805
2N4856	TO-18	40	50	50	–	4	10	25	8	9	25	815
2N4857	TO-18	40	50	20	100	2	6	40	8	10	50	815
2N4858	TO-18	40	50	8	80	0.8	4	60	8	20	100	815
2N4859	TO-18	30	50	50	–	4	10	25	8	9	25	815
2N4860	TO-18	30	50	20	100	2	6	40	8	10	50	815
2N4861	TO-18	30	50	8	80	0.8	4	60	8	20	100	815

P-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS FOR SWITCHING

TYPE NUMBER	PACKAGE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		R_{DSon} max. (Ω)	C_{rs} typ. (pF)	t_{on} typ. (ns)	t_{off} typ. (ns)	
				min.	max.	min.	max.					
J174	TO-92	30	50	20	135	5	10	85	4	7	15	671
J175	TO-92	30	50	7	70	3	6	125	4	15	30	671
J176	TO-92	30	50	2	35	1	4	250	4	35	35	671
J177	TO-92	30	50	1.5	20	0.8	2.25	300	4	45	40	671
PMBFJ174	SOT23	30	50	20	135	5	10	85	4	7	15	755
PMBFJ175	SOT23	30	50	7	70	3	6	125	4	15	30	755
PMBFJ176	SOT23	30	50	2	35	1	4	250	4	35	35	755
PMBFJ177	SOT23	30	50	1.5	20	0.8	2.25	300	4	45	40	755

N-CHANNEL, SINGLE GATE MOS-FETS FOR SWITCHING

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V) note 1		MODE	R_{DSon} max. (Ω)	C_{rss} typ. (pF)	t_{on}/t_{off} max. (ns)	
				min.	max.	min.	max.					
BFR29	TO-72	30 (2)	20	10	40	0.5	3.5	depl.	–	0.4	–	277
BSD12	TO-72	20	50	–	–	–	2	depl.	30	0.6	1/5	359
BSD22	SOT143	20	50	–	–	–	2	depl.	30	0.6	1/5	363
BSD212	TO-72	10	50	–	–	0.1	2	enh.	70	0.6	1/5	367
BSD213	TO-72	10	50	–	–	0.1	2	enh.	70	0.6	1/5	367
BSD214	TO-72	20	50	–	–	0.1	2	enh.	70	0.6	1/5	367
BSD215	TO-72	20	50	–	–	0.1	2	enh.	70	0.6	1/5	367
BSS83	SOT143	10	50	–	–	0.1	2	enh.	45	0.6	1/5	541
BSV81	TO-72	30(2)	25	–	–	–	–	depl.	100	0.5	–	659

Notes

1. Enhancement types $V_{GS(th)}$.
2. V_{DB}/V_{SB}.

N-CHANNEL, DUAL GATE MOS-FETS

All types protected against excessive input voltage surges.

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS						REMARKS	PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} min.. max. (mA)	$-V_{(P)GS}$ (V) note 1	$\|y_{fs}\|$ min. (mS)	C_{is} typ. (pF)	C_{os} typ. (pF)	F typ. (dB)		
BF901	SOT143	12	30	–	0.7	25	2.35	1.2	1.7	VHF & UHF	147
BF901R	SOT143R	12	30	–	0.7	25	2.35	1.2	1.7	VHF & UHF	147
BF904	SOT143	7	30	–	1.8	22	2.2	1.3	2	VHF & UHF	150
BF904R	SOT143R	7	30	–	1.8	22	2.2	1.3	2	VHF & UHF	150
BF904WR	SOT343R	7	30	–	1.8	22	2.2	1.3	2	VHF & UHF	159
BF908	SOT143	12	40	3 to 27	2	36	3.1	1.7	1.5	VHF & UHF	168
BF908R	SOT143R	12	40	3 to 27	2	36	3.1	1.7	1.5	VHF & UHF	168
BF908WR	SOT343R	12	40	3 to 27	2	36	3.1	1.7	1.5	VHF & UHF	174
BF909	SOT143	7	40	–	1	36	3.6	2.3	2	VHF & UHF	178
BF909R	SOT143R	7	40	–	1	36	3.6	2.3	2	VHF & UHF	178
BF909WR	SOT343R	7	40	–	1	36	3.6	2.3	2	VHF & UHF	186
BF989	SOT143	20	20	2 - 20	2.7	9.5	1.8	0.9	2.8	UHF	195
BF990A	SOT143	18	30	–	1.3	18	2.6	1.2	2.8	UHF	199
BF990AR	SOT143R	18	30	–	1.3	18	–	1.2	2	UHF	203
BF991	SOT143	20	20	4 - 25	2.5	10	2.1	1.1	0.7	VHF	205
BF992	SOT143	20	40	–	1.3	20	4	2	1.2	VHF	209
BF992R	SOT143R	20	40	–	1.3	20	–	2	1.2	VHF	215
BF994S	SOT143	20	30	4 to 20	2.5	15	2.5	1	1	VHF	217
BF996S	SOT143	20	30	4 to 20	2.5	15	2.3	0.8	1.8	UHF	221
BF997	SOT143	20	30	4 to 20	2.5	15	2.5	1	1	VHF	225
BF998	SOT143	12	30	2 to 18	2.5	21	2.1	1.05	1	VHF & UHF	228
BF998R	SOT143R	12	30	2 to 18	2.5	21	2.1	1.05	1	VHF & UHF	237
BF998WR	SOT343R	12	30	2 to 18	2.5	22	2.1	1.05	1	VHF & UHF	246
BF1100	SOT143	14	30	–	1	24	2.2	1.4	2	VHF & UHF	254
BF1100R	SOT143R	14	30	–	1	24	2.2	1.4	2	VHF & UHF	254
BF1100WR	SOT343R	14	30	–	1	24	2.2	1.4	2	VHF & UHF	265

Note

1. Enhancement types $V_{GS(th)}$.

N-CHANNEL VERTICAL D-MOS-FETS FOR SWITCHING

Total power dissipation (P_{tot}) measured at T_{amb} = 25 °C, unless otherwise specified.

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS107	TO-92 var.	200	120	500	typ. 1.8	15	28	20	2.6	10/10	334
BS107A	TO-92 var.	200	250	600	1 to 3	4.5	6.4	250	10	5/15	341
BS108	TO-92 var.	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	344
BS170	TO-92 var.	60	500	830	0.8 to 3	2.5	5	200	10	10/10	347
BSD254	TO-92 var.	250	200	850	0.6 to 1.4	–	12	250	5	10/30	371
BSD254A	TO-92 var.	250	200	850	0.6 to 1.4	–	12	250	5	10/30	371
BSD254AR	TO-92 var.	250	200	850	0.6 to 1.4	–	12	250	5	10/30	371
BSN10	TO-92 var.	50	175	830	0.4 to 1.8	14	20	100	5	5/10	377
BSN10A	TO-92 var.	50	175	830	0.4 to 1.8	14	20	100	5	5/10	377
BSN20	SOT23	50	100	250	0.4 to 1.8	14	20	100	5	5/10	381
BSN204	TO-92	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	385
BSN204A	TO-92	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	385
BSN205	TO-92 var.	200	300	1000	0.8 to 2.8	4.5	6	400	10	10/20	389
BSN205A	TO-92 var.	200	300	1000	0.8 to 2.8	4.5	6	400	10	10/20	389
BSN254	TO-92 var.	250	300	1000	0.8 to 2.2	4.5	10	20	2.4	10/30	393
BSN254A	TO-92 var.	250	300	1000	0.8 to 2.2	4.5	10	20	2.4	10/30	393
BSN274	TO-92 var.	270	250	1000	0.8 to 2	6.5	14	20	2.4	10/30	397
BSN274A	TO-92 var.	270	250	1000	0.8 to 2	6.5	14	20	2.4	10/30	397
BSN304	TO-92 var.	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	402
BSN304A	TO-92 var.	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	402
BSP89	SOT223	240	350	1500	0.8 to 2	4	6	340	10	10/30	408
BSP100	SOT223	30	3500	1650	1 to 2.8	0.08	0.1	2200	10	40/75	414
BSP106	SOT223	60	425	1500	0.8 to 3	2.5	4	200	10	5/15	420
BSP107	SOT223	200	200	1500	0.8 to 2.4	20	28	20	2.6	10/20	426
BSP108	SOT223	80	500	1500	1.5 to 3.5	2	3	500	10	8/15	433
BSP110	SOT223	80	325	1500	0.8 to 2.8	7	10	150	5	5/10	437
BSP120	SOT223	200	250	1500	0.8 to 2.8	7	12	250	10	6/20	441
BSP121	SOT223	200	350	1500	0.8 to 2.8	4.5	6	400	10	10/20	445
BSP122	SOT223	200	550	1500	0.4 to 2	1.6	2.5	750	10	35/50	450
BSP124	SOT223	250	250	1500	0.6 to 1.4	–	12	250	5	10/30	452
BSP126	SOT223	250	350	1500	0.8 to 2	5	10	20	2.4	10/30	459
BSP127	SOT223	270	350	1500	0.8 to 2	6.5	8	250	10	10/30	464
BSP128	SOT223	200	350	1500	0.4 to 1.8	5	8	100	2.8	10/30	466
BSP130	SOT223	300	300	1500	0.8 to 2	6.7	8	250	10	10/30	468
BSP145	SOT223	450	250	1500	2 to 4	10	14	100	10	10/100	474

N-CHANNEL VERTICAL D-MOS-FETS FOR SWITCHING (continued)

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BSP152	SOT223	200	550	1500	1.5 to 3.5	–	2.5	750	10	15/30	480
BSS87	SOT89	200	280	1000	0.8 to 2.8	4.5	6	400	10	10/25	551
BSS88	TO-92 var.	230	250	1000	0.4 to 1.2	5	8	150	5	10/30	554
BSS89	TO-92 var.	200	300	1000	0.8 to 2.8	4.5	6	400	10	–	557
BSS91	TO-18	200	350	1500(1)	0.8 to 2.8	4.5	6	400	10	15/25	561
BSS100	TO-92 var.	100	250	830	0.8 to 2.8	3	6	120	10	10/20	568
BSS123	SOT23	100	150	250	0.8 to 2.8	3	6	120	10	10/20	577
BSS131	SOT23	240	100	360	0.8 to 2.8	–	16	100	10	10/20(2)	581
BSS138	SOT23	50	200	360	0.5 to 1.5	2	3.5	200	5	16/40(2)	584
BST70A	TO-92 var.	80	500	1000	1.5 to 3.5	2	4	500	10	10/15	593
BST72A	TO-92 var.	80	300	830	1.5 to 3.5	7	10	150	5	10/10	597
BST74A	TO-92 var.	200	300	1000	0.8 to 2.8	6	12	250	10	10/25	601
BST76A	TO-92 var.	180	300	1000	0.7 to 2.7	7	10	15	3	10/15	605
BST78	TO-126	450	750	15000(3)	2 to 4	10	14	100	10	10/100	609
BST80	SOT89	80	500	1000	1.5 to 3.5	2	4	500	10	10/15	613
BST82	SOT23	80	175	300	1.5 to 3.5	7	10	150	5	10/10	617
BST84	SOT89	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	621
BST86	SOT89	180	300	1000	0.7 to 2.7	7	10	15	3	10/15	625
BST124	TO-126	250	450	6000	1.4 to 0.6	–	12	250	5	10/30	644
PHN205	SO8 (SOT96)	20	4800	1300	1.0 to 2.8	–	0.05	4400	10	t.b.f.	693
PHN110	SO8 (SOT96)	30	3500	1300	1.0 to 2.8	0.08	0.1	2200	10	40/140	696
PHN210(4)	SO8 (SOT96)	30	3500	1300	1.0 to 2.8	0.08	0.1	2200	10	40/140	700
PHC21025(5)	SO8 (SOT96)										684
PMBF107	SOT23	200	100	250	0.8 to 2.4	20	28	20	2.6	10/20	719
PMBF170	SOT23	60	250	300	0.8 to 3	2.5	5	200	10	10/15	725
VN2406L	TO-92 var.	240	210	1000	0.8 to 2	–	6	500	10	10/30	783
VN2410L	TO-92 var.	240	150	1000	0.8 to 2	–	10	100	2.5	10/30	789
2N7000	TO-92 var.	60	280	830	0.8 to 3	3.5	5.3	75	4.5	10/10	832
2N7002	SOT23	60	180	300	0.8 to 3	3.5	5.3	75	4.5	10/15	838

Notes

1. P_{tot} measured at T_{case} = 25 °C.
2. Typical values.
3. P_{tot} measured at T_{mb} = 75 °C.
4. Double DMOS.
5. Double DMOS complementary N and P channels; for N channel see PHN210, for P channel see PHP225.

P-CHANNEL VERTICAL D-MOS-FETS FOR SWITCHING

P_{tot} measured at T_{amb} = 25 °C.

TYPE NUMBER	ENVELOPE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	$V_{GS(th)}$ (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS208	TO-92 var.	200	200	830	0.8 to 2.8	10	14	200	10	10/30	350
BS250	TO-92 var.	45	250	830	1.3 to 5	9	14	200	10	4/10	355
BSP92	SOT223	240	180	1500	0.8 to 1.8	12	20	180	10	10/30	411
BSP204	TO-92 var.	200	250	1000	0.8 to 2.8	10	15	200	10	10/30	486
BSP204A	TO-92 var.	200	250	1000	0.8 to 2.8	10	15	200	10	10/30	486
BSP205	SOT223	60	275	1500	1.5 to 3.5	7.5	10	200	10	6/15	493
BSP206	SOT223	60	350	1500	1.5 to 3.5	4.5	6	200	10	8/25	497
BSP220	SOT223	200	225	1500	0.8 to 2.8	10	12	200	10	20/30	501
BSP225	SOT223	250	225	1500	0.8 to 2.8	10	15	200	10	10/30	507
BSP230	SOT223	200	550	1500	1.5 to 3.5	–	2.5	750	10	15/30	513
BSP250	SOT223	30	3000	1650	1 to 2.8	0.22	0.25	1000	10	80/140	519
BSP254	TO-92 var.	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	525
BSP254A	TO-92 var.	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	525
BSP304	SOT223	200	550	1500	1.5 to 3.5	–	2.5	170	10	15/30	530
BSS84	SOT23	50	130	250	0.8 to 2	6	10	130	10	3/7[1]	545
BSS92	TO-92 var.	200	250	1000	0.8 to 2.8	10	20	100	10	10/30	565
BSS110	TO-92 var.	50	170	830	0.8 to 2	6	10	170	10	3/7[1]	572
BSS192	SOT89	200	150	1000	0.8 to 2.8	10	20	100	10	10/30	587
BST100	TO-92 var.	60	300	1000	1.5 to 3.5	4.5	6	200	10	4/20	629
BST110	TO-92 var.	50	300	830	1.5 to 3.5	7.5	10	200	10	4/20	633
BST120	SOT89	60	300	1000	1.5 to 3.5	4.5	6	200	10	4/20	637
BST122	SOT89	50	250	1000	1.5 to 3.5	7.5	10	200	10	4/20	641
PHP112	SO8 (SOT96)	20	3100	1300	1.0 to 2.8	–	0.12	2000	10	t.b.f.	706
PHP125	SO8 (SOT96)	30	2300	1300	1.0 to 2.8	0.22	0.25	1000	10	80/140	709
PHP225[2]	SO8 (SOT96)	30	2300	1300	1.0 to 2.8	0.22	0.25	1000	10	80/140	712
PHC21025[3]	SO8 (SOT96)										684

Notes

1. Typical values.
2. Double DMOS.
3. Double DMOS complementary N and P channels; for N channel see PHN210, for P channel see PHP225.

MARKING CODES

Small-signal Field-effect Transistors — Marking codes

Types in SOT23, SOT89, SOT143 and SOT343 envelopes are marked with a code as listed in the following tables.

TYPE NUMBER	MARKING CODE
BF510	S6p
BF511	S7p
BF512	S8p
BF513	S9p
BF545A	M65
BF545B	M66
BF545C	M67
BF556A	M84
BF556B	M85
BF556C	M86
BF861A	M33
BF861B	M34
BF861C	M35
BF901	M01
BF901R	M02
BF904	M04
BF904R	M06
BF904WR	MC
BF908	M26
BF908R	M27
BF908WR	MD
BF909	M28
BF909R	M29
BF989	MAp
BF990A	M87
BF990AR	M85
BF991	M91
BF992	M92
BF992R	M52

TYPE NUMBER	MARKING CODE
BF994S	MGp
BF996S	MHp
BF997	MKp
BF998	MOp
BF998R	$\overline{\text{MOp}}$
BF998WR	MB
BF1100	M56
BF1100R	M57
BF1100WR	MF
BFR30	M1p
BFR31	M2p
BFR200	M20
BSD22	M32
BSN20	M8p
BSN22	M18
BSR56	M4p
BSR57	M5p
BSR58	M6p
BSS83	M74
BSS84	Sp
BSS87	KA
BSS123	SAp
BSS131	SR
BSS138	SS
BSS192	KB
BST80	KM
BST82	02p
BST84	KN
BST86	KO

TYPE NUMBER	MARKING CODE
BST120	LM
BST122	LN
PMBF107	pKz
PMBF170	pKX
PMBF4391	p6J
PMBF4392	p6K
PMBF4393	p6G
PMBF4416	p6A
PMBF4416A	M16
PMBF5484	p6B
PMBF5485	p6M
PMBF5486	p6H
PMBFJ108	p08
PMBFJ109	p09
PMBFJ110	p10
PMBFJ111	p11
PMBFJ112	p12
PMBFJ113	p13
PMBFJ174	p6X
PMBFJ175	p6W
PMBFJ176	p6S
PMBFJ177	p6Y
PMBFJ210	M68
PMBFJ211	M69
PMBFJ212	M70
PMBFJ308	M08
PMBFJ309	M09
PMBFJ310	M10
2N7002	702

GENERAL

QUALITY

Total Quality Management

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

QUALITY ASSURANCE

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

PARTNERSHIPS WITH SUPPLIERS

Ship-to-stock, statistical process control and ISO 9000 audits.

QUALITY IMPROVEMENT PROGRAMME

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A germanium or other material with a band gap of 0.6 to 1 eV

B silicon or other material with a band gap of 1 to 1.3 eV

C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R compound materials, e.g. cadmium sulphide

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A diode; signal, low power

B diode; variable capacitance

C transistor; low power, audio frequency

D transistor; power, audio frequency

E diode; tunnel

F transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter; see under Section "Serial number".

H diode; magnetic sensitive

L transistor; power, high frequency

N photocoupler

P radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q radiation generator; e.g. LED, laser; with special third letter

R control or switching device; e.g. thyristor, low power; with special third letter

S transistor; low power, switching

T control or switching device; e.g. thyristor, low power; with special third letter

U transistor; power, switching

W surface acoustic wave device

X diode; multiplier, e.g. varactor, step recovery

Y diode; rectifying, booster

Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1)

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Version letter

A letter may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic

device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS

The letter symbols for transistors detailed in this section are based on IEC publication number 148.

Basic letters

In the representation of currents, voltages and powers, lower-case letter symbols are used to indicate all instantaneous values that vary with time. All other values are represented by upper-case letters.

Electrical parameters[1] of external circuits and of circuits in which the device forms only a part are represented by upper-case letters. Lower-case letters are used for the representation of electrical parameters inherent in the device. Inductances and capacitances are always represented by upper-case letters.

The following is a list of basic letter symbols used with semiconductor devices:

B, b susceptance (imaginary part of an admittance)
C capacitance
G, g conductance (real part of an admittance)
H, h hybrid parameter
I, i current
L inductance
P, p power
R, r resistance (real part of an impedance)
V, v voltage
X, x reactance (imaginary part of an impedance)
Y, y admittance
Z, z impedance

(1) For the purpose of this publication, the term 'electrical parameters' applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

Subscripts

Upper-case subscripts are used for the indication of:

- continuous (DC) values (without signal), e.g. I_D
- instantaneous total values, e.g. i_D
- average total values, e.g. $I_{D(AV)}$
- peak total values, e.g. I_{DM}
- root-mean-square total values, e.g. $I_{D(RMS)}$.

Lower-case subscripts are used for the indication of values applying to the varying component alone:

- instantaneous values, e.g. i_b
- root-mean-square values, e.g. $I_{d(rms)}$
- peak values, e.g. I_{dm}
- average values, e.g. $I_{d(av)}$.

The following is a list of subscripts used with basic letter symbols for semiconductor devices:

A, a	anode
amb	ambient
(AV), (av)	average value
B, b	base
(BO)	breakover
(BR)	breakdown
case	case
C, c	collector
C	controllable
D, d	drain
E, e	emitter
F, f	fall, forward (or forward transfer)
G, g	gate
H	holding
h	heatsink
I, i	input
j-a	junction to ambient
j-mb	junction to mounting base
K, k	cathode
L	load
M, m	peak value
(min)	minimum
(max)	maximum
mb	mounting base
O, o	as third subscript: the terminal not mentioned is open-circuit
(OV)	overload
P, p	pulse
Q, q	turn-off
R, r	as first subscript: reverse (or reverse transfer), rise. As second subscript: repetitive, recovery. As third subscript: with a specified resistance between the terminal not mentioned and the reference terminal
(RMS), (rms)	root-mean-square value
S, s	as first subscript: series, source, storage, stray, switching. As second subscript: surge (non-repetitive). As third subscript: short circuit between the terminal not mentioned and the reference terminal
stg	storage
th	thermal
TO	threshold
tot	total
W	working
X, x	specified circuit
Z, z	reference or regulator (zener)
1	input (four-pole matrix)
2	output (four-pole matrix).

Applications and examples

TRANSISTOR CURRENTS

The first subscript indicates the terminal carrying the current (conventional current flow from the external circuit into the terminal is positive).

Examples: I_D, i_D, i_d, I_{dm}.

TRANSISTOR VOLTAGES

A voltage is indicated by the first two subscripts: the first identifies the terminal at which the voltage is measured and the second the reference terminal or the circuit node. The second subscript may be omitted when there is no possibility of confusion.

Examples: V_{GS}, v_{GS}, v_{gs}, V_{gsm}.

SUPPLY VOLTAGES OR CURRENTS

Supply voltages or supply currents are indicated by repeating the appropriate terminal subscript.

Examples: V_{DD}, I_{SS}.

A reference terminal is indicated by a third subscript.

Example: V_{DDS}.

DEVICES WITH MORE THAN ONE TERMINAL OF THE SAME KIND

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal, followed by a number. Hyphens may be used to avoid confusion in multiple subscripts.

Examples:

I_{G2}	continuous (DC) current flowing into the second gate terminal
V_{G2-S}	continuous (DC) voltage between the terminals of second gate and source.

MULTIPLE DEVICES

For multiple unit devices, the subscripts are modified by a number preceding the letter subscript. Hyphens may be used to avoid confusion in multiple subscripts.

Examples:

I_{2D}	continuous (DC) current flowing into the drain terminal of the second unit
V_{1D-2D}	continuous (DC) voltage between the drain terminals of the first and second units.

ELECTRICAL PARAMETERS

The upper-case variant of a subscript is used for the designation of static (DC) values.

Examples:

g_{FS}	static value of forward transconductance in common-source configuration (DC current gain)
R_{DS}	DC value of the drain-source resistance.

The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript is used for the designation of small-signal values.

Examples:

g_{fs}	small-signal value of the short-circuit forward transconductance in common-source configuration
$Z_i = R_i + jX_i$	small-signal value of the input impedance.

If more than one subscript is used, subscripts for which a choice of style is allowed, the subscripts chosen are all upper-case or all lower-case.

Examples: h_{FE}, y_{RE}, h_{fe}, g_{FS}.

FOUR-POLE MATRIX PARAMETERS

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer.

Examples: h_i (or h_{11}), h_o (or h_{22}), h_f (or h_{21}), h_r (or h_{12}).

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E}).

DISTINCTION BETWEEN REAL AND IMAGINARY PARTS

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts are used. If basic symbols for the real and imaginary parts exist, these may be used.

Examples: $Z_i = R_i + jX_i$, $y_{fe} = g_{fe} + jb_{fe}$.

If such symbols do not exist or are not suitable, the notation shown in the following examples is used.

Examples:

Re (h_{ib}) etc. for the real part of h_{ib}

Im (h_{ib}) etc. for the imaginary part of h_{ib}.

S-PARAMETER DEFINITIONS

The S-parameter symbols in this section are based on IEC publication 747-7.

S-parameters (return losses or reflection coefficients) of a module can be defined as the S_{11} and the S_{22} of a two-port network (see Fig.1).

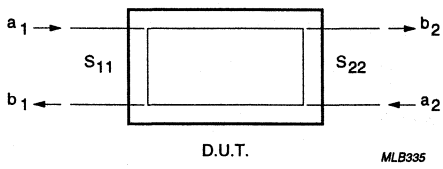


Fig.1 Two-port network with reflection coefficients S11 and S22.

$$b_1 = S_{11} \cdot a_1 + S_{12} \cdot a_2 \quad (1)$$

$$b_2 = S_{21} \cdot a_1 + S_{22} \cdot a_2 \quad (2)$$

where:

$$a_1 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_1) = \text{signal into port 1} \quad (3)$$

$$a_2 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_2 + Z_o \cdot i_2) = \text{signal into port 2}$$

$$b_1 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_1) = \text{signal out port 1} \quad (4)$$

$$b_2 = \frac{1}{2 \cdot \sqrt{Z_o}} \cdot (V_1 + Z_o \cdot i_2) = \text{signal out port 2}$$

From (1) and (2) formulae for the return losses can be derived:

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2 = 0} \quad (5)$$

$$S_{22} = \frac{b_2}{a_2}\Big|_{a_1 = 0} \quad (6)$$

In (5), $a_2 = 0$ means output port terminated with Z_o (derived from formula (4)).

In (6), $a_1 = 0$ means input port terminated with Z_o (derived from formula (3)).

Measurement

The return losses are measured with a network analyzer after calibration, where the influence of the test jig is eliminated. The necessary termination of the other port with Z_o is done automatically by the network analyzer.

The network analyser must have a directivity of at least 40 dB to obtain an accuracy of 0.5 dB when measuring return loss figures of 20 dB. A full two-port correction method can be used to improve the accuracy.

TAPE AND REEL PACKING

Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286-2 and 286-3). Additionally, the tape is an ideal shipping container.

Packing (TO-92 leaded types)

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel and per ammopack is 2000. The ammopack has 80 layers of 25 transistors each. Each layer contains 25 transistors, plus one empty position in order to fold the layer correctly.The ammopack is accessible from both sides, enabling the user to choose between 'normal' (see Fig.3) and 'reverse' tape. 'Normal' is indicated by a plus sign (+) on the ammopack and 'reverse' by a minus sign (–). In the European version, the leading pin is the source.

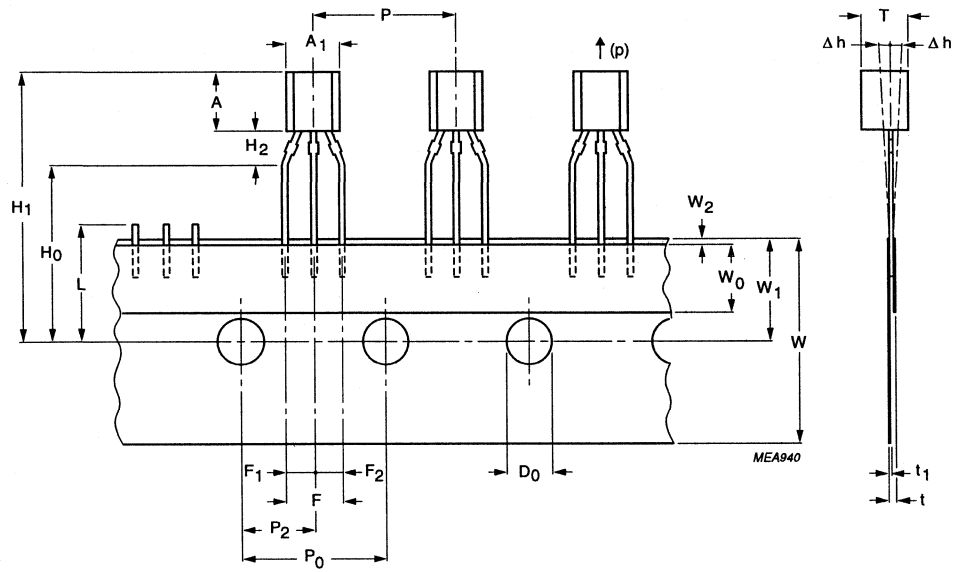


Fig.2 TO-92 transistors on tape.

Table 1 Tape specification (TO-92 leaded types)

SYMBOL	DIMENSION	SPECIFICATIONS					REMARKS
		MIN.	NOM.	MAX.	TOL.	UNIT	
A_1	body width	4	–	4.8	–	mm	
A	body height	4.8	–	5.2	–	mm	
T	body thickness	3.5	–	3.9	–	mm	
P	pitch of component	–	12.7	–	±1	mm	
P_0	feed hole pitch	–	12.7	–	±0.3	mm	
	cumulative pitch error	–	–	–	±0.1		note 1
P_2	feed hole centre to component centre	–	6.35	–	±0.4	mm	to be measured at bottom of clinch
F	distance between outer leads	–	5.08	–	+0.6/–0.2	mm	
Δh	component alignment	–	0	1	–	mm	at top of body
W	tape width	–	18	–	±0.5	mm	
W_0	hold-down tape width	–	6	–	±0.2	mm	
W_1	hole position	–	9	–	+0.7/–0.5	mm	
W_2	hold-down tape position	–	0.5	–	±0.2	mm	
H_0	lead wire clinch height	–	16.5	–	±0.5	mm	
H_1	component height	–	–	23.25	–	mm	
L	length of snipped leads	–	–	11	–	mm	
D_0	feed hole diameter	–	4	–	±0.2	mm	
t	total tape thickness	–	–	1.2	–	mm	t_1 = 0.3 to 0.6
F_1, F_2	lead-to-lead distance	–	–	–	+0.4/–0.2	mm	
H_2	clinch height	–	–	–	–	mm	
(p)	pull-out force	6	–	–	–	N	

Note

1. Measured over 20 devices.

Dropouts

A maximum of 0.5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

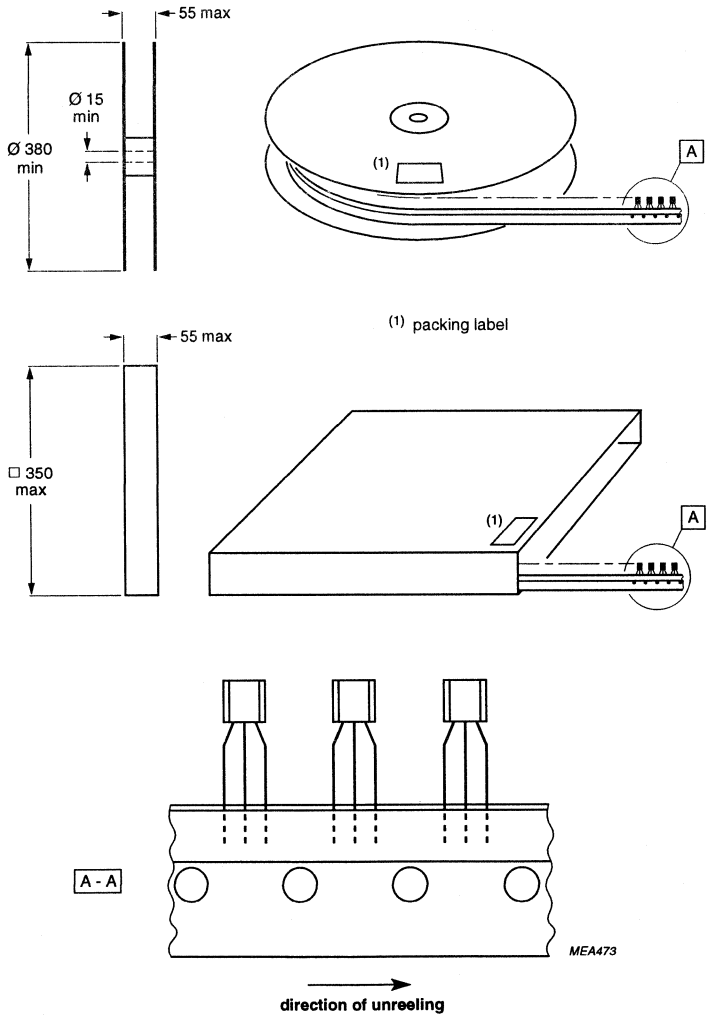
Tape splicing

Splice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Figs 2 and 4).

Bulk packing

In addition to TO-92 on tape, TO-92 can also be delivered in bulk. Products are packed in boxes in foil and plastic bags with 1000 pieces to a bag and 5 bags to a box.

As well as the standard TO-92 with straight leads, (see Fig.5) leads with delta pinning are available in bulk, on request (see Fig.6).



Dimensions in mm.

Fig.3 Dimensions of reel and box.

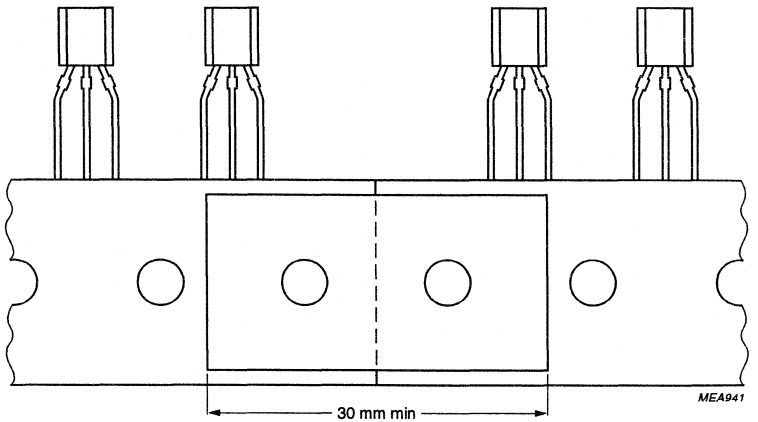
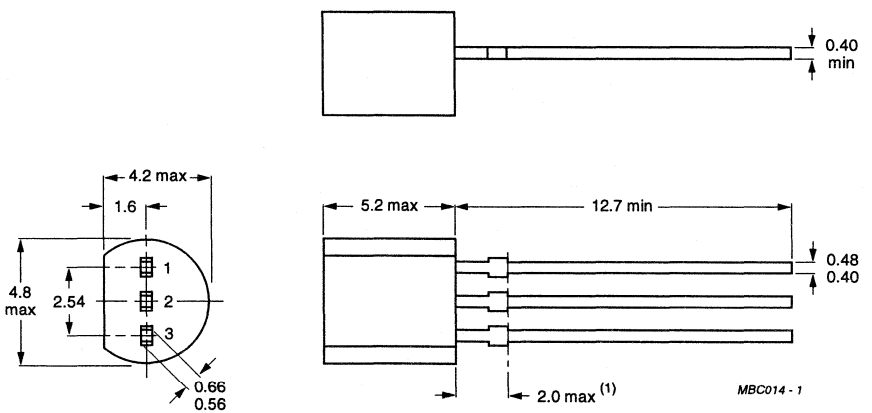


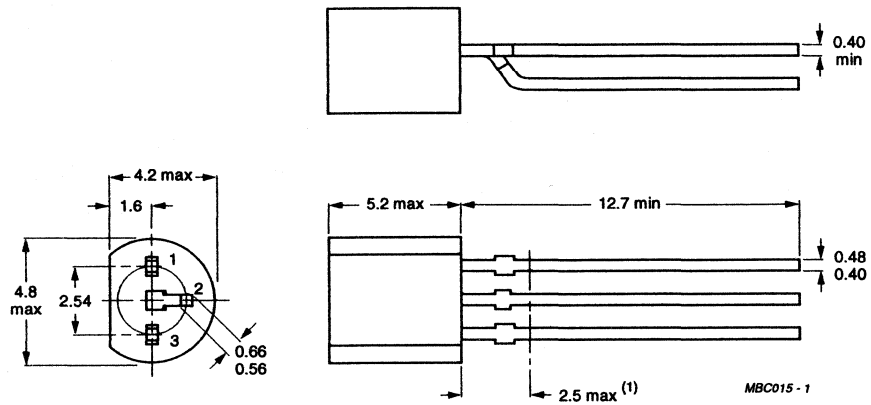
Fig.4 Joining tape with splicing patch.



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.5 TO-92 with straight leads.



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.6 TO-92 with delta pinning.

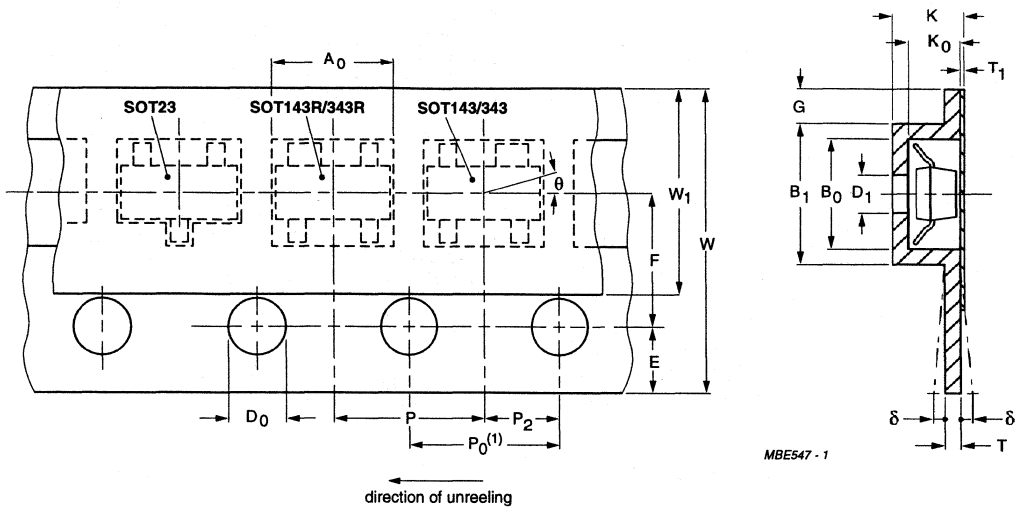
Packing SMD types

Table 2 Packing quantities per reel (SMD types)

PACKAGE	180 mm REEL	330 mm REEL
SOT23	3000	10000
SOT89	1000	4000
SOT143	3000	10000
SOT143R	3000	10000
SOT223	1000	4000
SOT343	3000	10000
SOT343R	3000	10000
SO8 (SOT96)	1000	2500

Table 3 Packing quantities per tube (SMD types)

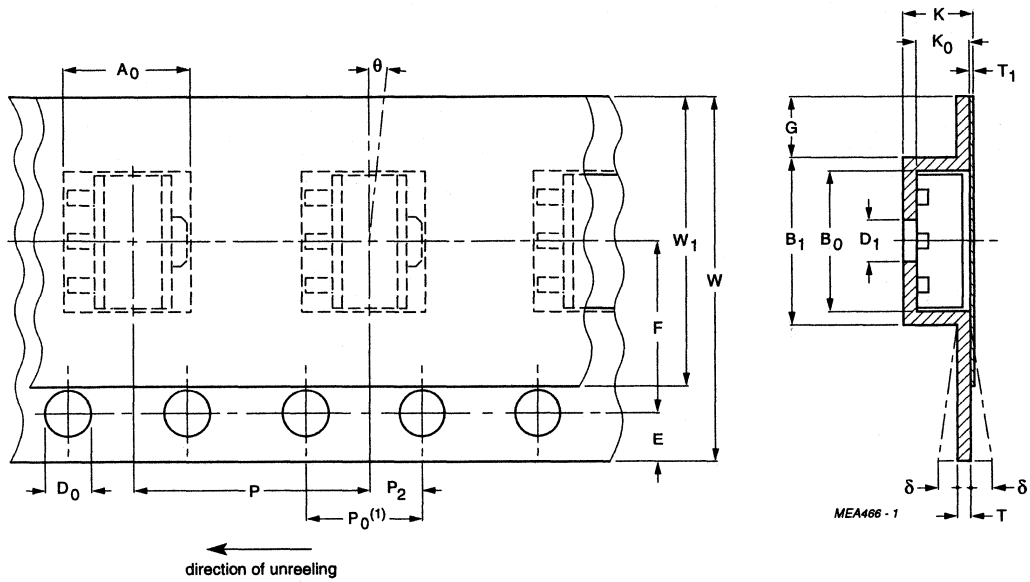
PACKAGE	SPQ	PQ
SO8 (SOT96)	100	2000



For dimensions see Table 5.

(1) Tolerance over any 10 pitches: ±0.2 mm.

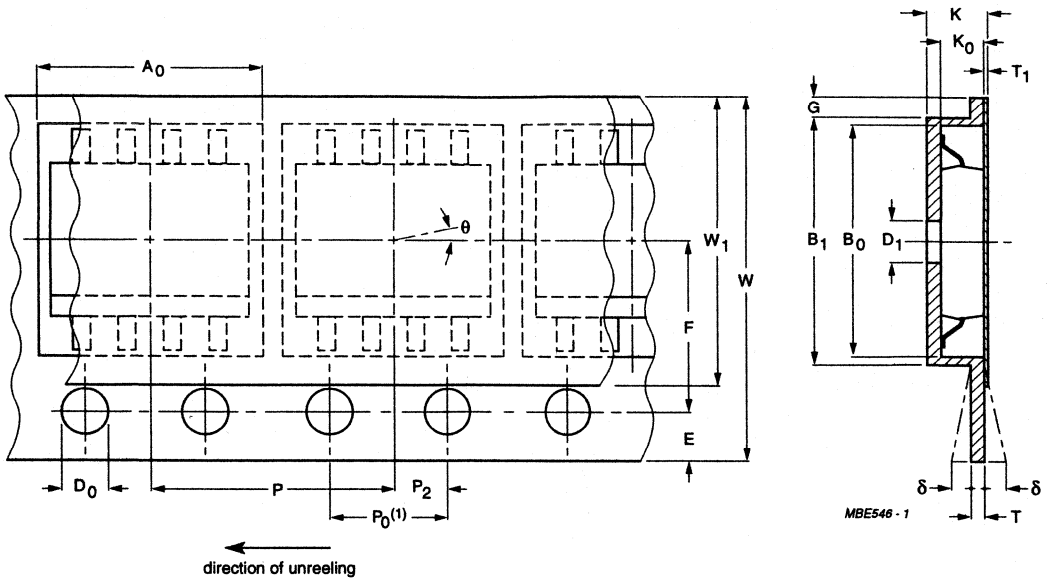
Fig.7 Specification for 8 mm tape (SOT23, SOT143, SOT143R, SOT343 and SOT343R).



For dimensions see Table 5.

(1) Tolerance over any 10 pitches: ±0.2 mm.

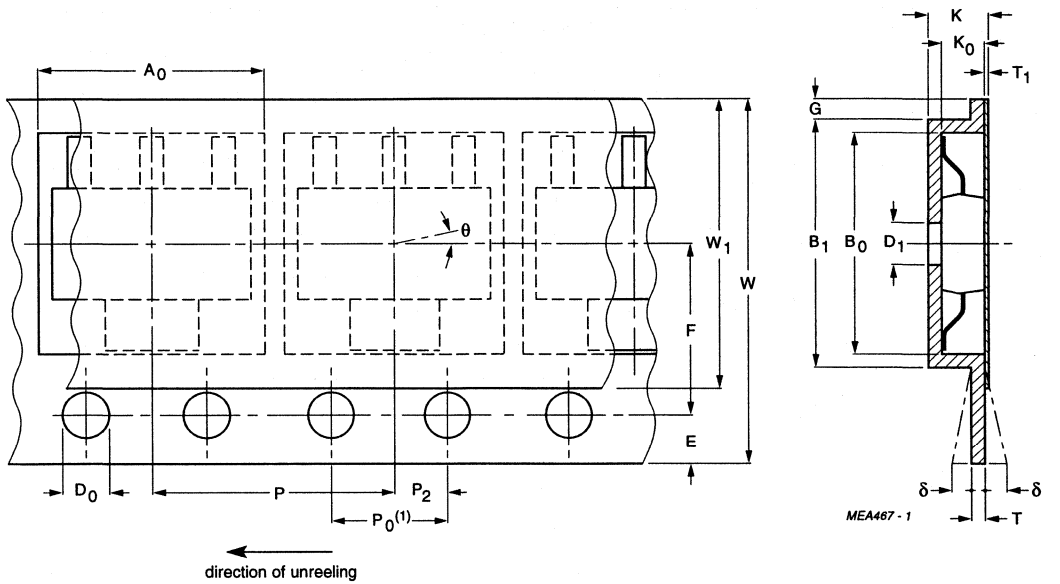
Fig.8 Specification for 12 mm tape (SOT89).



For dimensions see Table 5.

(1) Tolerance over any 10 pitches: ±0.2 mm.

Fig.9 Specification for 12 mm tape (SOT96).



For dimensions see Table 5.

(1) Tolerance ove any 10 pitches: ±0.2 mm.

Fig.10 Specification for 12 mm tape (SOT223).

Table 4 Carrier tape widths for packages

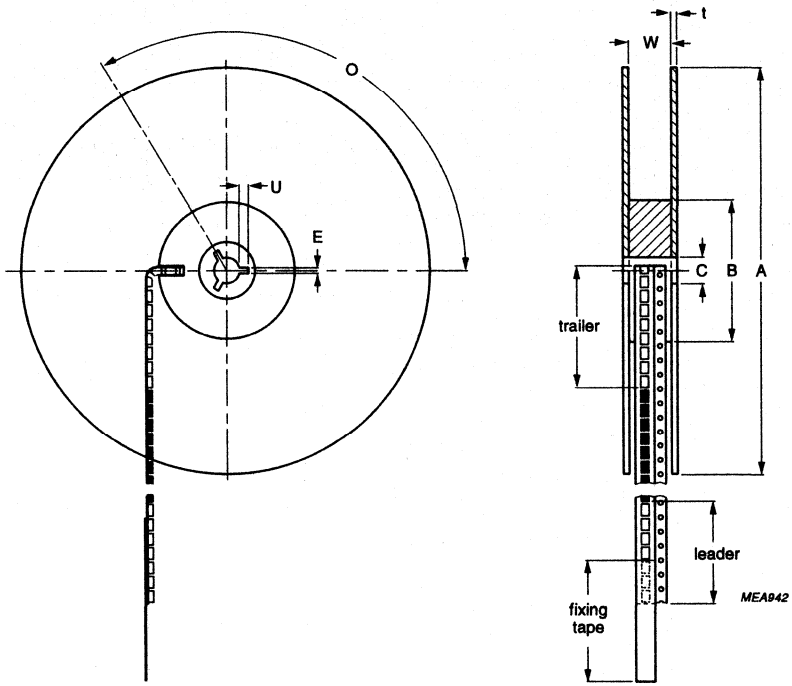
CARRIER TAPE	
8 mm	**12 mm**
SOT23	SOT89
SOT143(R)	SOT223
SOT343(R)	SOT96 (SO8)

Table 5 SMD packages: tape dimensions (in mm)

DIMENSION (Figs 7 to 10)	CARRIER TAPE		TOLERANCE
	8 mm	12 mm	
Overall dimensions			
W	8.0	12.0	±0.2
K	<1.5	<2.4	–
G	>0.75	>0.75	–
Sprocket holes; note 1			
D_0	1.5	1.5	+0.1/–0
E	1.75	1.75	±0.1
P_0	4.0	4.0	±0.1
Relative placement compartment			
P_2	2.0	2.0	±0.1
F	3.5	5.5	±0.05
Compartment			
A_0	Compartment dimensions depend on package size. Maximum clearance between device and compartment is 0.3 mm; the minimum clearance ensures that the device is not totally restrained within the compartment.		
B_0			
B_1			
K_0			
D_1	>1.0	>1.5	–
P	4.0	8.0	±0.1
θ	<15°	<15°	–
Cover tape; note 2			
W_1	<5.4	<9.5	–
T_1	<0.1	<0.1	–
Carrier tape			
W	8.0	12.0	±0.2
T	<0.2	<0.2	–
δ	<0.3	<0.3	–

Notes

1. Tolerance over any 10 pitches ±0.2 mm.
2. The cover tape shall not overlap the tape or sprocket holes.



For dimensions see Table 6.

Fig.11 Reel specification.

Table 6 Reel dimensions (in mm)

DIMENSION (see Fig.11)	**8 mm TAPE**	**12 mm TAPE**	**TOLERANCE**
Flange			
A	180 [1] – 286 or 330	180 or 330	±0.5
t	1.5	1.5	+0.5/–0.1
W	8.4	12.4	18.0+0.2
Hub			
B	62	62	±1.5
C	12.75	12.75	+0.15/–0.2
Key slot			
E	2	2	±0.2
U	4	4	±0.5
O	120°	120°	–

Note

1. Large reel diameter depends on individual package (286 or 350).

MOUNTING AND SOLDERING

Mounting methods

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting (SMD). Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly. Surface mounting techniques are complex and this chapter gives only a simplified overview of the subject.

Although many electronic components are available as surface mounting types, some are not and this often leads to the use of through-hole as well as surface mounting components on one substrate (a mixed print). The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

Reflow soldering

SOLDER PASTE

Most reflow soldering techniques utilize a paste that is a mixture of flux and solder. The solder paste is applied to the substrate before the components are placed. It is of sufficient viscosity to hold the components in place and, therefore, an application of adhesive is not required. Drying of the solder paste by preheating increases the viscosity and prevents any tendency for the components to become displaced during the soldering process. Preheating also minimizes thermal shock and drives off flux solvents.

Screen printing

This is the best high-volume production method of solder paste application. An emulsion-coated, fine mesh screen with apertures etched in the emulsion to coincide with the surfaces to be soldered is placed over the substrate. A squeegee is passed across the screen to force solder paste through the apertures and on to the substrate. The layer thickness of screened solder paste is usually between 150 and 200 μm.

Stencilling

In this method a stencil with etched holes to pass the paste is used. The thickness of the stencil determines the amount of amount of solder paste that is deposited on the substrate. This method is also suited to high-volume work.

Dispensing

A computer-controlled pressure syringe dispenses small doses of paste to where it is required. This method is mainly suitable for small production runs and laboratory use.

Pin transfer

A pin picks up a droplet of solder paste from a reservoir and transfers it to the surface of the substrate or component. A multi-pin arrangement with pins positioned to match the substrate is possible and this speeds up the process time.

REFLOW TECHNIQUES

Thermal conduction

The prepared substrates are carried on a conveyor belt, first through a preheating stage and then through a soldering stage. Heat is transferred to the substrate by conduction through the belt. Figure 12 shows a theoretical time/temperature relationship for thermal conduction reflow soldering. This method is particularly suited to thick film substrates and is often combined with infrared heating.

Infrared

An infrared oven has several heating elements giving a broad spectrum of infrared radiation, normally above and below a closed loop belt system. There are separate zones for preheating, soldering and cooling. Dwell time in the soldering zone is kept as short as possible to prevent damage to components and substrate. A typical heating profile is shown in Fig.13. This reflow method is often applied in double-sided prints.

Vapour phase

A substrate is immersed in the vapours of a suitable boiling liquid. The vapours transfer latent heat of condensation to the substrate and solder reflow takes place. Temperature is controlled precisely by the boiling point of the liquid at a given pressure. Some systems employ two vapour zones, one above the other. An elevator tray, suspended from a hoist mechanism passes the substrate vertically through the first vapour zone into the secondary soldering zone and then hoists it out of the vapour to be cooled. A theoretical time/temperature relationship for this method is shown in Fig.14.

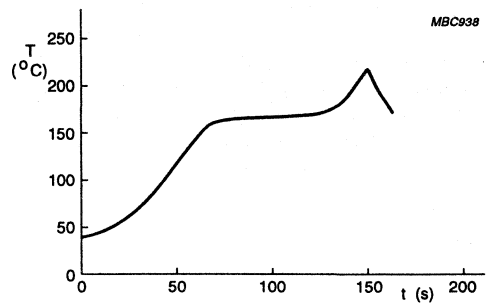


Fig.12 Theoretical time / temperature curve for a typical thermal conductive reflow cycle.

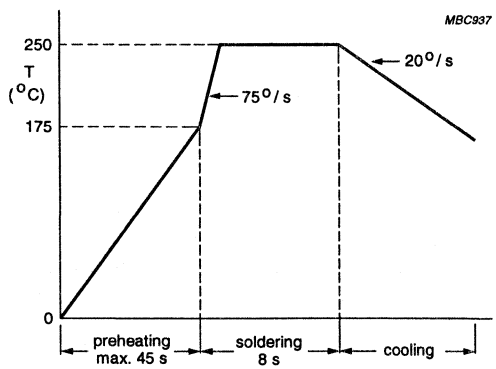


Fig.13 Typical temperature profile of an infrared oven operating at a belt speed of 0.41 mm / min.

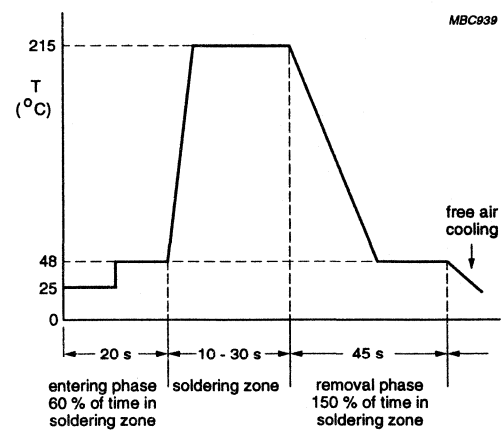


Fig.14 Theorectical time / temperature curve relationship for dual vapour reflow soldering.

Wave soldering

This soldering technique is not recommended for SOT89.

ADHESIVE APPLICATION

Since there are no connecting wires to retain them, leadless and short-leaded components are held in place with adhesive for wave soldering. A spot of adhesive is carefully placed between each SMD and the substrate. The adhesive is then heat-cured to withstand the forces of the soldering process, during which the components are fully immersed in solder. There are several methods of adhesive application.

Pin transfer method

A pin is used to transfer a droplet of adhesive from a reservoir to a precise position on the surface where it is required. The size of the droplet depends on pin diameter, depth to which the pin is dipped in the reservoir, rheology of the adhesive, and the temperature of adhesive and surrounds. The pin can be part of a pin array (bed of nails) that corresponds exactly with the required adhesive positions on the substrate. With this method, adhesive can be applied to the whole of one side of a substrate in one operation and is therefore suitable for high-volume production and can be used with pre-loaded mixed prints.

Alternatively, pins can be used to transfer adhesive to the components before they are placed on the substrate. This adds flexibility to production runs where variations in layout must be accommodated.

Screen printing method

A fine mesh screen is coated with emulsion except in the positions where the adhesive is required to pass. The screen is placed on the substrate and a squeegee passing across it forces adhesive through the uncoated parts of the screen. The amount of adhesive printed-through depends on the size of the uncoated screen areas, the thickness of the screen coating, the rheology of the adhesive and various machine parameters. With this method, the substrate must be flat and pre-loaded mixed prints cannot be accommodated.

Pressure syringe method

A computer-controlled syringe dispenses adhesive from an enclosed reservoir by means of pulses of compressed air. The adhesive dot size depends on the size of the syringe nozzle, the duration and pressure of the pulsed air and the viscosity of the adhesive. This method is most suited to low volume production. An advantage is the flexibility provided by computer programmability.

FLUXING

The quality of the soldered connections between components and substrate is critical for circuit performance and reliability. Flux promotes solderability of the connecting surfaces and is chosen for the following attributes:

- removal of surface oxides
- prevention of reoxidation
- transference of heat from source to joint area
- residue that is non-corrosive or, if residue is corrosive, should be easy to clean away after soldering
- ability to improve wettability (readiness of a metal surface to form an alloy at its interface with the solder) to ensure strong joints with low electrical resistance
- suitability for the desired method of flux application.

In wave soldering, liquified flux is usually applied as a foam, a spray or in a wave.

Foam

Flux foam is made by forcing low-pressure, water-free clean air through an aerator immersed in liquid flux. Fine bubbles of flux are directed onto the substrate/component surfaces where they burst and form a thin, even layer. The flux also penetrates any plated-through holes. The flux has to be chosen for its foaming capabilities.

Spray

Several methods of spray fluxing exist, the most common involves a mesh drum rotating in liquid flux. Air is blown into the drum which, when passing through the fine mesh, directs a spray of flux onto the underside of the substrate. The amount of flux deposited is controllable by the speed of the substrate passing through the spray, the speed of rotation of the drum and the density of the flux.

Wave

A wave fluxer creates a double flowing wave of liquid flux which adheres to the surface as the substrate passes through. Wave height control is essential and a soft wipe-off brush is usually incorporated to remove excess flux from the substrate.

PRE-HEATING

Pre-heating of the substrate and components is performed immediately before soldering. This reduces thermal shock as the substrate enters the soldering process, causes the flux to become more viscous and accelerates the chemical action of the flux and so speeds up the soldering action.

SOLDERING

Wave soldering is usually the best method to use when high throughput rates are required. The single-wave soldering principle (see Fig.15) is the most straight forward method and can be used on simple substrates with two-terminal SMD components. More complex substrates with increased circuit density and closer spacing of conductors can pose the problems of nonwetting (dry joints) and solder bridging. Bridging can occur across the closely spaced leads of multi-leaded devices as well as across adjacent leads on neighbouring components. Nonwetting is usually caused by components with plastic bodies. The plastic is not wetted by solder and creates a depression in the solder wave, which is augmented by surface tension. This can cause a shadow behind the component and prevent solder from reaching the joint surfaces. A smooth laminar solder wave is required to avoid bridging and a high pressure wave is needed to completely cover the areas that are difficult to wet. These conflicting demands are difficult to attain in a single wave but dual wave techniques go a long way in overcoming the problem.

In a dual wave machine (see Fig.16), the substrate first comes into contact with a turbulent wave which has a high vertical velocity. This ensures good solder contact with both edges of the components and prevents joints from being missed. The second smooth laminar wave completes the formation of the solder fillet, removes excess solder and prevents bridging. Figure 17 indicates the time/temperature relationship measured at the soldering site in dual wave soldering.

New methods of wave soldering are developing continually. For example, the Omega System is a single wave agitated by pulses, which combines the functions of smoothness and turbulence. In another, a lambda wave injects air bubbles in the final part of the wave. A further innovation is the hollow jet wave in which the solder wave flows in the opposite direction to the substrate.

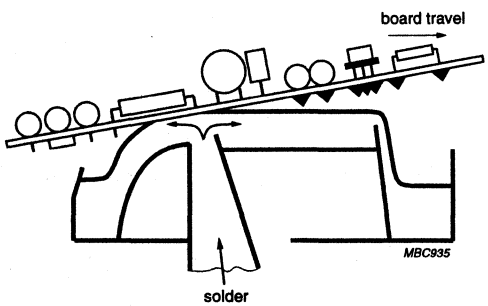


Fig.15 Single wave soldering principle.

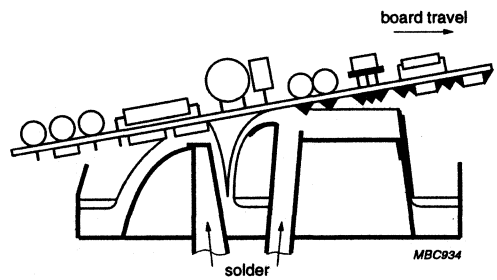


Fig.16 Dual wave soldering principle.

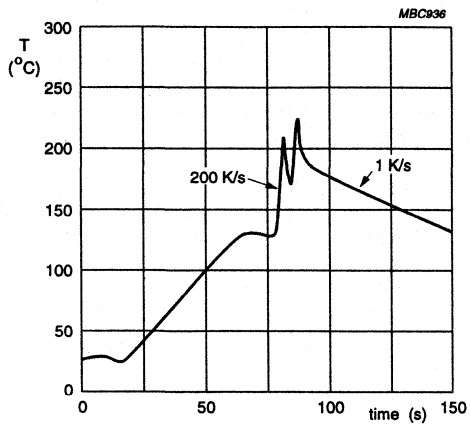


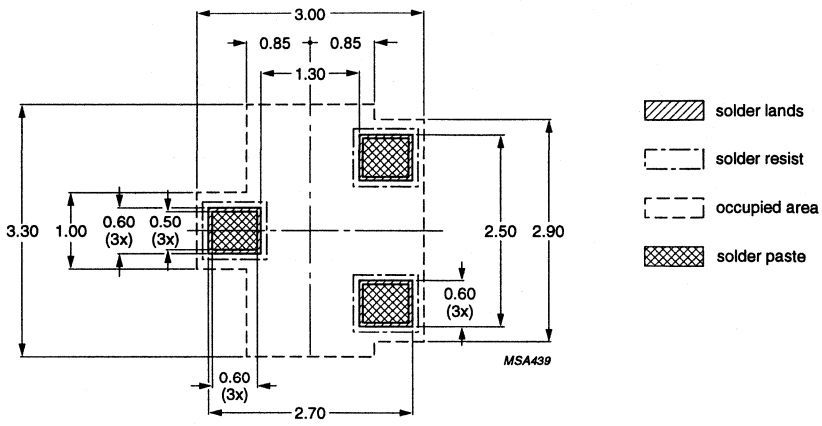
Fig.17 Typical time-temperature curve measured at the soldering site.

Footprint design

The footprint design of a component for surface mounting is influenced by many factors:

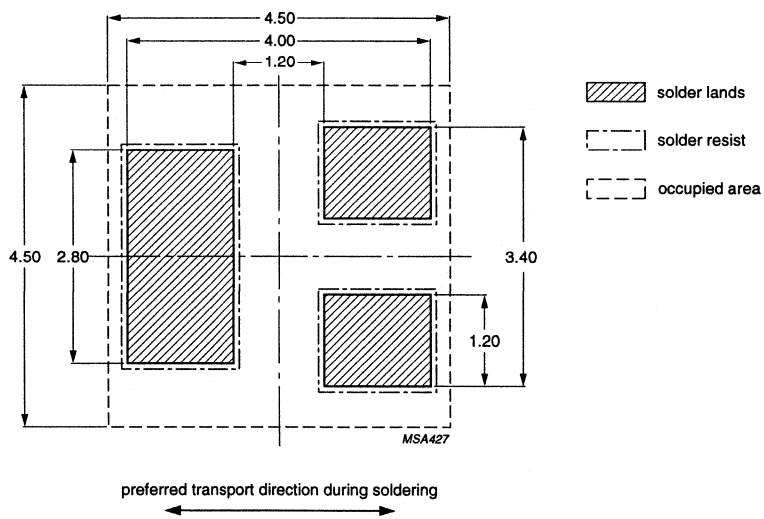
- features of the component, its dimensions and tolerances
- circuit board manufacturing processes
- desired component density
- minimum spacing between components
- circuit tracks under the component
- component orientation (if wave soldering)
- positional accuracy of solder resist to solder lands
- positional accuracy of solder paste to solder lands (if reflow soldering)
- component placement accuracy
- soldering process parameters
- solder joint reliability parameters.

SOT23 FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

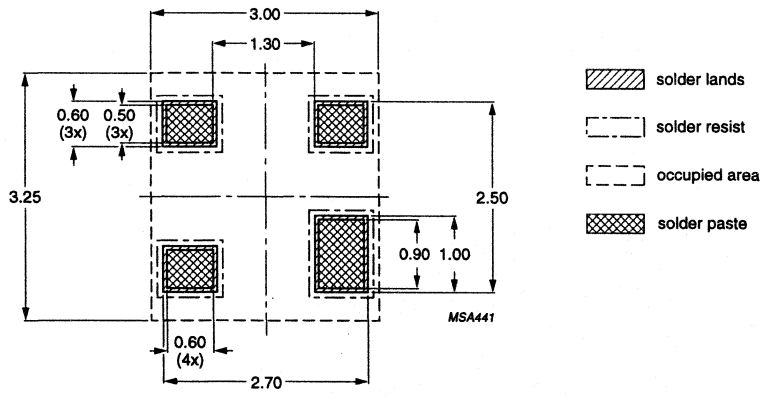
Fig.18 Reflow soldering footprint for SOT23; typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

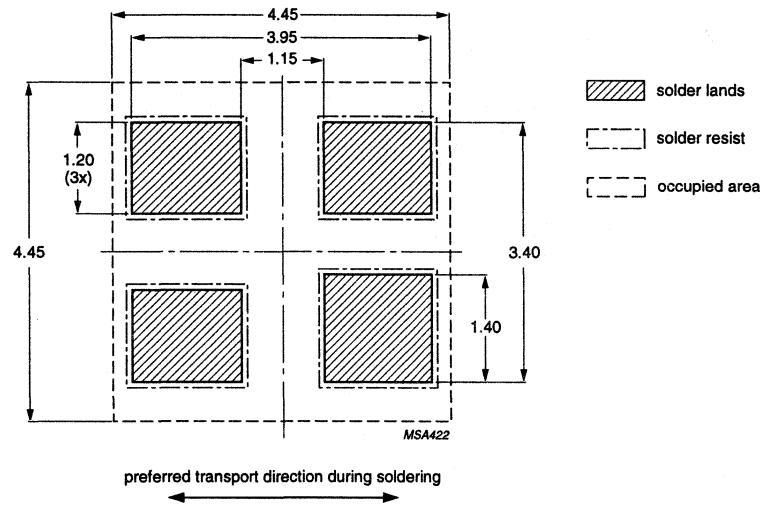
Fig.19 Wave soldering footprint for SOT23; typical dimensions.

SOT143/SOT143R FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

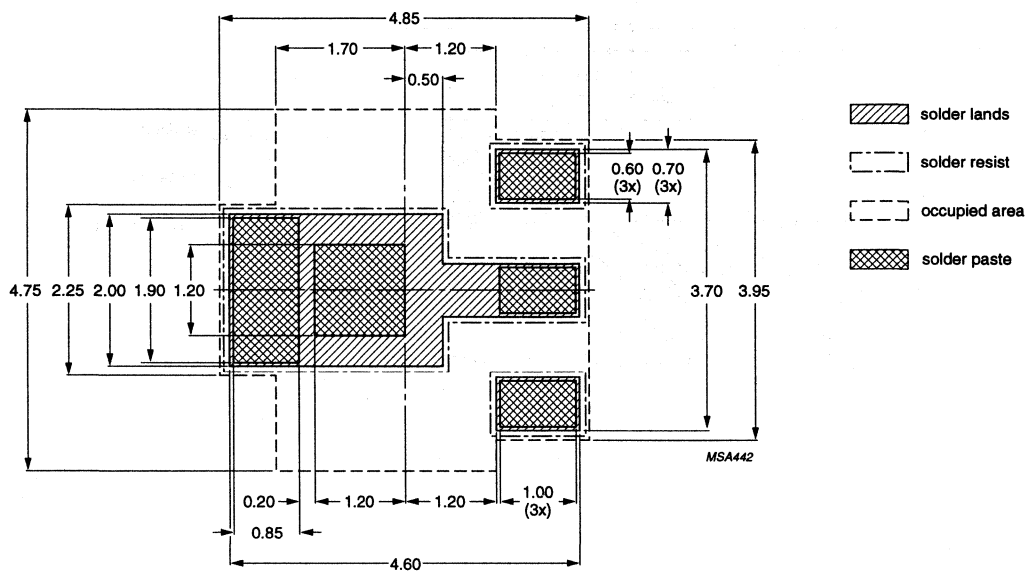
Fig.20 Reflow soldering footprint for SOT143; typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

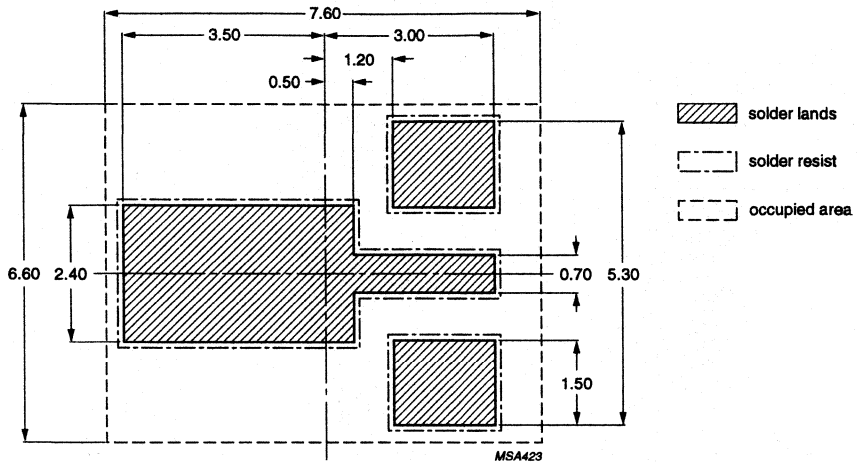
Fig.21 Wave soldering footprint for SOT143; typical dimensions.

SOT89 FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

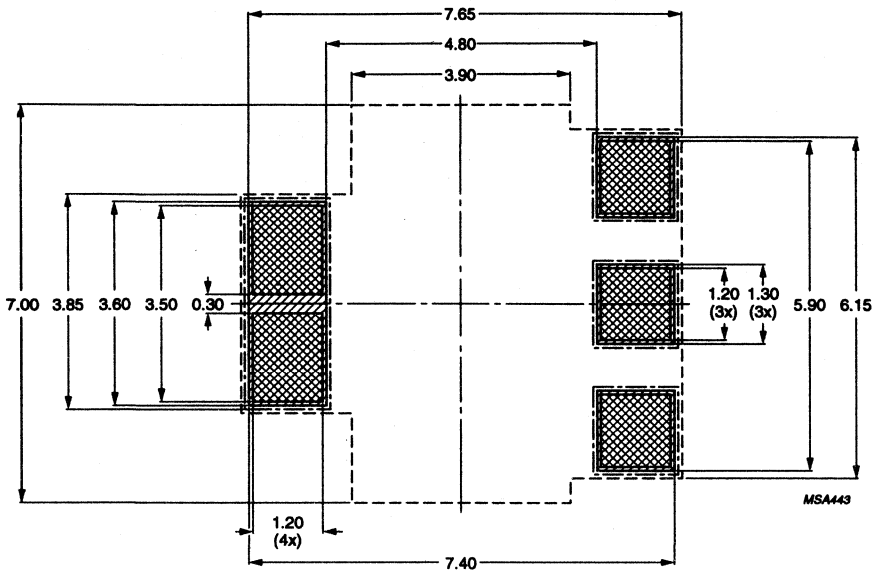
Fig.22 Reflow soldering footprint for SOT89; typical dimensions.



We do not recommend SOT89 for wave soldering, SOT223 is preferred.
Dimensions in mm.
Placement accuracy: ±0.25 mm.

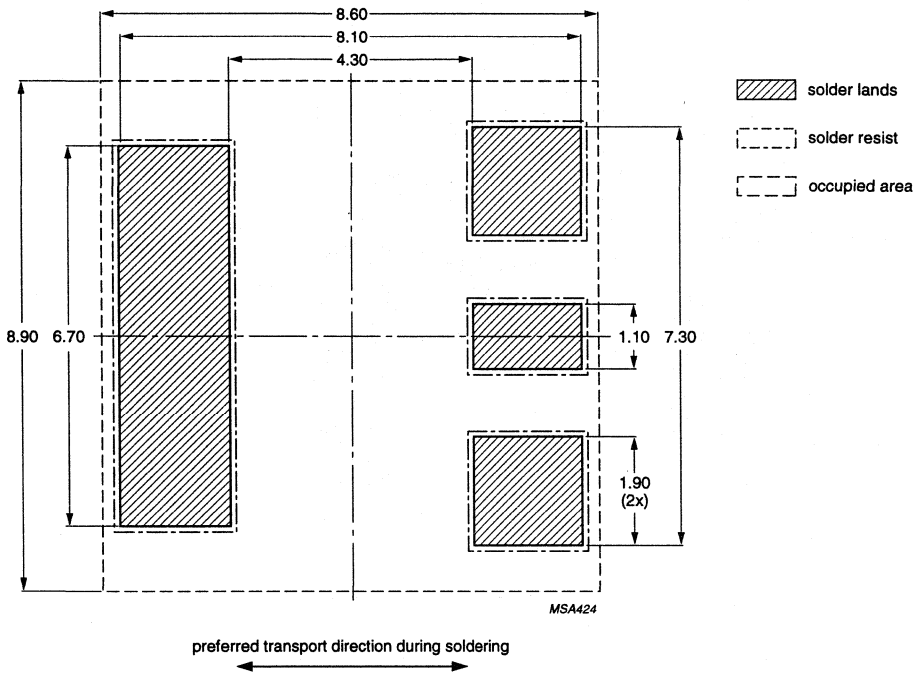
Fig.23 Wave soldering footprint for SOT89: typical dimensions.

SOT233 FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

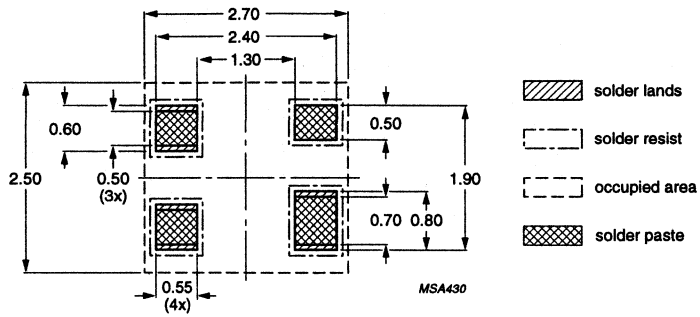
Fig.24 Reflow soldering footprint for SOT223; typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

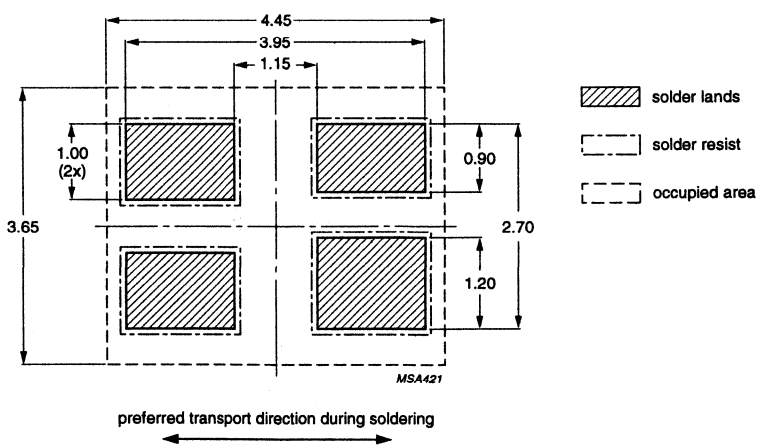
Fig.25 Wave soldering footprint for SOT223; typical dimensions.

SOT343 FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

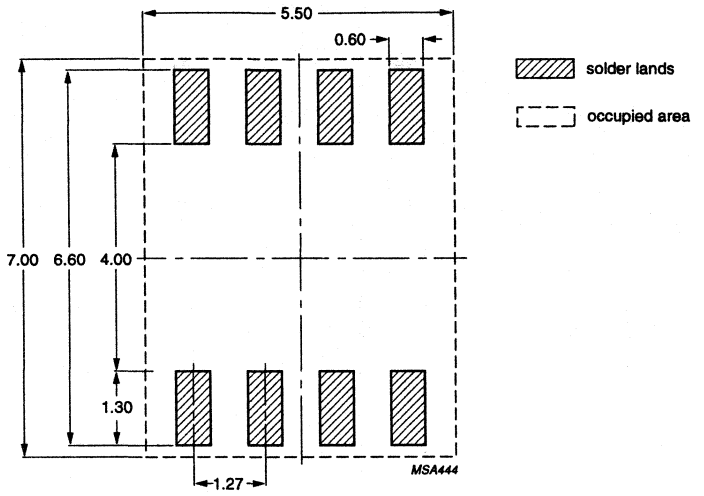
Fig.26 Reflow soldering footprint for SOT343; typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

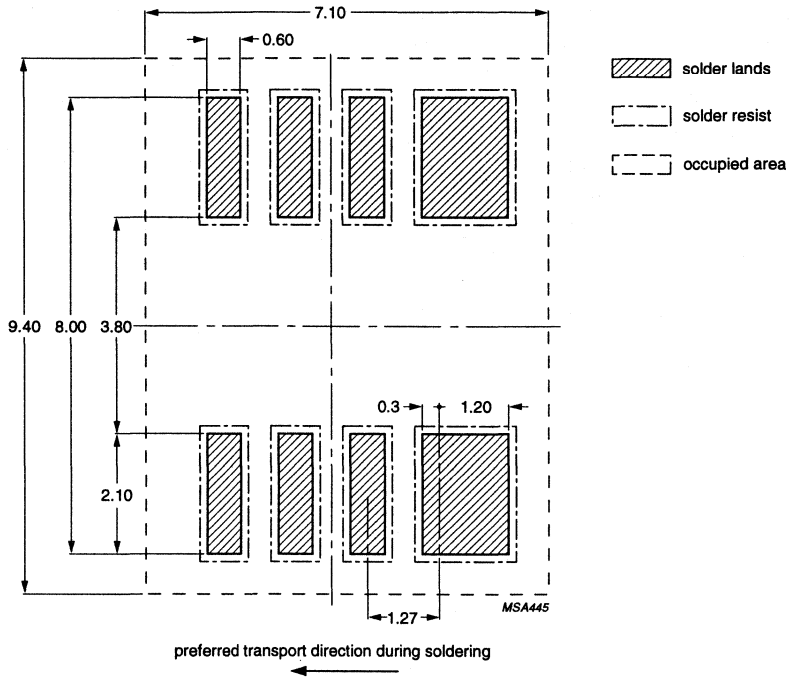
Fig.27 Wave soldering footprint for SOT343; typical dimensions.

SOT96 (SO8) FOOTPRINTS



Dimensions in mm.
Placement accuracy: ±0.25 mm.

Fig.28 Reflow soldering footprint for SOT96 (SO8); typical dimensions.



Dimensions in mm.
Placement accuracy: ±0.25 mm.

Fig.29 Wave soldering footprint for SOT96 (SO8); typical dimensions.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- hand-soldering is time-consuming and therefore expensive.
- the component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it.
- there is a risk of breaking the substrate and internal connections in the component could be damaged.
- the component package could be damaged by the iron.

THERMAL CONSIDERATIONS

Thermal resistance

Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a a printed board, a substrate or heatsink. Referring to Fig.30 (for surface mounted devices mounted on a substrate), heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air where it is dispersed by convection or by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

The elements of thermal resistance shown in Fig.31 are defined as follows:

$R_{th\ j\text{-}mb}$ thermal resistance from junction to mounting base

$R_{th\ j\text{-}c}$ thermal resistance from junction to case

$R_{th\ j\text{-}s}$ thermal resistance from junction to soldering point

$R_{th\ s\text{-}a}$ thermal resistance from soldering point to ambient

$R_{th\ c\text{-}a}$ thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most packages)

$R_{th\ j\text{-}a}$ thermal resistance from junction to ambient.

The temperature at the junction depends on the ability of the package and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\ max} = T_{amb} + P_{tot\ max}\,(R_{th\ j\text{-}s} + R_{th\ s\text{-}a})$$
$$= T_{amb} + P_{tot\ max}\,(R_{th\ j\text{-}a})$$

where:

$T_{j\ max}$ is the maximum junction temperature

T_{amb} is the ambient temperature

$P_{tot\ max}$ is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\ max}$, only T_{amb} and $R_{th\ s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\ s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\ j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\,max}$ and $R_{th\,j\text{-}s}$, or $R_{th\,j\text{-}c}$ or $R_{th\,j\text{-}a}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from

$T_j = T_{case} + P_{tot} \times R_{th\,j\text{-}c}$ or, using the soldering point definition, from $T_j = T_{solder} + P_{tot} \times R_{th\,j\text{-}s}$.

Thermal resistance ($R_{th\,s\text{-}a}$ and $R_{th\,c\text{-}a}$)

The thermal resistance from soldering point to ambient (SMDs), and that from case to ambient depends on the mounting technique, the shape and material of the tracks and substrate. Standard mounting conditions to set the maximum power ratings of the various packages are shown in Figs 32 to 37. Each figure shows single-sided 35 µm copper-clad epoxy fibre-glass print, 1.5 mm thick, the tracks are fully solder-tinned and the shaded areas shown are copper or ceramic (Al_2O_3) 0.7 mm thick.

$R_{th\,s\text{-}a}$ for SMDs mounted on ceramic substrate

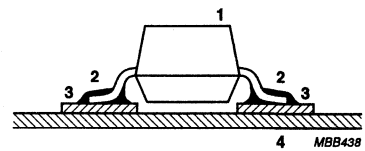
The thermal resistance $R_{th\,s\text{-}a}$ for devices in SOT23, 89, 143 and 223 packages mounted on ceramic substrate is a function of the substrate area as shown in Fig.39.

The thermal resistance $R_{th\,j\text{-}a}$ can then be calculated by:

$R_{th\,j\text{-}a}$ (substrate) = $R_{th\,j\text{-}a}$ (PCB) – $R_{th\,s\text{-}a}$ (PCB) + $R_{th\,s\text{-}a}$ (substrate)

The $R_{th\,s\text{-}a}$ (PCB) is:

SOT23 and SOT143	150 K/W
SOT89	140 K/W
SOT223	a function of pad area as shown in Fig.38.



Heat radiates from the package '1' to ambient.
Heat conducts via leads '2', solder joints '3' to the substrate '4'.

Fig.30 Heat losses.

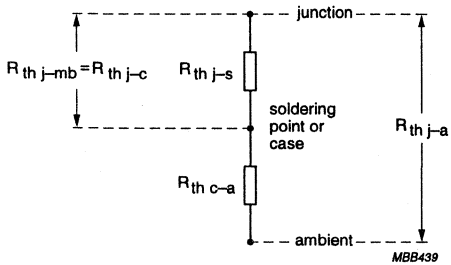
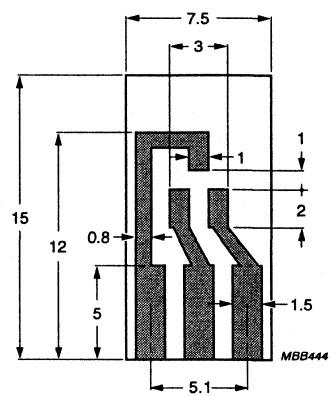
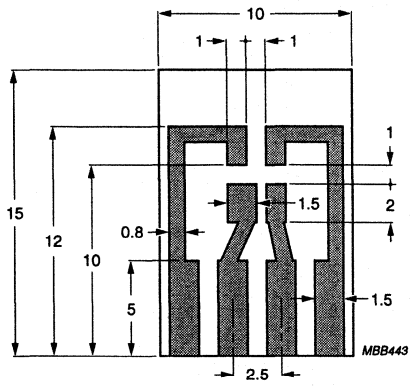


Fig.31 Representation of thermal resistance paths of a device mounted on a substrate or printed board.



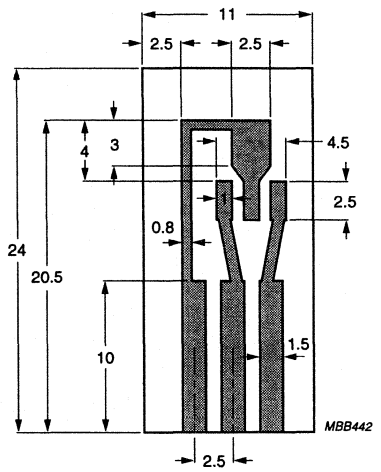
Dimensions in mm.

Fig.32 Standard mounting conditions for SOT23. .



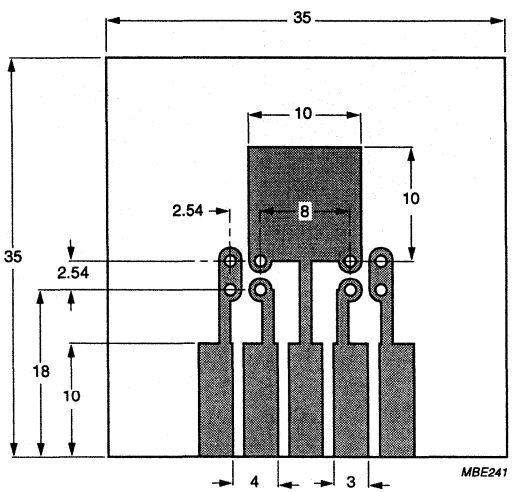
Dimensions in mm.

Fig.33 Standard mounting conditions for SOT143.



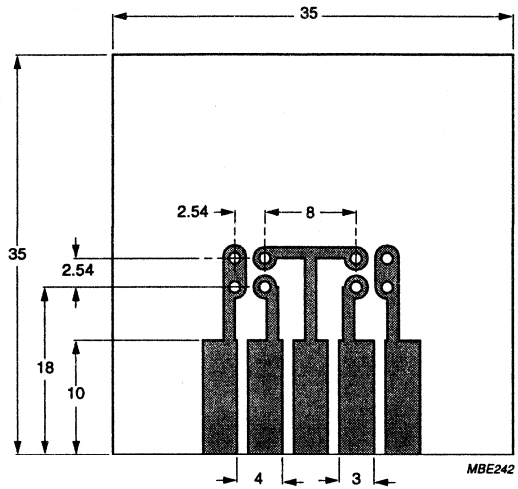
Dimensions in mm.

Fig.34 Standard mounting conditions for SOT89.



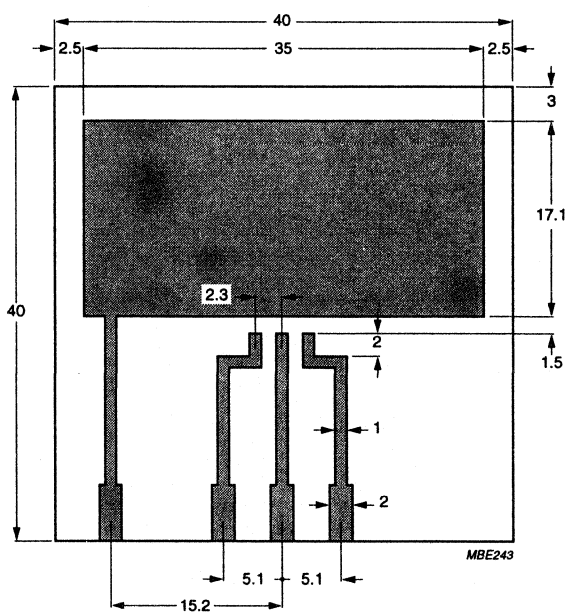
Dimensions in mm.

Fig.35 Standard mounting conditions for SOT54, higher dissipation option.



Dimensions in mm.

Fig.36 Standard mounting conditions for SOT54.



Dimensions in mm.

Fig.37 Standard mounting conditions for SOT223.

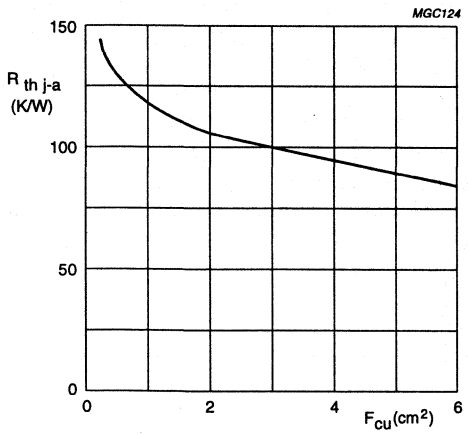


Fig.38 Thermal resistance ($R_{th\ j\text{-}a}$) as a function of FR4 epoxy fibre-glass circuit board.

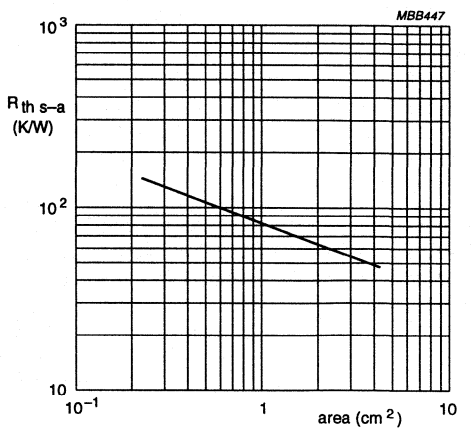


Fig.39 Thermal resistance ($R_{th\ s\text{-}a}$) as a function of area of ceramic substrate.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. Our devices **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 40 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material.

The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

Our devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

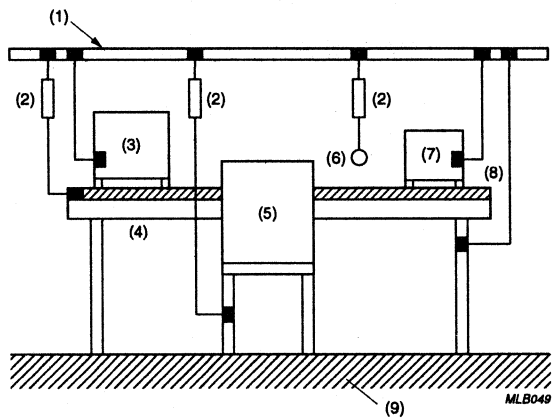
ASSEMBLY

The devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards should be handled in the same way as unmounted devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.40 Protected work station.

IDEAS FOR DESIGN

POWER/BATTERY SWITCHING USING VD-MOS-FETS

A Power switch can be used to disconnect a load during a period of non use. The load may be anything from a light bulb, an electronic valve, a stepper or brush motor to electronic components in a lap top computer that is not in use all the time. There is a choice between a low-side switch (LSS) located between the load and the power supply input, and a high-side switch (HSS), between the load and the power supply return. With an LSS the control is referenced to ground, whilst with an HSS the control is referenced to V_{DD} (see Fig.1). This makes the control for an HSS more complicated than for an LSS, and the design is more expensive and has a higher risk.

For power switching purposes MOS-FETs have some important advantages over bipolar transistors. Firstly they are voltage controlled instead of current controlled, and secondly they have no thermal runaway or secondary breakdown. This is due to the fact that a MOS-FET has a negative temperature coefficient of drain current, while a bipolar transistor has a positive temperature coefficient of collector current. Also the on-resistance of the FET can be reduced simply by connecting two or more in parallel.

Although more expensive, an HSS may perform better during fault conditions. The most probable fault that will occur is a short from the output of the switch to ground. Since most environments are connected to ground, damage to the output wire of the switch may be sufficient for an output short to ground to cause the load to remain active. In the case of an HSS the short will be across the load, thus preventing its activation.

It is often required to control power switches from the output of digital logic. The most common logic families use levels of +2.4 V (TTL) or +5 V (CMOS). Figures 2 to 5 illustrate how to switch loads from these logic levels. In Fig.2 the 2.4 volt gate drive will fully turn on a MOS-FET with a gate-source threshold voltage (VGS_{th}) of less than 1.5 V. However, when using a FET with VGS_{th} of less than 3 V (see Fig.3), a gate pull-up resistor connected to +5 V is necessary to generate a full 5 volt swing from the TTL output. Using CMOS levels makes life easier. Since these levels equal the V+ and V– values, a MOS-FET is simply chosen with a VGS_{th} somewhere between V+ and V–. If the load is returned to ground, a P-channel FET is recommended (see Fig.4), or N-channel (see Fig.5) otherwise.

If the load is inductive, the use of a series gate resistor is recommended, as the drain-gate capacitance of the FET could couple inductive transients of the load back to the delicate logic circuitry.

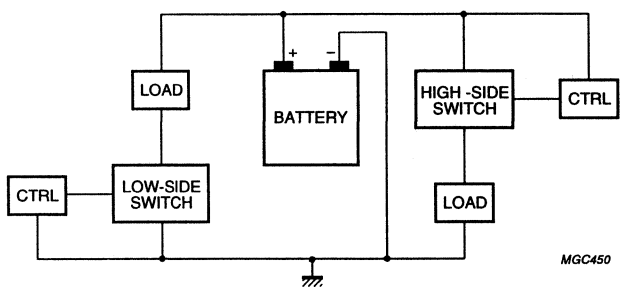


Fig.1 Power/Battery switching using VD-MOS-FETs circuit diagram.

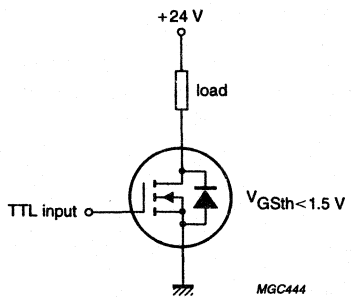


Fig.2 Low threshold N-channel VD-MOS-FET switching with TTL levels.

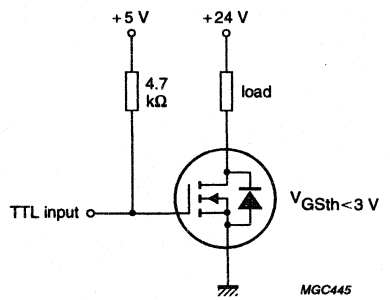


Fig.3 Low threshold N-channel VD-MOS-FET switching with TTL levels using a pull-up resistor.

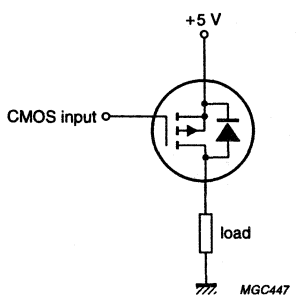


Fig.4 P-channel VD-MOS-FET switching with CMOS levels.

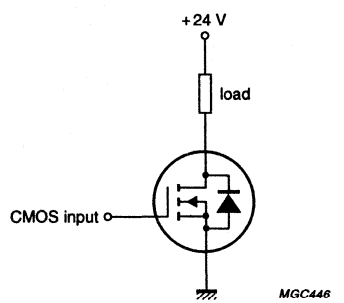


Fig.5 N-channel VD-MOS-FET switching with CMOS levels.

DRIVERS FOR BRUSHLESS DC MOTORS

Brushless DC motors normally have a permanent magnet rotor and a wire-wound stator. They are very efficient and provide rapid acceleration, high speed, and smooth, quiet operation. The current to the stator coils is switched electronically as shown in Fig.6 and the switches are arranged in a bridge configuration to allow current flow in both directions.

In this example, the complementary P and N channel VD-MOS-FETs are shown, but it is also possible to use only N channel switches, depending on the control circuitry. The PHILIPS Integrated Circuit TDA5142T has been chosen as the controller, and three of the PHC21025 MOS-FETs (one 100 mΩ N-channel and one 250 mΩ P-channel type in a SO8 package) as motor drivers. These FETs can drive motors that require currents of up to 4 A (when soldering point temperature of drain pins does not exceed 80 °C) with gate drive coming directly from the IC.

A characteristic of inductive loads (such as stator windings) is the flyback energy that occurs when the drive current through a winding is switched off. This energy needs to be absorbed by the intrinsic source-drain diode of the FET. The flyback current is equal to the motor current, which is at a maximum during acceleration and (active) braking. The flyback power is the product of both this current and the forward voltage drop over the diode, and of the duty cycle which in turn depends on the inductance of the windings. This dissipation is a substantial part of the total dissipation.

We can take a practical example and calculate the power dissipation of the intrinsic diodes during flyback, and the FETs when in the 'on' state.

Assume that we have a motor with 6000 rpm (100 rps) and 6 pole-pairs (600 'electrical' rps). The period time for one 'electrical revolution' is 1.667 ms. In each 'electrical revolution' all of the six FETs are switched, giving a switching frequency of 3600 Hz. A FET is therefore switching once every 278 µs, which is also the maximum time that the diode can be conducting. The FETs themselves are conducting at two periods, 278 µs and 556 µs, which is at a duty factor of 33%. The dissipation per half bridge (per SO8) is: $\{0.33 \times (I_{MOTOR})^2 \times R_{DSonP}\} + \{0.33 \times (I_{MOTOR})^2 \times R_{DSonN}\} + flyback_P + flyback_N$.

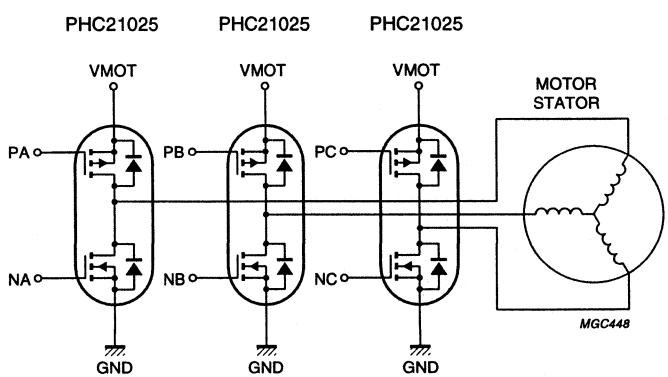


Fig.6 Drivers for brushless DC motors

To calculate the dissipation during flyback for this example, values of 2 Ω for the ohmic resistance of the windings, and 540 μH for the inductance have been assumed. With a 12 V, 1 A motor, SPICE simulations show that the dissipation in the diode during flyback starts at 1.6 W at time zero, decreasing to 0 W after 60 μs. This is repeated every 1.667 ms and gives an average dissipation of 29 mW. The dissipation in the N-channel FET is 33 mW and in the P-channel FET 83 mW. This gives a total dissipation of 174 mW, of which 58 mW (33%) is in the diodes and cannot be neglected.

During acceleration and (active) braking, the motor current is much higher than during normal operation, and a current limiter may be necessary. The circuit design must be based on this higher current, because acceleration may last for up to 10 or 15 seconds, long enough to heat up the FETs. During flyback, not only is the current much higher but it also lasts longer. In the simulation example, if the motor current is increased to 3 A, the flyback will last for 120 μs. The diode forward voltage will also be higher at this current level, and for one SO8 package the total dissipation increased to 1.5 W.

SIREN DRIVER CIRCUIT FOR CAR ALARM

Figure 7 shows a siren driver circuit created with VD-MOS-FETs. Power is supplied by a 12 V battery, and the driver inputs are complementary pulse waveforms from a microprocessor.

Chosen for our example are two BSN20 VD-MOS-FETs in small SOT23 packages and two PHC21025, each comprising two FETs in one SO8 package. In its minimum configuration the circuit requires six components (excluding the speaker) and its maximum configuration is eight components. All components can be surface mounted.

The two push-pull stages X2/X3 and X5/X6 drive the speaker directly. Either X2 and X6 are conducting or X5 and X3, reversing the current through the speaker. Driver stages X1 and X4 convert the 5 V input swing from the microprocessor to the 12 V switching level.

During microprocessor reset and with no alarm, both driver input pins must have the same potential. (0 or 5 V; 0 V is preferred). With the FETs X1 and X4 not conducting, the gates of FETs X2, X3, X5 and X6 will be high, and X2 and X5 will be conducting, resulting in no current through the speaker. When driver inputs are pulsed (complementary), almost the full 12 V is switched over the speaker (a little less due to the on-resistance of the push-pull FETs 100 mΩ N-channel and 250 mΩ P-channel).

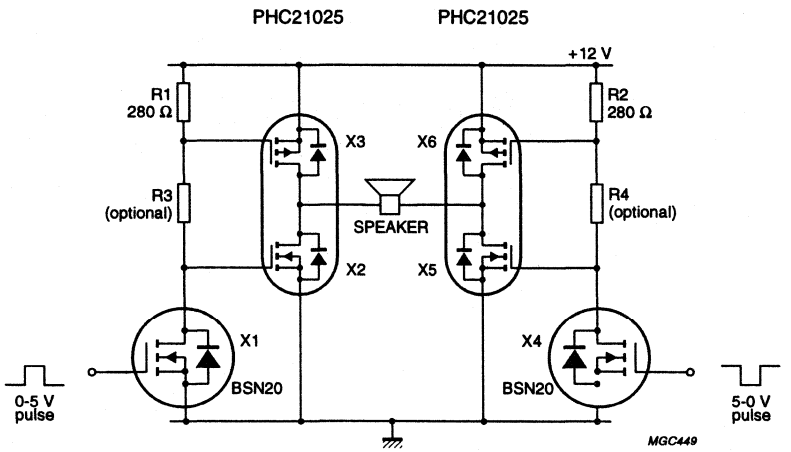


Fig.7 Siren driver circuit for car alarm.

When designing this siren driver circuit, take the following into account. The BSN20 (X1 and X4) have an input threshold between 0.4 and 1.8 V. The value of the pull-up resistors R1 + R3 and R2 + R4 must be as small as possible (but not less than 280 Ω) to achieve the highest possible switching speed, and to guarantee a voltage level at the gates of X2 and X5 less than 0.8 V. R3 and R4 are optional, but may be necessary to reduce high through-current in the push-pull stages. When using these resistors however, the gate voltage at X3 and X6 will not fully reduce to 0.8 V, which can influence the on-resistance of these FETs and consequently the dissipation when conducting. When using R3 and R4, the values of R1 and R2 need to be adjusted to maintain the 280 Ω.

Concerning the dissipation in the push-pull stage, the on-resistance of the FETs increases by a factor of 1.7 when operating at 150 °C junction temperature. For the P-channel, which dissipates the most, this means that the on-resistance increases to 425 mΩ. If a 4 Ω speaker is used, the maximum current will be 2.6 A at 12 V. If the pulse is symmetrical and the duty cycle is 50%, the dissipation in the P-channel FET will be 1.45 W. Note that the temperature at the soldering point of the drain pins must not exceed 99 °C.

PRINTED CIRCUIT-BOARD HEATSINK AREA FOR SURFACE MOUNT PACKAGES

When using surface mount components, it is not as easy to dissipate heat in clip-on or bolt-on heatsinks than with through-hole components. With surface mount components, the conductive tracks or pads on the printed-circuit board are often the only means to transfer heat away from the component.

The amount of heat sink area required for the BSP100 type in a SOT223 package can be calculated as follows. This type has been selected as an example for a design that uses a 100 mΩ, N-channel VD-MOS-FET with an I_{DS} of 3 A. The maximum operating junction temperature of this device is 150 °C. At this temperature, the on-resistance of the FET increases with a factor of 1.7 and the power dissipation in continuous use (duty factor 100%) is 1.53 W.

If the ambient temperature is 40 °C, then the total thermal resistance (R_{th}) requirement for FET and PCB) is: (150 – 40)/1.53 = 72 K/W. The thermal resistance of the FET itself is 10 K/W from junction to the soldering point of the drain tab. Therefore the requirement for Rth of the heatsink is 72 – 10 = 62 K/W.

Figure 8 shows typical thermal resistance from soldering point to ambient as a function of area of an epoxy printed-circuit board. The drain tab of the SOT223 is soldered in the centre of one of the sides (as shown in Fig.9). In this example curve (1) shows a single-sided and unplated copper pad area of 20 × 20 mm.

A similar calculation can be applied to the SO8 package. Using the PHN210 as an example, we have two 100 mΩ, N-channel VD-MOS-FETs in one SO8 package. Taking I_{DS} = 2 A per FET and duty factor = 50%, the dissipation per FET is 0.34 W and the total for both FETs is 0.68 W. If the ambient temperature is 60 °C, then the total thermal resistance (R_{th}) requirement for FET and PCB is: (150 – 60)/0.68 = 132 K/W. For the SO8 package the R_{th} from junction to the soldering point of the drain tab is 35 K/W, so the requirement for the heat sink thermal resistance is 163 – 35 = 128 K/W. Referring again to curve (1) in Fig.8, it can be seen that 50 mm² is required.

This example is true for both FETs dissipating equal power. A suggested PCB design is shown in Fig.10. Here the copper is divided into two 3.5 × 7 mm rectangular portions which gives the required total heatsink area and keeps the drain connections separated.

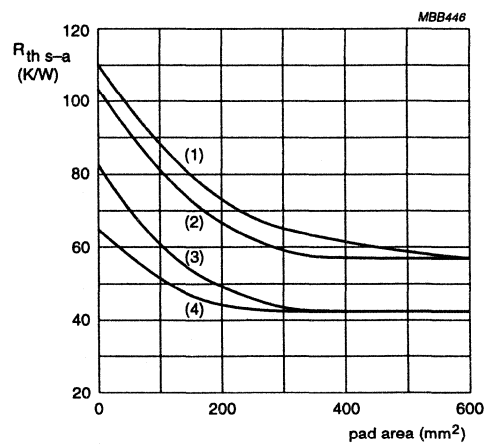


Fig.8 Thermal resistance as a function of pad area of an epoxy printed-circuit board, for square, horizontal PCB copper, no airflow.

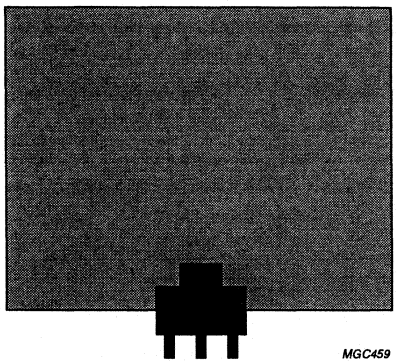


Fig.9 PCB heatsink area for SOT223 package.

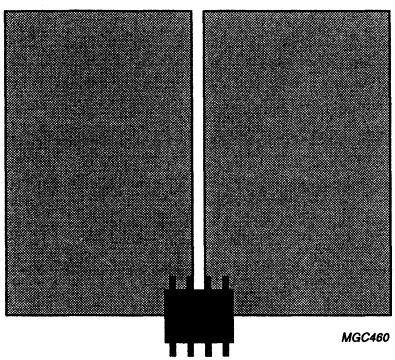


Fig.10 PCB heatsink area for SO8 package.

JFET CONSTANT-CURRENT SOURCES

The simplest JFET current source is shown in Fig.11. The JFET has been selected rather than a MOS-FET because it does not require gate bias (depletion mode). The current will be reasonably constant for a V_{DS} larger than several volts. However, because of I_{DSS} spread, the current is unpredictable. This can be seen, for example, with the 2N5484 which has a specified I_{DSS} of 1 to 5 mA. The circuit is attractive because of its simplicity. (Current regulator diodes are JFETs with the gate tied to the source, sorted according to current).

With a small variation this circuit gives an adjustable current source (see Fig.12). Resistor R back-biases the gate by $V = I_D \times R$, thus reducing I_D. The value of R can be calculated from the I_D/V_D characteristic for that particular JFET. This circuit makes it possible to set the current (must be less than I_{DSS}) as well as to make this current more predictable.

A JFET current source always shows some variation of output current with output voltage because of its finite output impedance, even if built with source resistor.

An improvement can be made by using a second JFET to hold the drain-source voltage of the current source constant (see Fig.13). The JFET Q2 has a larger I_{DSS} and is connected in series with the current source. It passes the (constant) drain current from Q1 through to the load, whilst holding the drain at Q1 at a fixed voltage; namely the gate-source voltage that makes Q2 operate at the same current as Q1. Q2 therefore shields Q1 from voltage swings at its output, and since Q1 is not subject to drain voltage variations, it provides constant current.

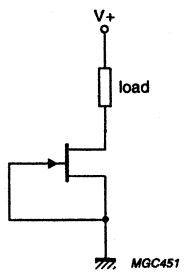


Fig.11 Simple JFET current source.

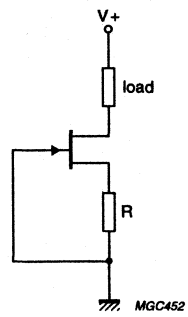


Fig.12 Adjustable JFET current source.

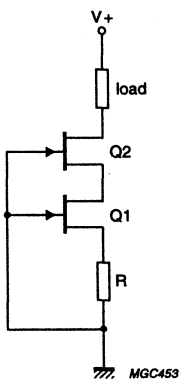


Fig.13 Adjustable JFET current source with high output impedance.

JFET SOURCE FOLLOWERS AND AMPLIFIERS

There are normally three major considerations to be taken into account when designing amplifiers: voltage gain, distortion and noise, and the importance of each of these depends on the application. This is also true for the type of circuit configuration used. There are three basic circuit configurations for JFETs:

- Common source configuration (CSC)
- Common gate configuration (CGC)
- Common drain configuration (CDC).

The choice of circuit configuration depends on the design requirements with respect to:

- Input impedance (high in CSC and CDC)
- Impedance matching to signal source and load
- Distortion (lowest in CGC).

Common-drain amplifiers, or source followers, and common-source amplifiers are analogous to emitter followers and common-emitter amplifiers in bipolar transistors. However, the absence of DC gate current makes it possible to realize very high input impedances. Such amplifiers are essential when dealing with the high-impedance signal sources encountered in measurement and instrumentation.

It is convenient to use a self-biasing scheme with a single gate-biasing resistor to ground.

Figure 14 shows a source follower, Fig.15 a common-source amplifier. The gate-biasing resistor can be quite large (at least 1 MΩ), because the gate leakage current is in the order of nA.

Matched FETs can be used to construct high input impedance front-end stages for bipolar differential amplifiers, op-amps and comparators.

There are many applications in which the signal source impedance is intrinsically high, e.g. capacitor microphones, pH probes, charged particle detectors, or microelectrode signals in biology and medicine. In these cases a FET input stage is ideal.

Within some circuits there are situations where the following stage must draw little or no current. Common examples are analog 'sample and hold' and 'peak detector' circuits, in which the level is stored in a capacitor and will 'droop' if the next amplifier draws significant input current. In all these applications the negligible input current of a FET is an important feature.

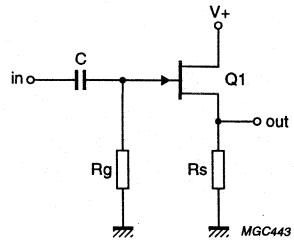


Fig.14 JFET source follower circuit.

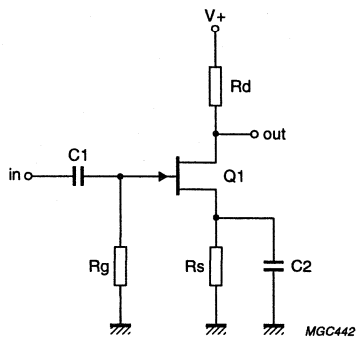


Fig.15 Common-source amplifier circuit.

JFET VOLTAGE CONTROLLED RESISTORS

Under certain biasing conditions, the on-resistance of the JFET is a function of the gate source voltage alone, so that the JFET will behave as an almost pure ohmic resistor.

Figure 16 shows the output characteristics of a 2N4416 for relatively small positive and negative values of V_{DS} in the linear or triode region, where $V_{DS} < V_{GS} - V_{GSth}$. It can be seen that all characteristics pass through the origin (no offset) and are symmetrical and relatively linear. This means that the JFET can be used as a variable resistance in voltage controlled attenuators, analog multipliers, amplitude modulators, bandwidth controlled filters, automatic gain control circuits, and so on.

The channel resistance in the linear region is the inverse of the transconductance in the saturated region: $R_{DS} = 1/g_m$ at a given V_{GS}.

In the first quadrant, the boundaries are set by $V_{GS} = 0$ and $V_{GD} = -V_{GSth}$, in the third quadrant by $V_{GS} = -V_{GSth}$ and $V_{GD} = 0$.

In the first quadrant, as V_{DS} increases towards $V_{DSsat} = V_{GS} - V_{GSth}$, the value of R_{DSon} changes, causing distortion in voltage-controlled-resistor circuits. The same thing happens in the third quadrant, as the negative drain voltage exceeds the negative gate voltage and causes the gate-channel diode to start conducting.

This signal distortion must be as low as possible, while at the same time a large signal handling capability is desirable. The linearity can be improved by means of feedback from the drain to the gate (see Fig.17).

Now, part of the drain signal is applied to the gate. In the case of a positive V_{DS} signal, this reduces the gate voltage, increasing the drain current and pushing the bias line into the more linear part of the operating region.

When V_{DS} is negative, V_{GS} will go more negative, causing a reduction in drain current. This reduces the conduction of the gate channel diode, resulting in a more linear bias line.

The value of R1 and R2 should be equal, to maintain symmetry between the first and third quadrants.

Feedback is essential for a reasonably linear characteristic, and high values of I_{DSS} and V_{GSth} are preferred.

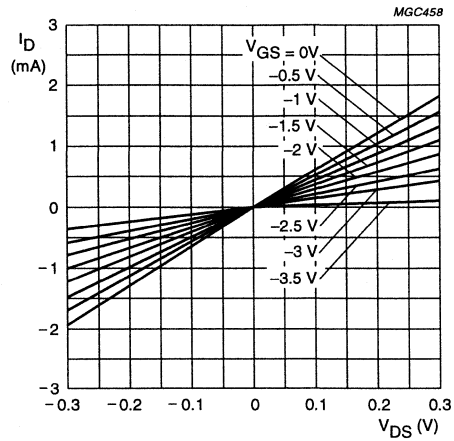


Fig.16 Output characteristics; 2N4416.

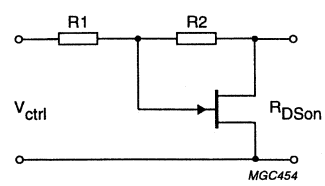


Fig.17 JFET voltage controlled resistor.

MOS-FET ANALOG SWITCHES

The combination of low on-resistance, extremely high off-resistance, low leakage current and low capacitance, makes FETs, particularly lateral MOS-FETs, ideal as voltage-controlled switching elements for analog signals.

Like mechanical switches, the FET switch is a bi-directional device; signals can go either way through it.

The circuit as shown in Fig.18 will switch signals in the −10 to +10 V range if the gate has been driven from −15 V (off) to +15 V (on); the body (back-gate) should then be tied to −15 V.

With any FET switch it is important to provide a load resistance in the 1 to 100 kΩ range in order to reduce capacitive feed-through of the input signal, that would otherwise occur during the off-state. If it is necessary to switch signals that may nearly reach the supply voltages, the simple N-channel switch shown in Fig.18 will not work, since the gate is not forward biased at the peak of the signal swing.

The solution is to use paralleled complementary MOS-FET switches (Fig.19). In this case the gate-drive is somewhat more complicated, since the N-channel FET needs to be positive biased with respect to the back-gate and the P-channel negative biased. This switch is also bidirectional; either terminal can be the input.

A useful application of FET analog switches is the 'multiplexer', a circuit that allows you to select any of several inputs, as specified by a control signal. The analog signal present on the selected input will be passed through to the output.

Because analog switches are bidirectional, an analog multiplexer is also a 'demultiplexer'; a signal can be fed into the output and will appear on the selected input.

Voltage-controlled analog switches form essential building blocks for op-amps, integrators, sample-and-hold circuits and peak detectors.

Another application is in switchable RC low-pass filters. A multiplexer is used to select one out of a series of resistors, or independent switches are used to select one or more resistors in parallel.

As stated before, a load resistor is necessary to reduce capacitive feed-through (cross-talk).

If a switch that has really low cross-talk performance is needed, the circuit shown in Fig.20 could be used. When switches Q1 and Q2 are off, Q3 is on and will prevent any capacitive feed-through.

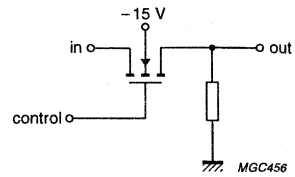


Fig.18 MOS-FET analog switch.

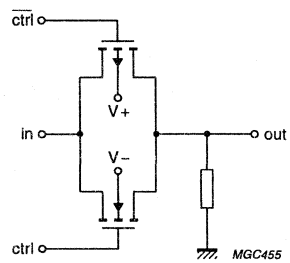


Fig.19 Paralleled complementary MOS-FET switches.

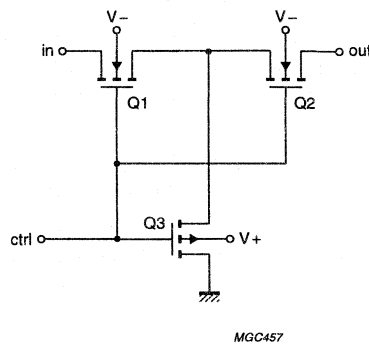


Fig.20 MOS-FET analog switch with low cross talk performance.

DEVICE DATA

in alphanumeric sequence

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

QUICK REFERENCE DATA

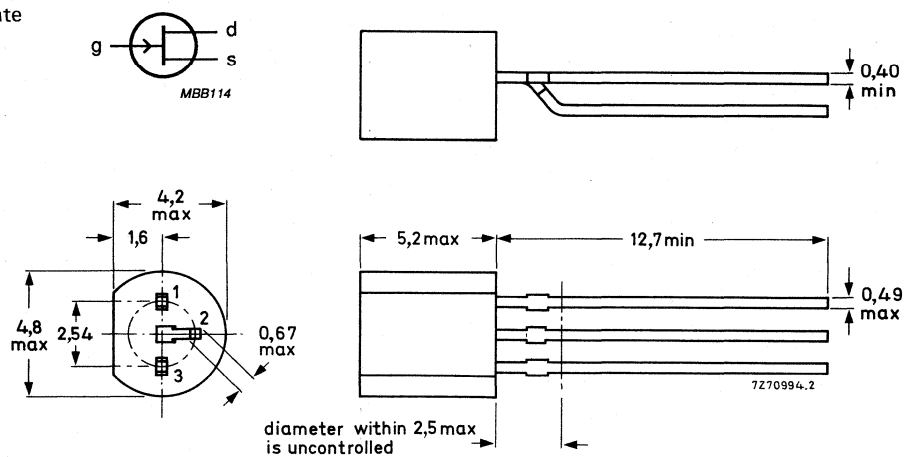
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 °C
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 12 mA
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|Y_{fs}\|$	typ.	3,5 mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 1 kHz; R_G = 1 MΩ	F	<	2 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to +150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BC264A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	5	5	5	5	nA
Drain current							
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
		<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage							
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage							
I_D = 200 µA ; V_{DS} = 15 V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
I_D = 1,0 mA; V_{DS} = 15 V	$-V_{GS}$	>	0,2	–	–	–	V
		<	1,2	–	–	–	V
I_D = 1,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	0,4	–	–	V
		<	–	1,4	–	–	V
I_D = 2,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	0,5	–	V
		<	–	–	1,5	–	V
I_D = 3,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	–	0,6	V
		<	–	–	–	1,6	V
Gate-source cut-off voltage							
I_D = 10 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz							
Transfer admittance	$\lvert y_{fs} \rvert$	>	2,5	3,0	3,5	4,0	mS

V_{DS} = 15 V; $-V_{GS}$ = 1 V; f = 1 MHz				
Input capacitance	C_{is}	typ.	4.0	pF
Feedback capacitance	C_{rs}	typ.	1,2	pF
Output capacitance	C_{os}	typ.	1,6	pF
Noise figure at f = 1 kHz; R_G = 1 MΩ				
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C	F	typ.	0,5	dB
		<	2	dB
Equivalent noise voltage at T_{amb} = 25 °C				
V_{DS} = 15 V; V_{GS} = 0; f = 10 Hz	$V_n / \sqrt{B}$	typ.	40	$nV/\sqrt{Hz}$

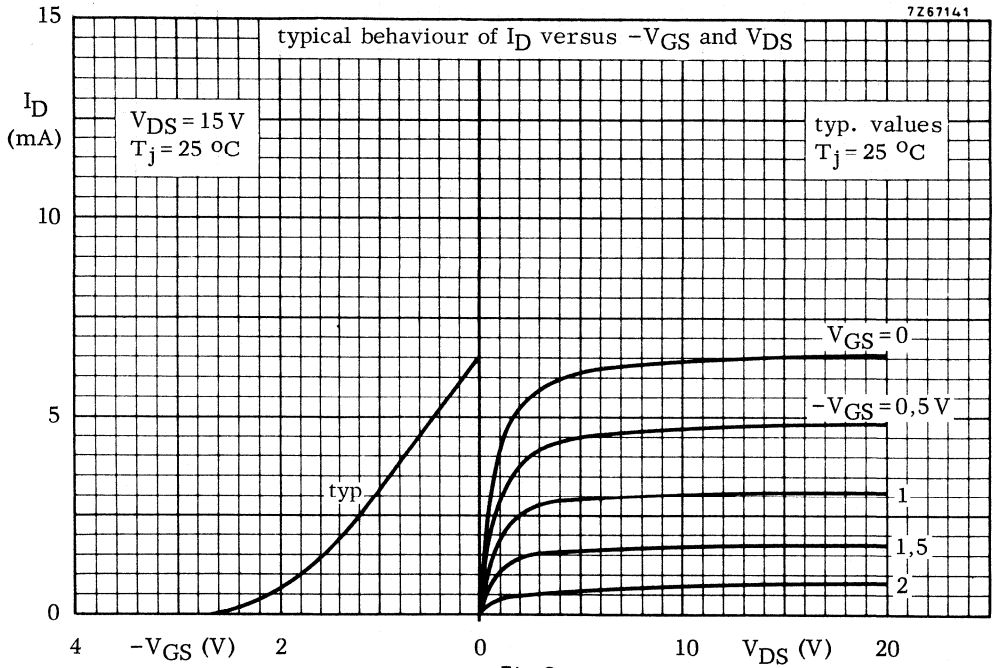


Fig. 2

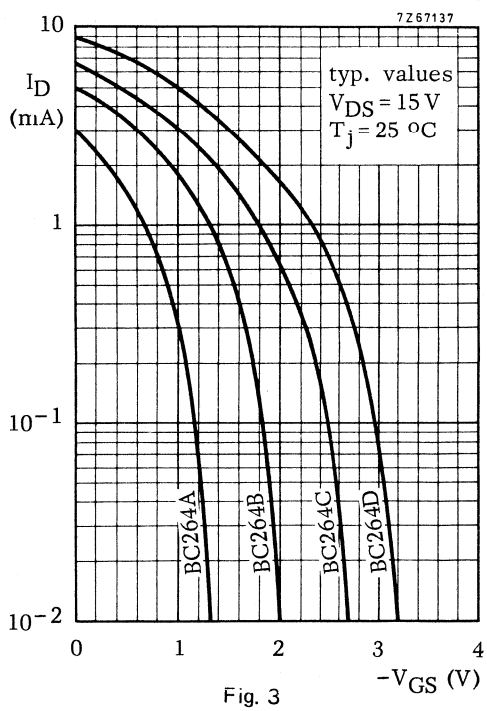


Fig. 3

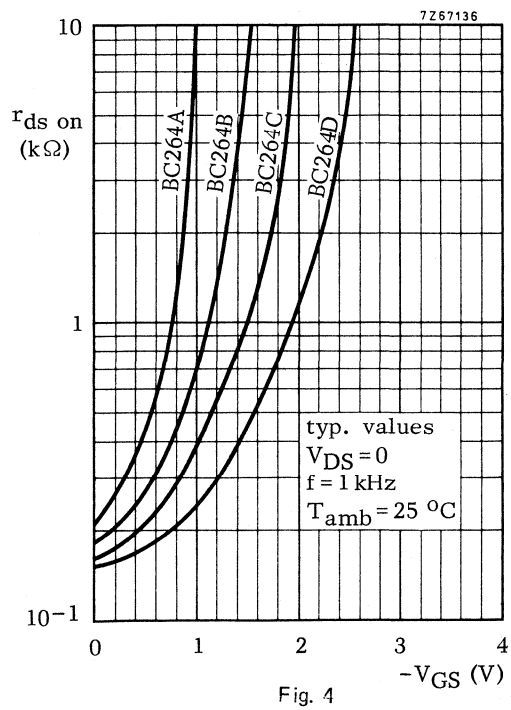


Fig. 4

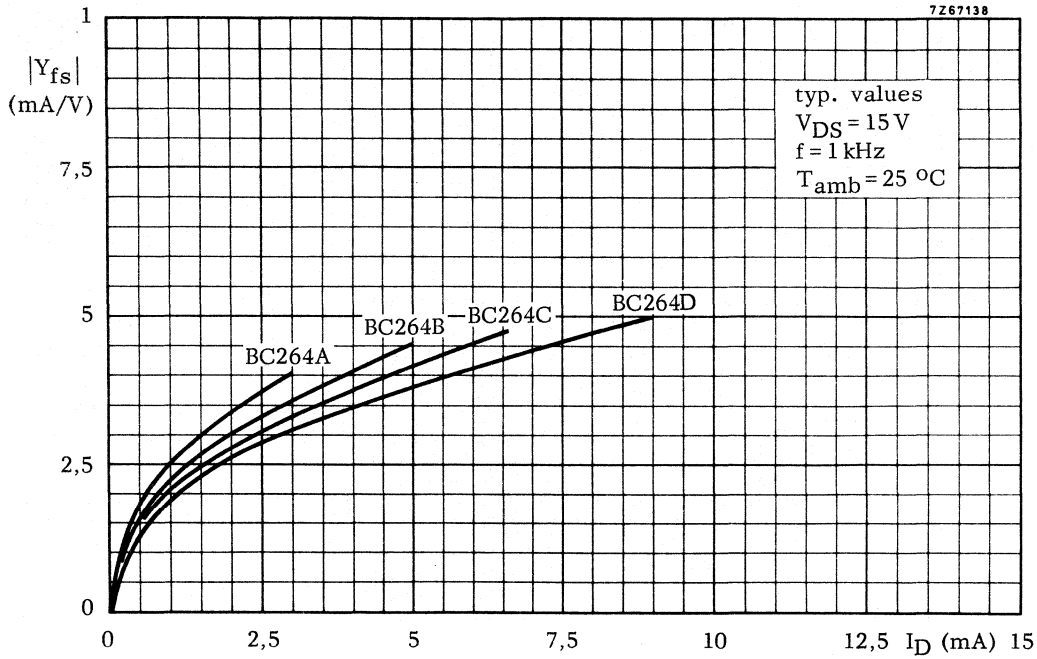


Fig. 5

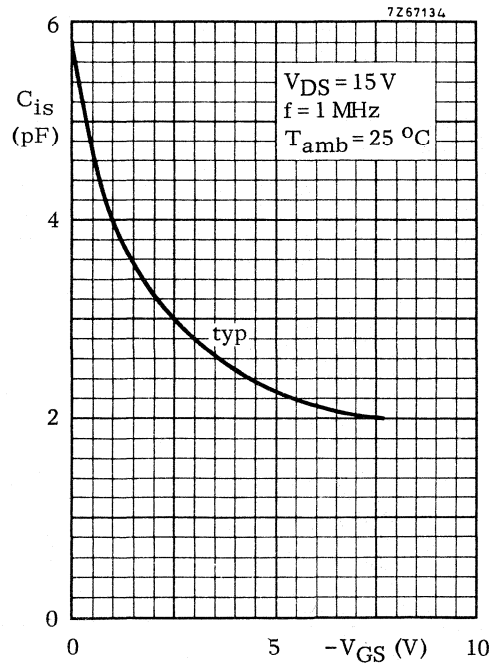


Fig. 6

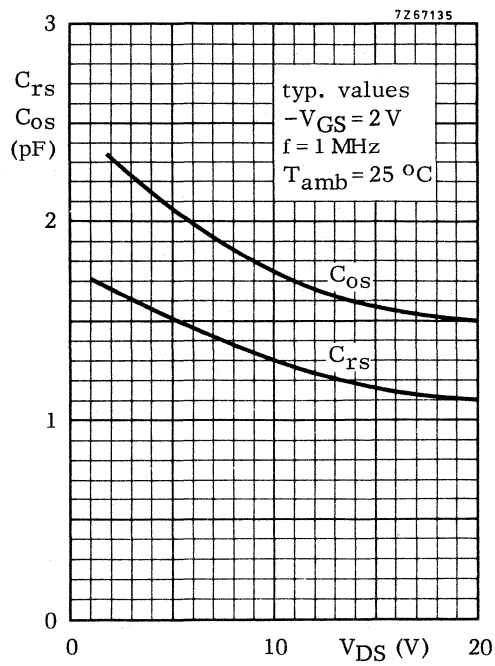


Fig. 7

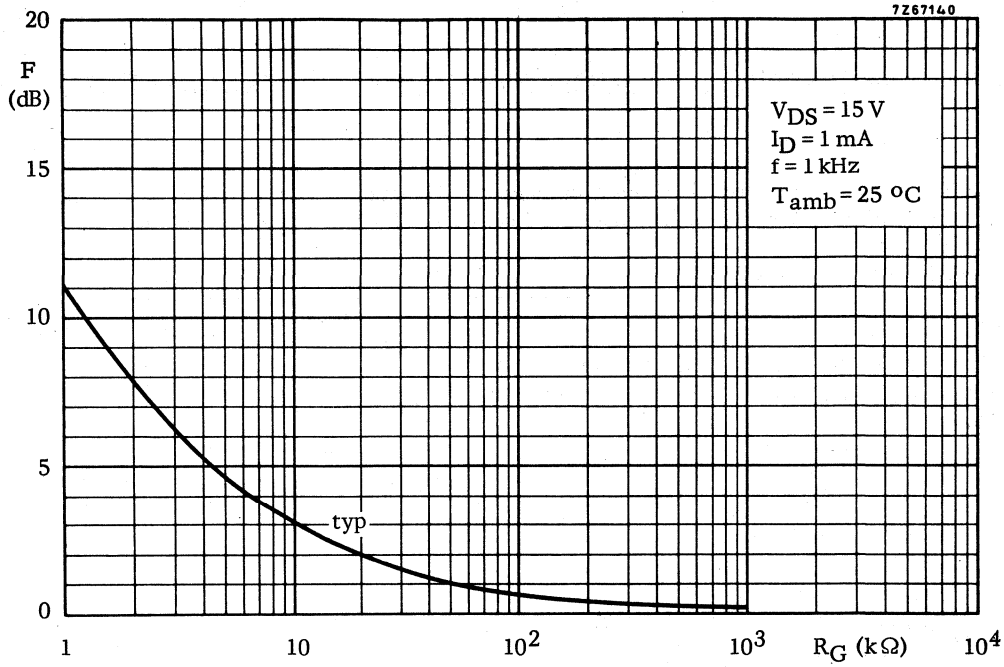

7Z67140
20
F
(dB)
15
10
5
0
typ
V_{DS} = 15 V
I_D = 1 mA
f = 1 kHz
T_{amb} = 25 °C
1
10
10^2
10^3
R_G (kΩ)
10^4

Fig. 8

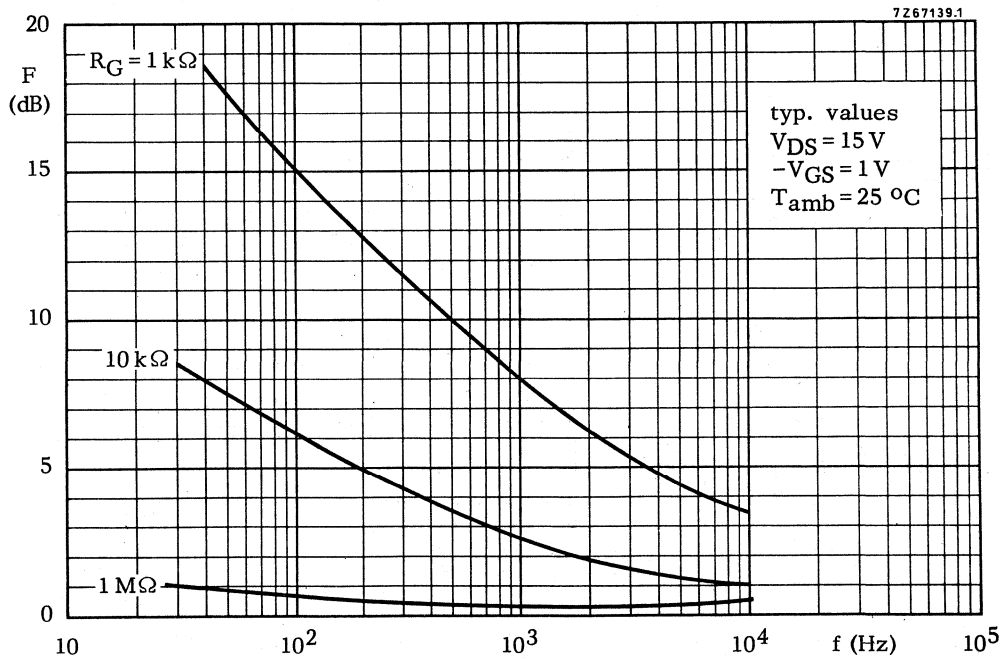

7Z67139.1
20
F
(dB)
15
10
5
0
R_G = 1 kΩ
10 kΩ
1 MΩ
typ. values
V_{DS} = 15 V
$-V_{GS}$ = 1 V
T_{amb} = 25 °C
10
10^2
10^3
10^4
f (Hz)
10^5

Fig. 9

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

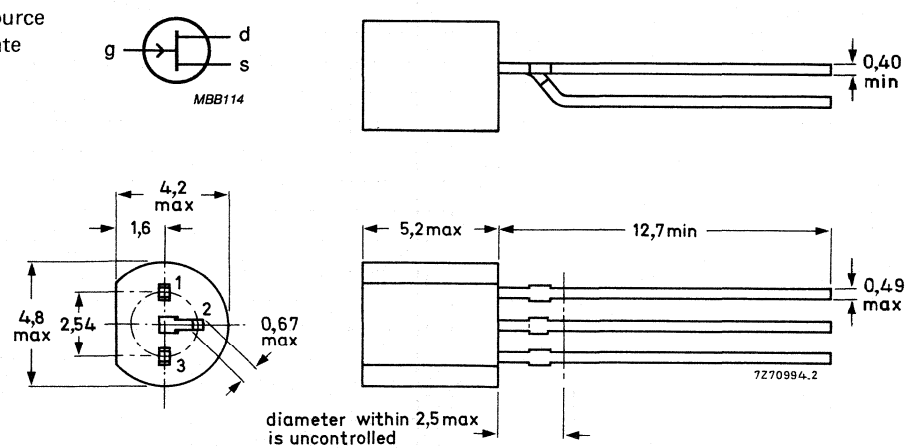
Drain-source voltage	$\pm V_{DS}$			max. 30		V
Gate-source voltage (open drain)	$-V_{GSO}$			max. 30		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}			max. 300		mW
		BF245A/0	A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 0,5	2,0	6	12	mA
		< 2,1	6,5	15	25	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0,25 to 8,0		V
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}			typ. 1,1		pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\|y_{fs}\|$			3,0 to 6,5		mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

		BF245A	B	C
Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	< 5	5	5 nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	< 0,5	0,5	0,5 μA
Drain current 2)				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 2	6,0	12 mA
		< 6,5	15,0	25 mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	> 30	30	30 V
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	> 0,4	1,6	3,2 V
		< 2,2	3,8	7,5 V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

Gate-source cut-off voltage					
I_D = 10 nA; V_{DS} = 15 V		$-V_{(P)GS}$	0,25 to 8,0		V
y-parameters at T_{amb} = 25 °C (common source)					
V_{DS} = 15 V; V_{GS} = 0					
f = 1 kHz	Transfer admittance	$\|y_{fs}\|$	3,0 to 6,5		mS
	Output admittance	$\|y_{os}\|$	typ.	25	μS
f = 200 MHz	Input conductance	g_{is}	typ.	250	μS
	Reverse transfer admittance	$\|y_{rs}\|$	typ.	1,4	mS
	Transfer admittance	$\|y_{fs}\|$	typ.	6	mS
	Output conductance	g_{os}	typ.	40	μS
V_{DS} = 20 V; $-V_{GS}$ = 1 V					
f = 1 MHz	Input capacitance	C_{is}	typ.	4,0	pF
	Feedback capacitance	C_{rs}	typ.	1,1	pF
	Output capacitance	C_{os}	typ.	1,6	pF
Cut-off frequency *					
V_{DS} = 15 V; V_{GS} = 0		f_{gfs}	typ.	700	MHz
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise		F	typ.	1,5	dB

* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

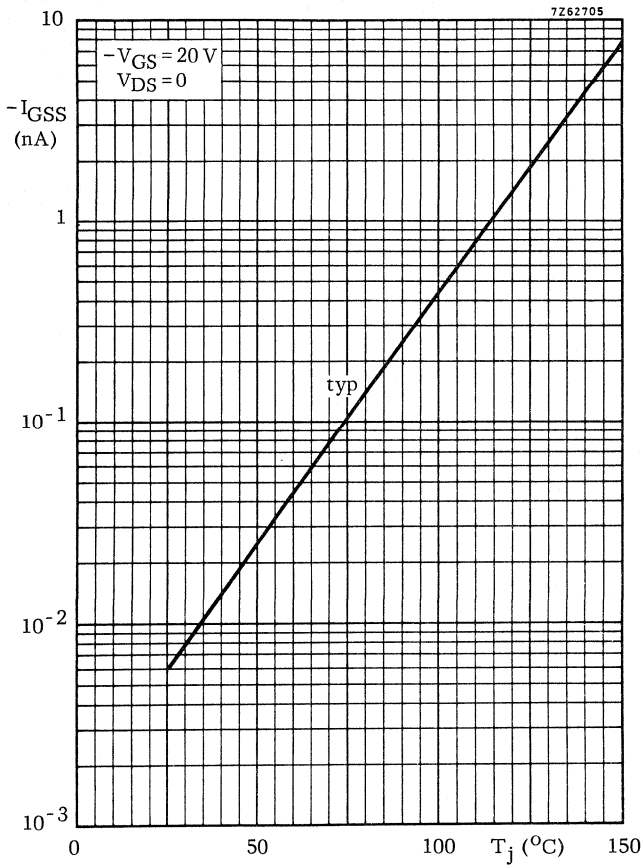

7Z62705
10
$-V_{GS} = 20\ V$
$V_{DS} = 0$
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (°C)
150

Fig. 2

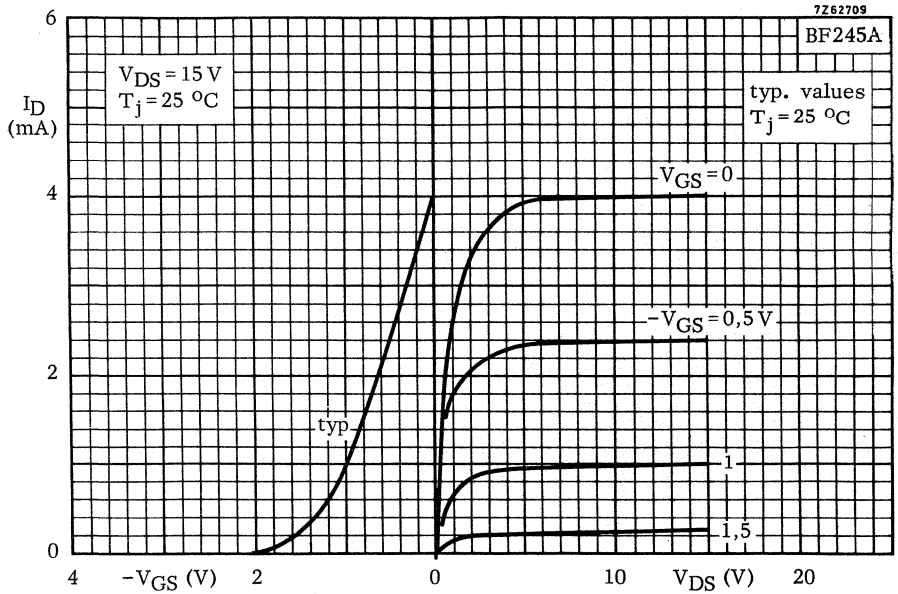

7Z62709
BF245A
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
typ.
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

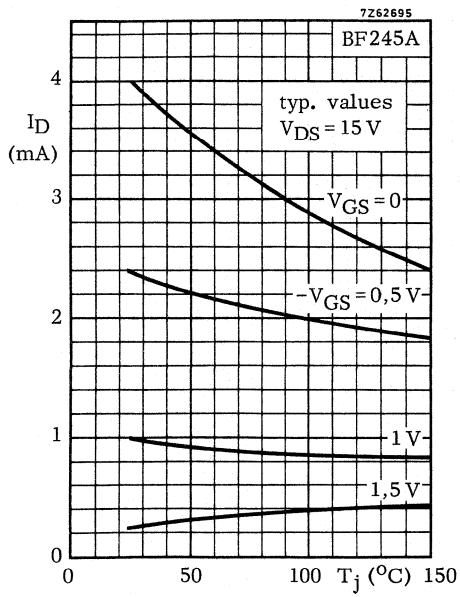

7Z62695
BF245A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
4
3
2
1
0
0
50
100
T_j (°C)
150

Fig. 4

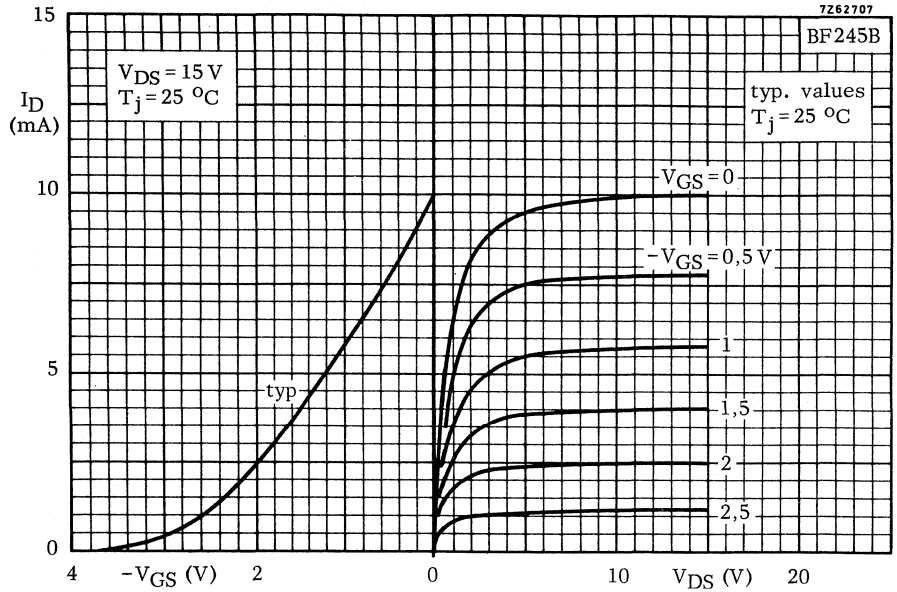

7Z62707
BF245B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
2,5
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

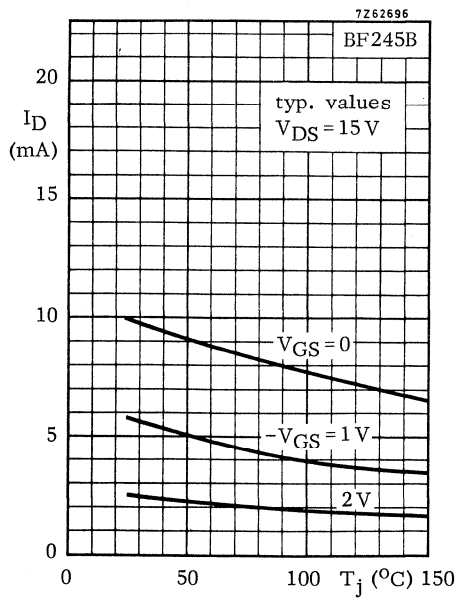

7Z62696
BF245B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

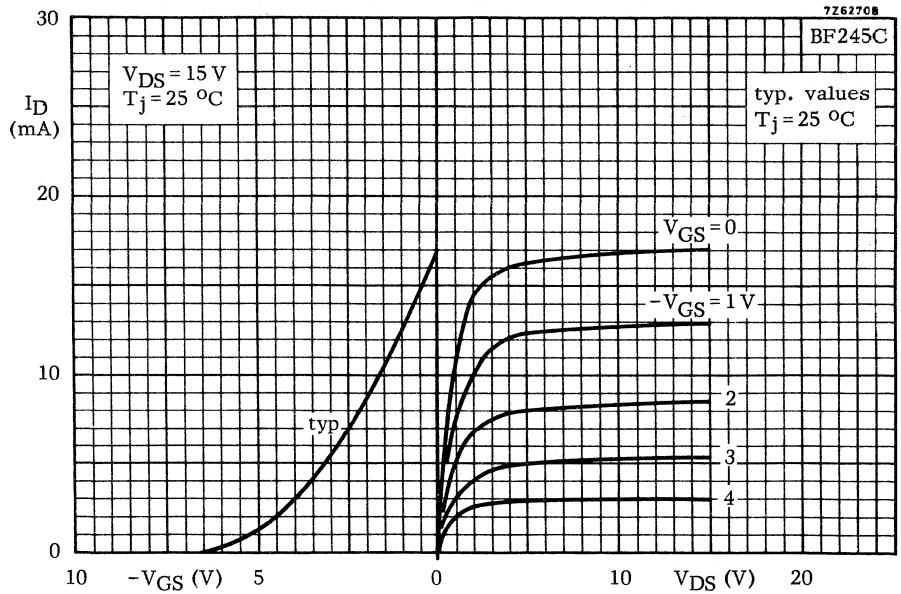

7Z62708
BF245C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
30
20
10
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2
3
4
typ
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

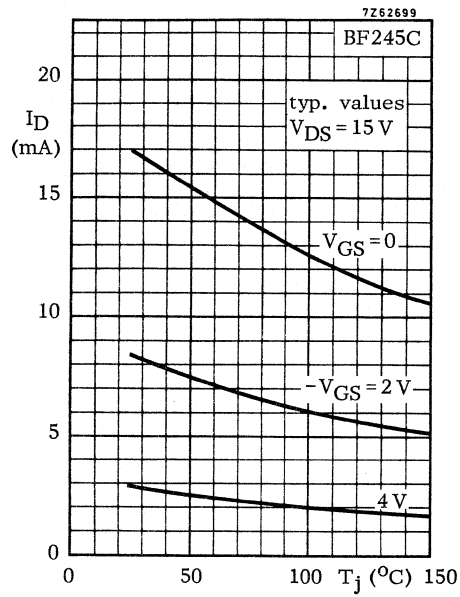

7Z62699
BF245C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100
T_j (°C)
150

Fig. 8

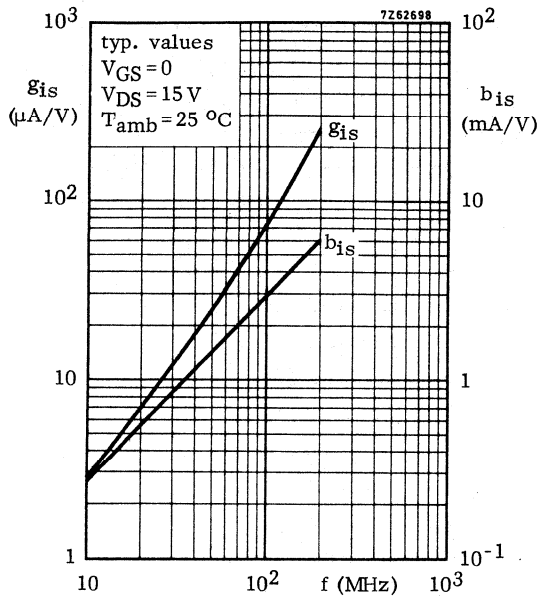

7Z62698
typ. values
$V_{GS} = 0$
$V_{DS} = 15\ V$
$T_{amb} = 25\ ^{o}C$
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

Fig. 9

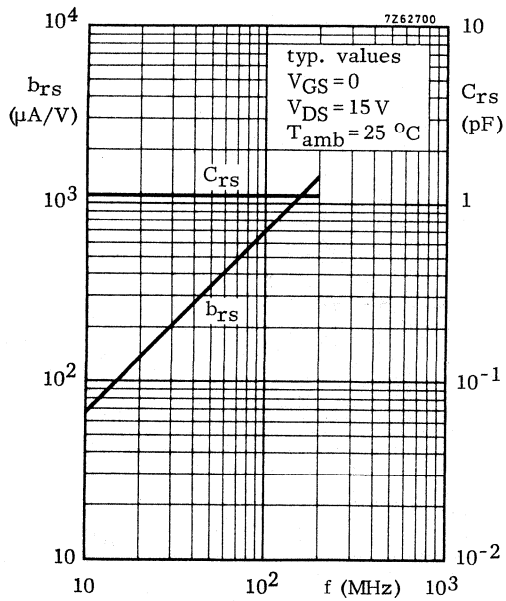

7Z62700
typ. values
$V_{GS} = 0$
$V_{DS} = 15\ V$
$T_{amb} = 25\ ^{o}C$
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

Fig. 10

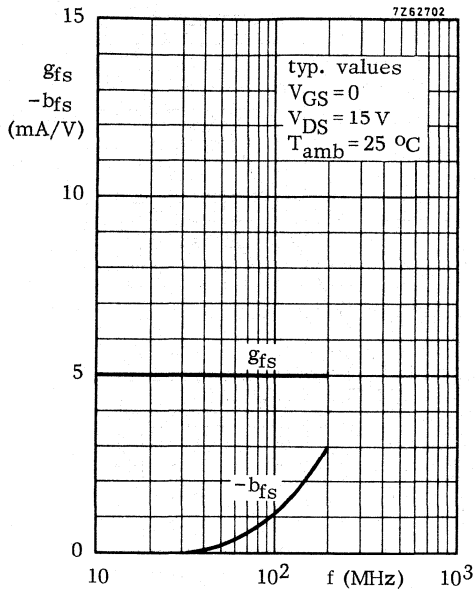

7Z62702
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

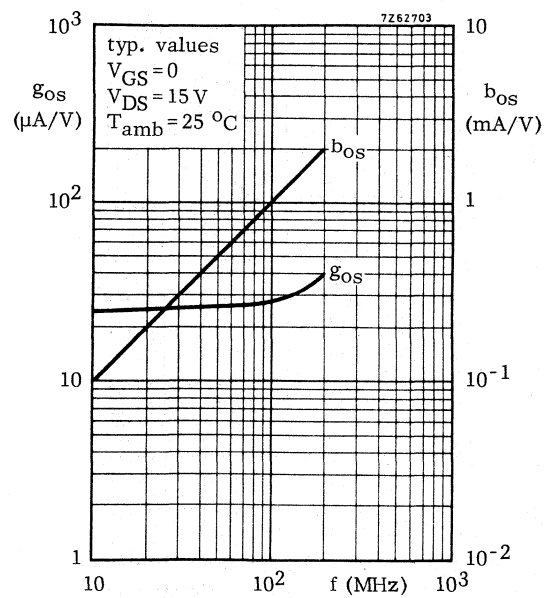

7Z62703
10^3
g_{os}
(μA/V)
10^2
10
1
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{os}
g_{os}
10
b_{os}
(mA/V)
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

Fig. 12

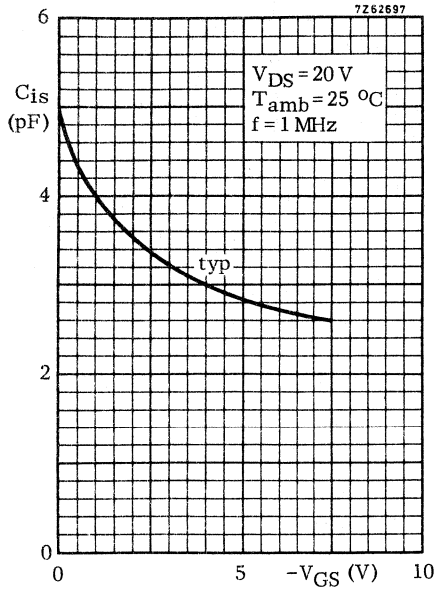


Fig. 13

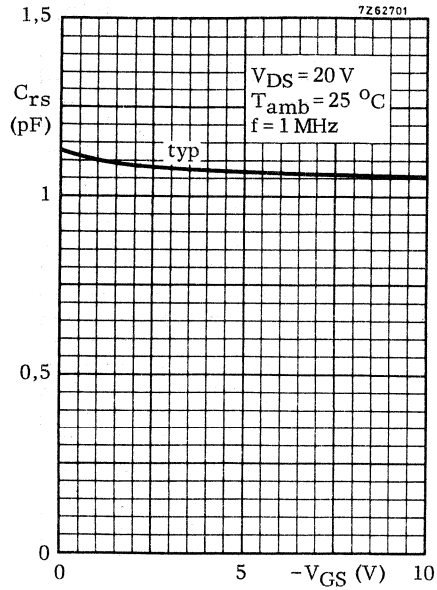


Fig. 14

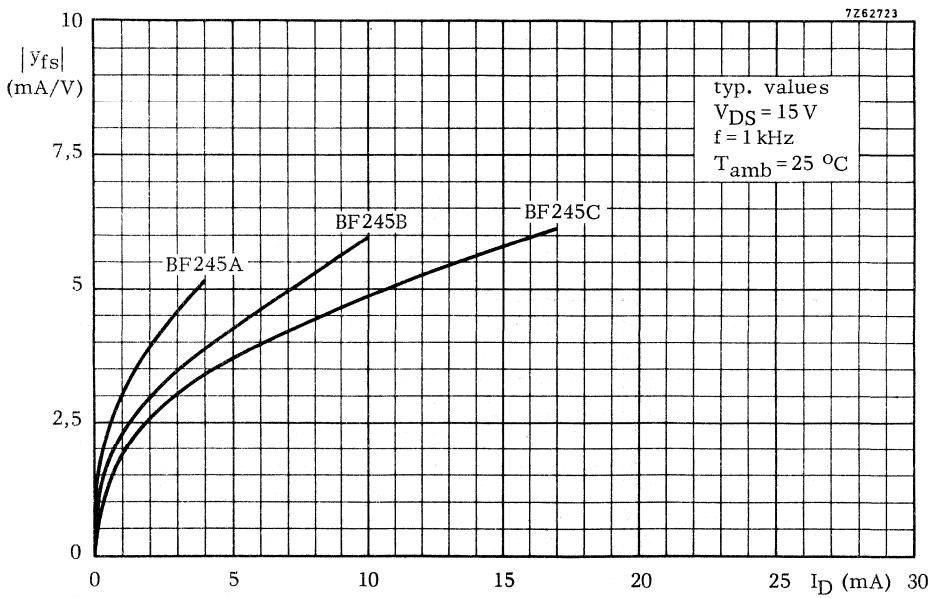


Fig. 15

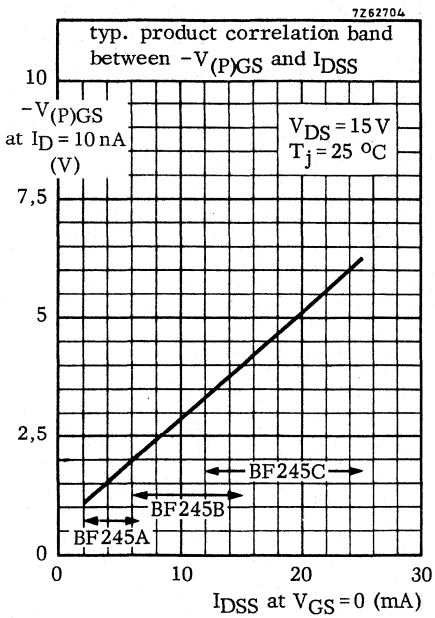


Fig. 16

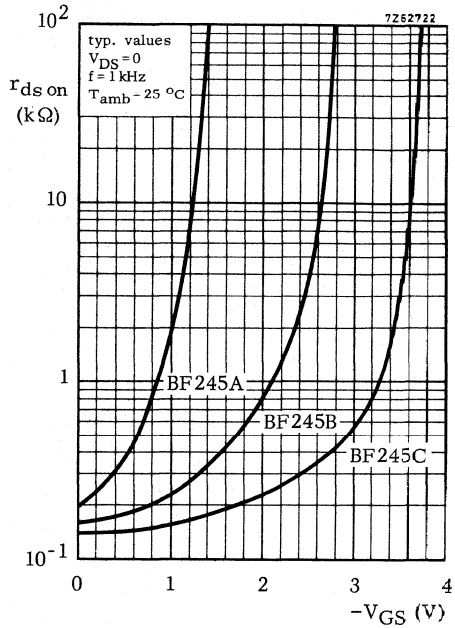


Fig. 17

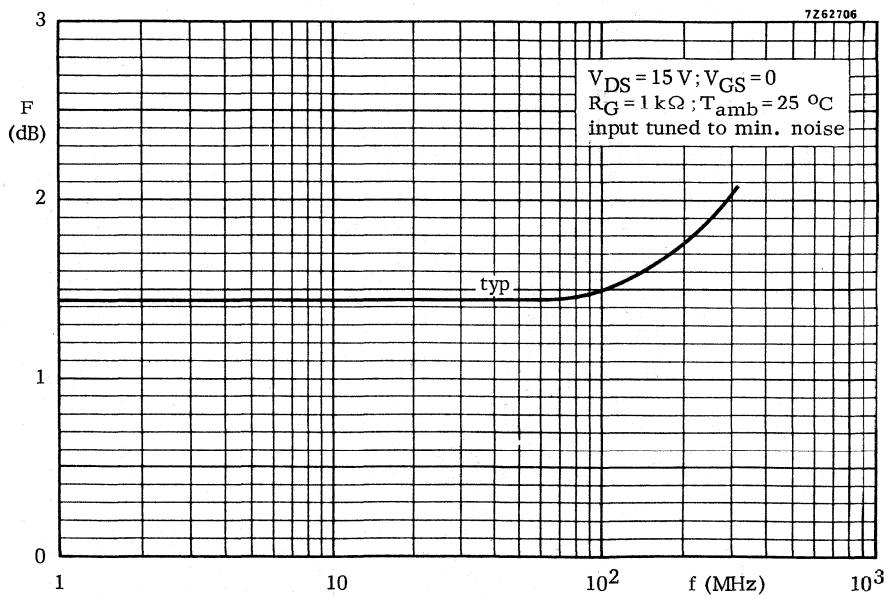


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for VHF and UHF amplifiers, mixers and general purpose switching.

QUICK REFERENCE DATA

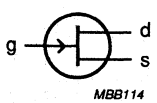
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.			250	mW
			A	B	C	
Drain current		min.	30	60	110	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	max.	80	140	250	mA
Gate-source cut-off voltage						
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$				0.6 to 14.5	V
Feedback capacitance at f = 1 MHz						
I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.			3.5	pF
Transfer admittance (common source)						
I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	min.			8	mS

MECHANICAL DATA

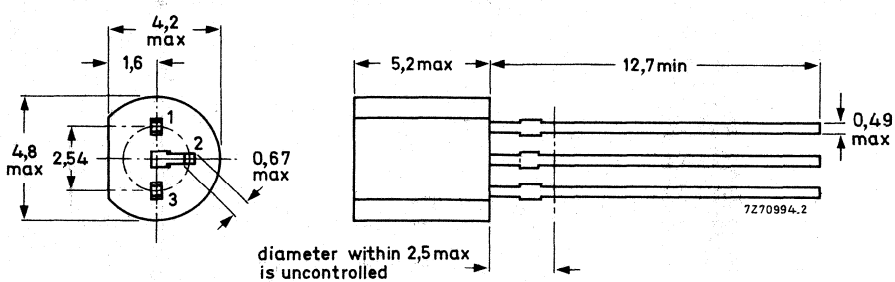
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning (BF246):
1 = drain
2 = gate
3 = source



Pinning (BF247):
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

CHARACTERISTICS

T_{amb} = 25 °C

			A	B	C	
Gate cut-off current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	5	5	5	nA
Drain current* V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	25	25	25	V
Gate-source voltage I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	min.	1.5	3.0	5.5	V
		max.	4.0	7.0	12.0	V
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0.6 to 14.5		V
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	min.			8	mS
		typ.			17	mS
Capacitances at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V						
feed-back capacitance	C_{rs}	typ.			3.5	pF
input capacitance	C_{is}	typ.			11	pF
output capacitance	C_{os}	typ.			5	pF
Cut-off frequency** V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.			450	MHz

* Measured under pulse conditions; t_p = 300 μs; $\delta \leqslant 0.02$.

** The frequency at which g_{fs} is 0.7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

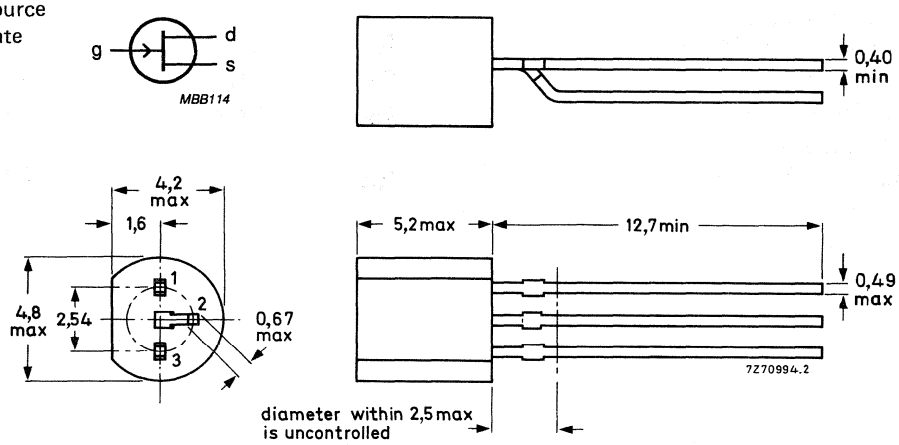
Drain-source voltage	$\pm V_{DS}$		max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$		max.	30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}		max.	300	mW
		BF256A | B | C			
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>3 | 6 | 11 <7 | 13 | 18			mA mA
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}		typ.	0,7	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\lvert y_{fs} \rvert$		>	4,5	mS
Power gain at f = 800 MHz V_{DS} = 15 V; R_S = 47 Ω	G_p		typ.	11	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning;
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W 1)

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<			5	nA
			BF256A	B	C	
Drain current 2)		>	3	6	11	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	<	7	13	18	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>			30	V
Gate-source voltage						
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)				0,5 to 7,5	V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF256B/1: I_{DSS} = 6 to 8 mA; $-V_{GS}$ = 1,4 to 2,6 V.

y-parameters (common source)				
Transistor admittance at f = 1 kHz				
V_{DS} = 15 V; V_{GS} = 0	$\|y_{fs}\|$	>	4,5 mS	1)
		typ.	5 mS	1)
Output capacitance at f = 1 MHz				
V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.	1,2 pF	
Feedback capacitance at f = 1 MHz				
V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.	0,7 pF	
Cut-off frequency				
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	1 GHz	2)
Noise figure at f = 800 MHz				
V_{DS} = 10 V; R_S = 47 Ω	F	typ.	7,5 dB	
Power gain at f = 800 MHz				
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11 dB	

1) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

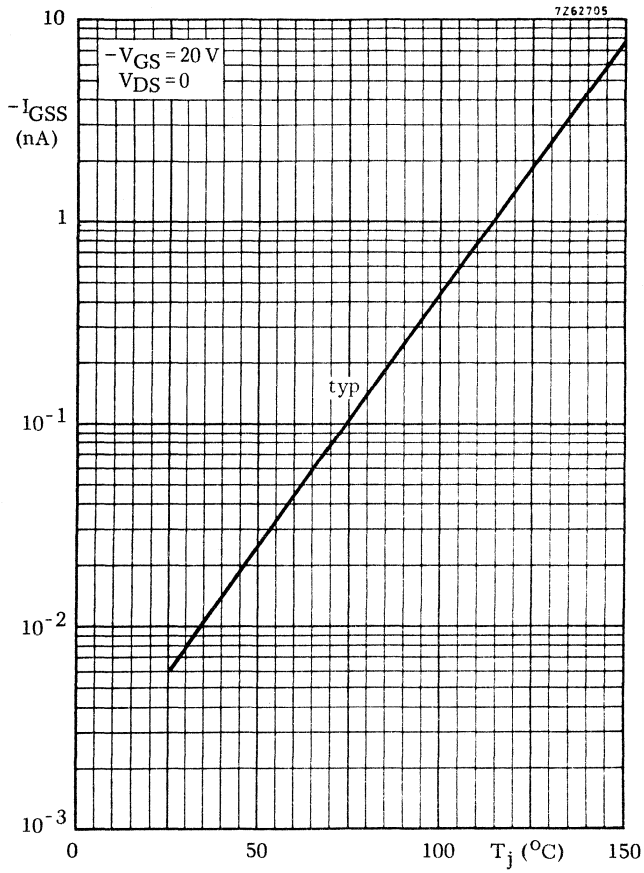

7Z62705
10
$-V_{GS}$ = 20 V
V_{DS} = 0
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (°C)
150

Fig. 2

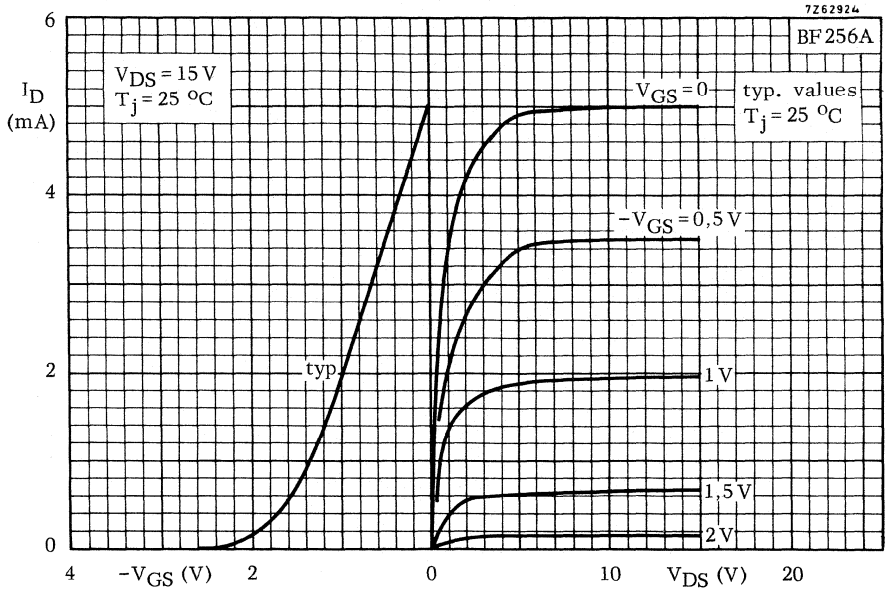

7Z62924
BF256A
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
typ
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

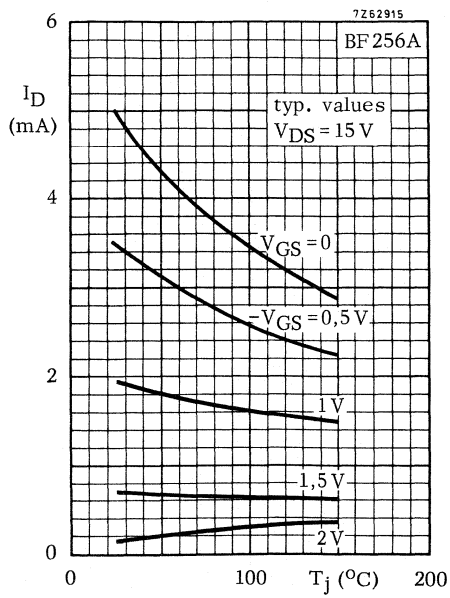

7Z62915
BF256A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
6
4
2
0
0
100
T_j (°C)
200

Fig. 4

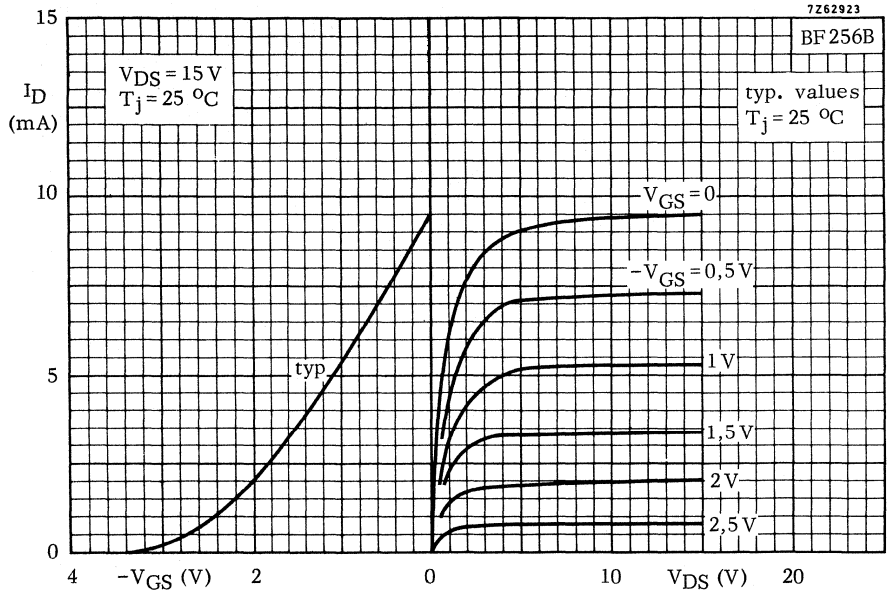

7Z62923
BF256B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
2,5 V
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

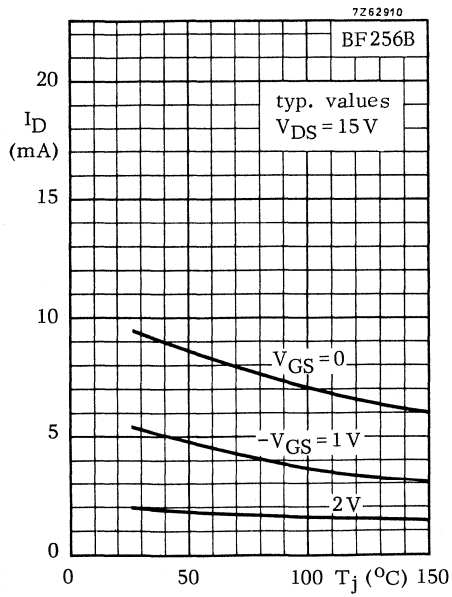

7Z62910
BF256B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

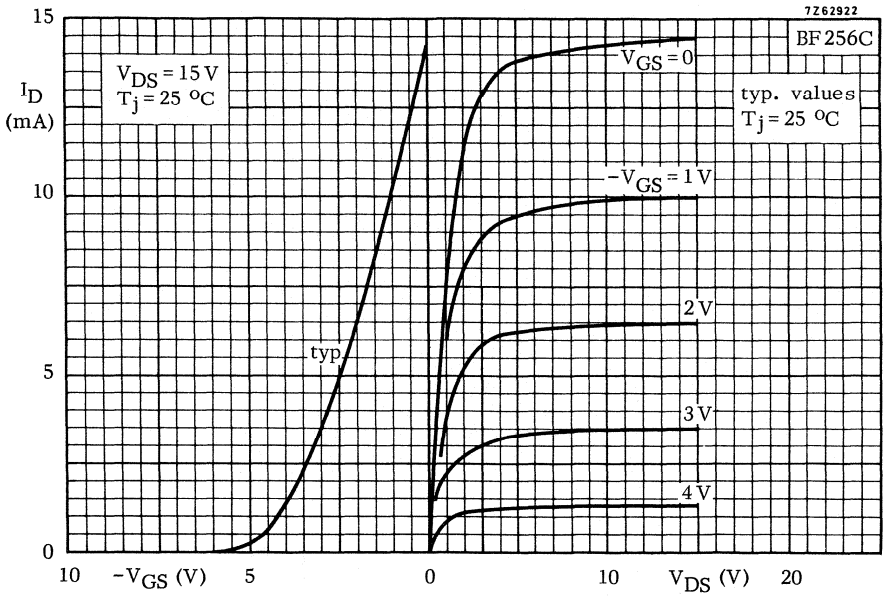

7Z62922
BF256C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
$-V_{GS}$ = 0
$-V_{GS}$ = 1 V
2 V
3 V
4 V
typ
15
10
5
0
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

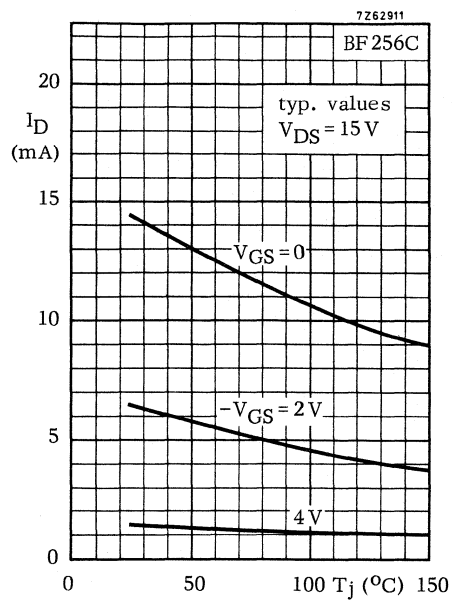

7Z62911
BF256C
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
20
15
10
5
0
0
50
100 T_j (°C)
150

Fig. 8

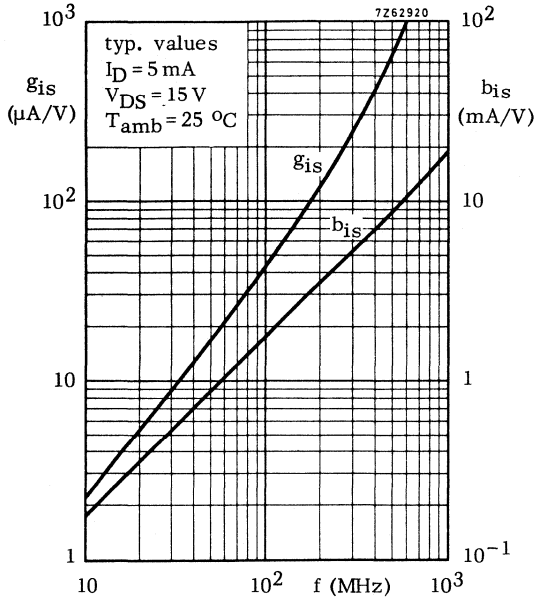

7Z62920
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^{-1}
f (MHz)

Fig. 9

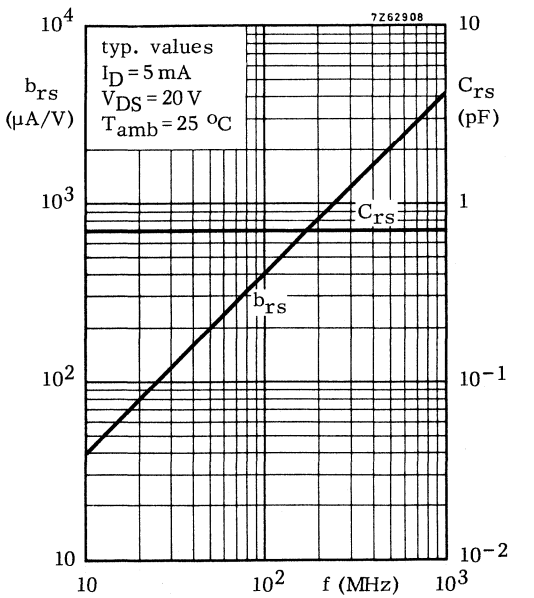

7Z62908
typ. values
I_D = 5 mA
V_{DS} = 20 V
T_{amb} = 25 °C
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
f (MHz)

Fig. 10

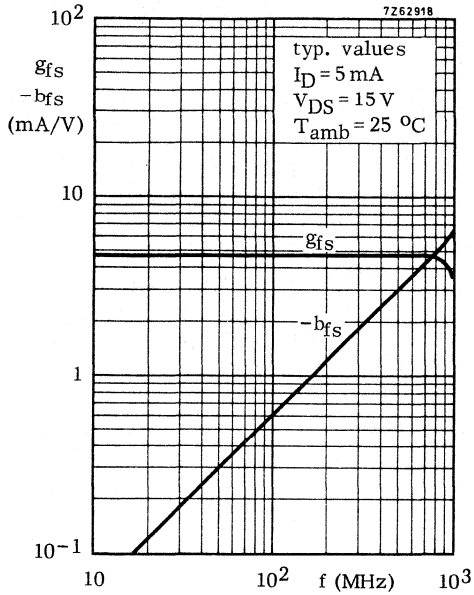

7Z62918
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{fs}
$-b_{fs}$
(mA/V)
10^2
10
1
10^{-1}
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

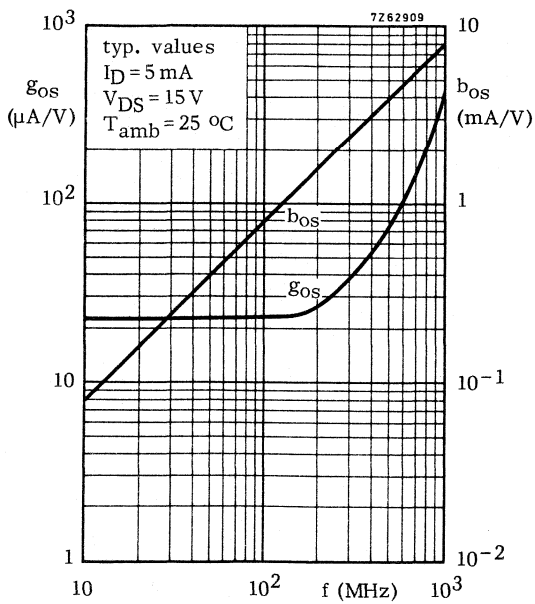

7Z62909
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{os}
(μA/V)
b_{os}
(mA/V)
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
b_{os}
g_{os}
10
10^2
f (MHz)
10^3

Fig. 12

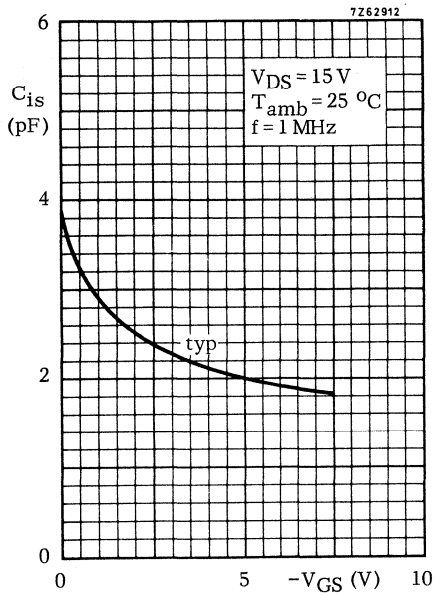


Fig. 13

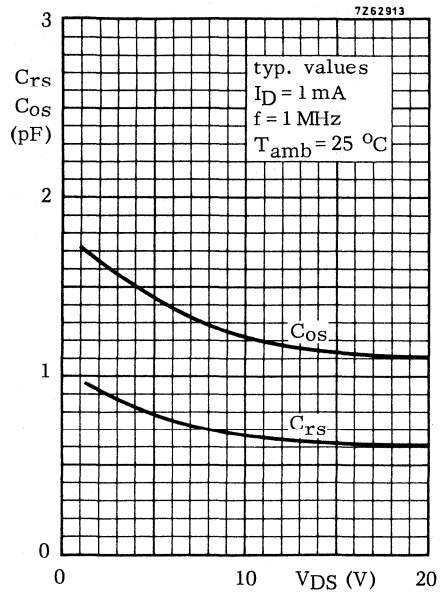


Fig. 14

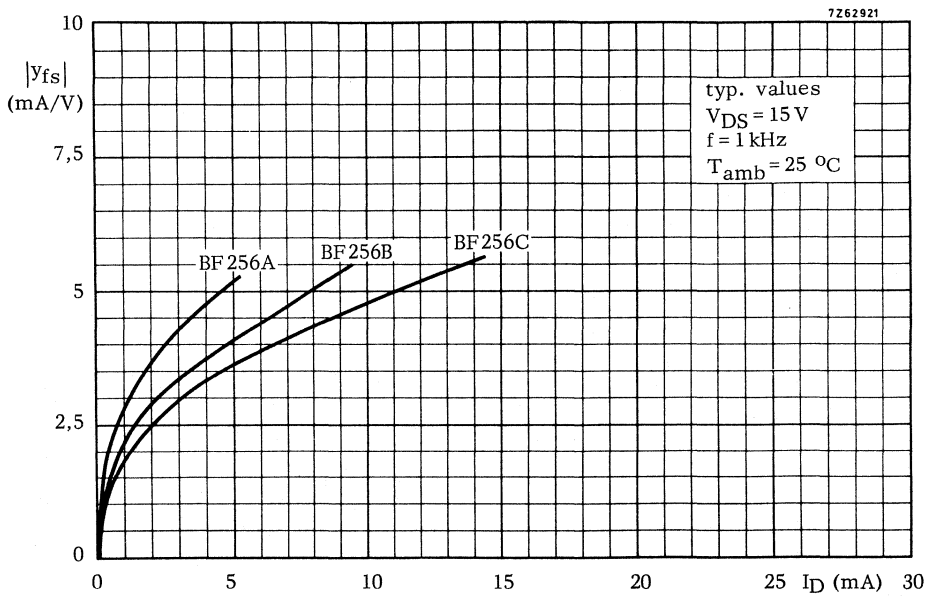


Fig. 15

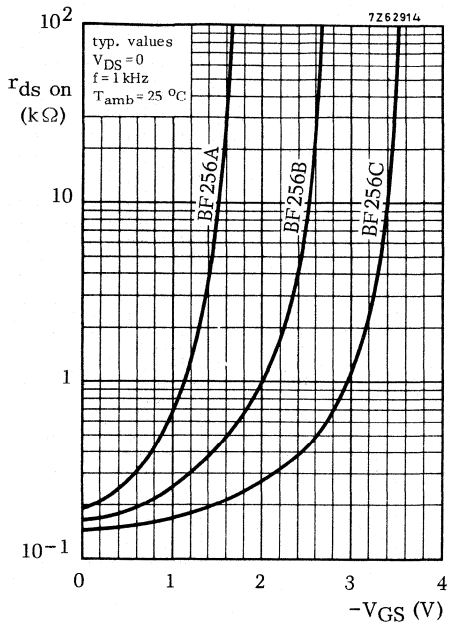


Fig. 16

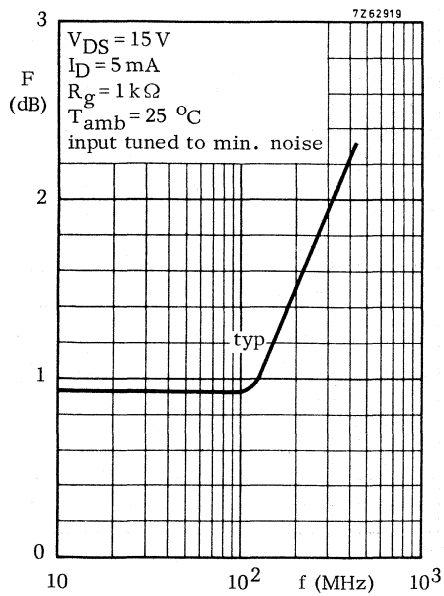


Fig. 17

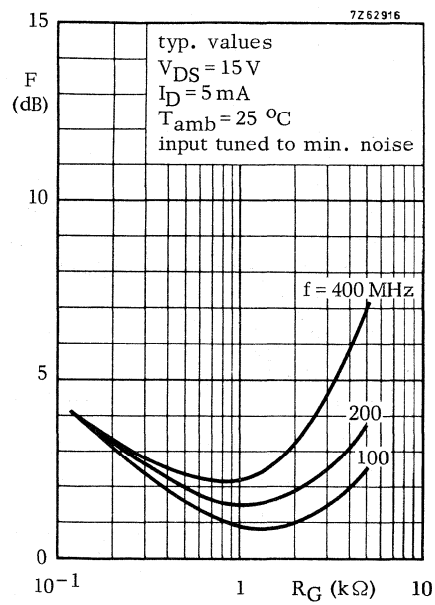


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the VHF range.
These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the RF stages in FM portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

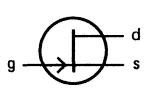
Drain-source voltage	V_{DS}	max.		20			V
Drain current (DC or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.		300			mW
			BF410A	B	C	D	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Transfer admittance V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	min.	2.5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.5	0.5	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0.5	0.5	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz							
V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1.5	1.5	dB

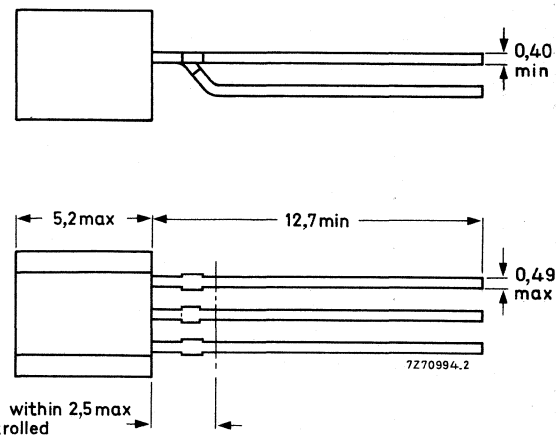
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	max.	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	min.	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for **BF410A** and **B**

V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for **BF410C** and **D**

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	max.	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.5	0.5	0.5	0.5	pF
		max.	0.7	0.7	0.7	0.7	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\lvert y_{fs} \rvert$	min.	—	—	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	max.	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	max.	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

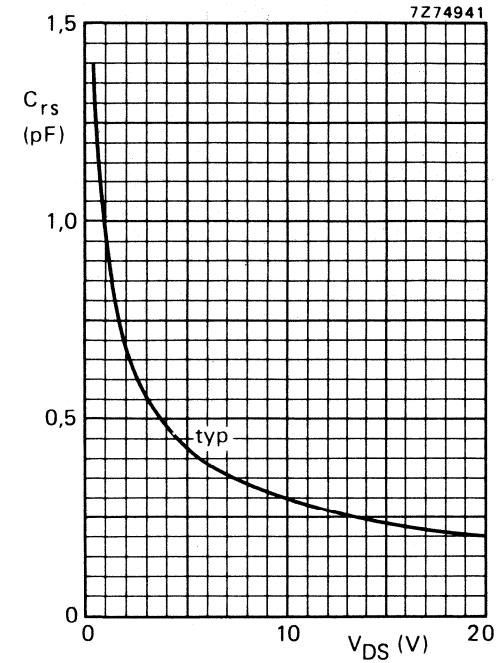


Fig. 2 V_{GS} = 0 for **BF410A** and **BF410B**; I_D = 5 mA for **BF410C** and **BF410D**; f = 1 MHz; T_{amb} = 25 °C.

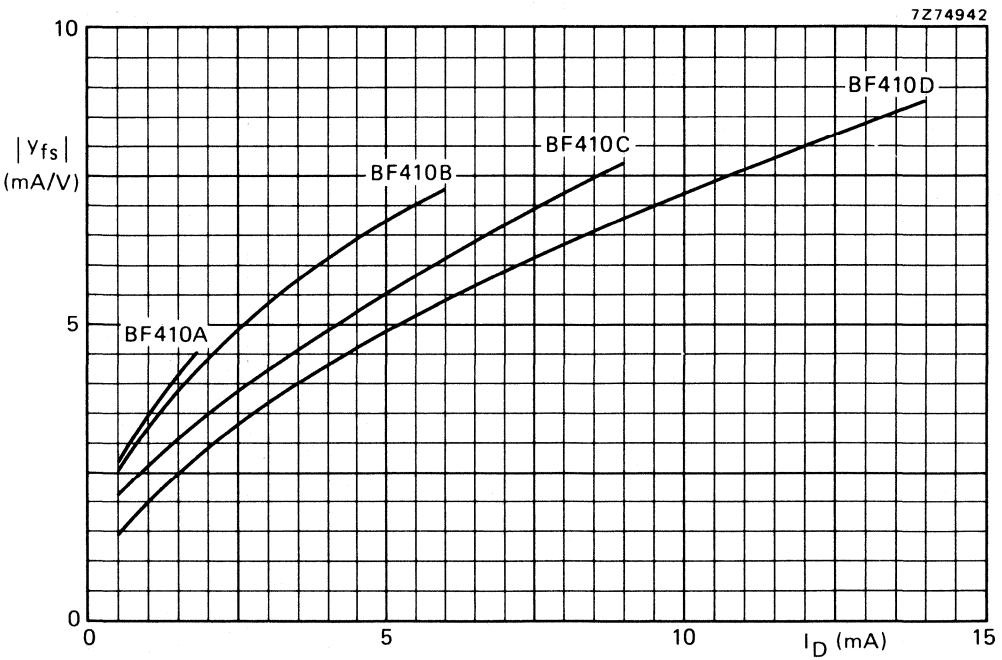


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.			20		V
Drain current (DC or average)	I_D	max.			30		mA
Total power dissipation up to $T_{amb} = 40\ ^oC$	P_{tot}	max.			250		mW
			BF510	511	512	513	
Drain current $V_{DS} = 10$ V; $V_{GS} = 0$	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Transfer admittance (common source) $V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2.5	4	6	7	mS
Feedback capacitance $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	0.3	0.3	–	–	pF
$V_{DS} = 10$ V; $I_D = 5$ mA	C_{rs}	typ.	–	–	0.3	0.3	pF
Noise figure at optimum source admittance $G_S = 1$ mS; $-B_S = 3$ mS; f = 100 MHz							
$V_{DS} = 10$ V; $V_{GS} = 0$	F	typ.	1.5	1.5	–	–	dB
$V_{DS} = 10$ V; $I_D = 5$ mA	F	typ.	–	–	1.5	1.5	dB

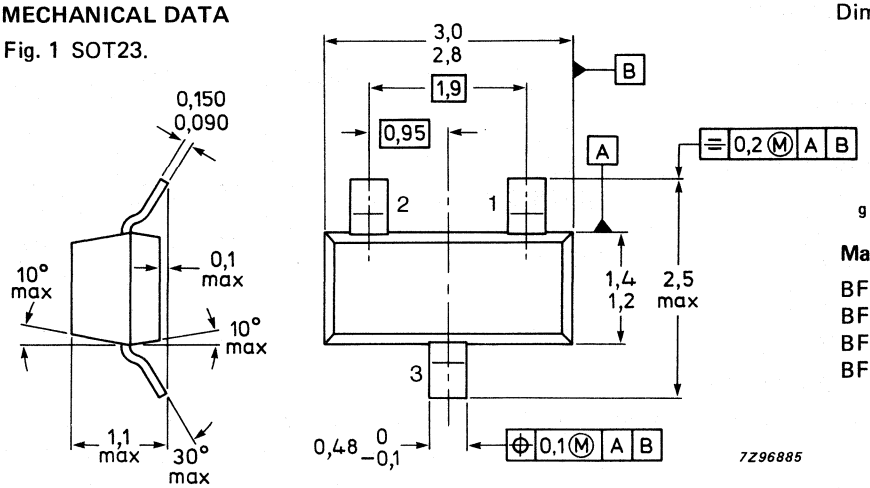
MECHANICAL DATA

SOT23.

See also *Soldering recommendations.*

MECHANICAL DATA

Fig. 1 SOT23.

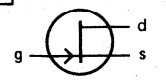


TOP VIEW

Dimensions in mm

Pinning

1 = gate
2 = drain
3 = source



Marking code

BF510 = S6p
BF511 = S7p
BF512 = S8p
BF513 = S9p

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-gate voltage (open source)	V_{DGO}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate current	$\pm I_G$	max.	10 mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

Note

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current							
$-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511

V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.3	0.3	0.3	0.3	pF
		<	0.4	0.4	0.4	0.4	pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	>	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance							
G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

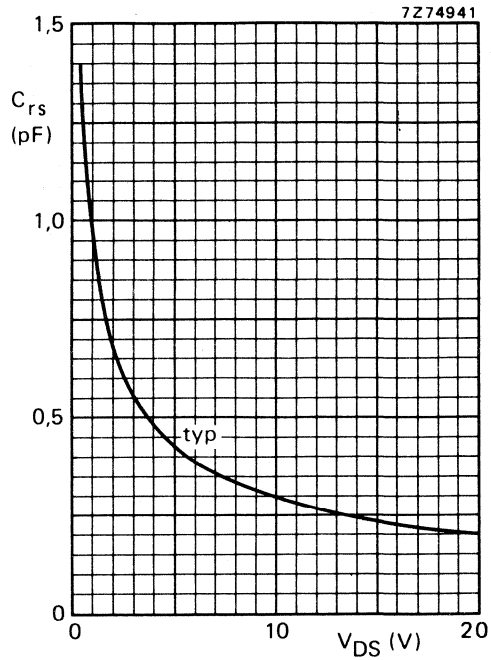


Fig. 2 V_{GS} = 0 for BF510 and BF511; I_D = 5 mA for BF512 and BF513; f = 1 MHz; T_{amb} = 25 °C.

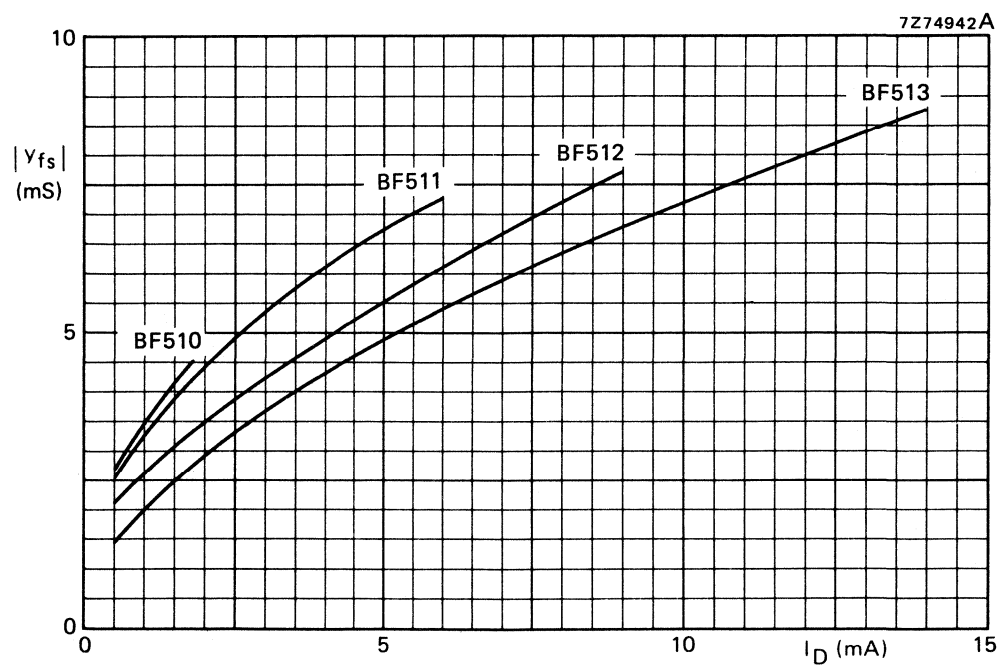


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

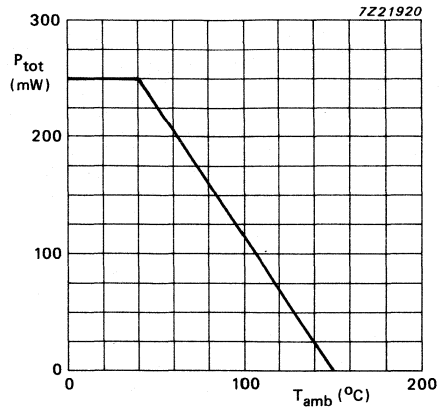


Fig.4 Power derating curve.

N-channel silicon junction field-effect transistor

BF545A; BF545B; BF545C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage (max. 2.2 V for BF545A).

DESCRIPTION

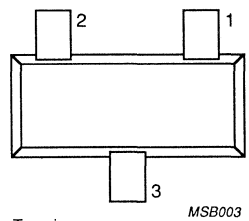
N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING

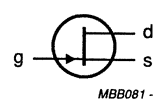
PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF545A		2	6.5	mA
	BF545B		6	15	mA
	BF545C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 μA	0.4	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	6.5	mS



Top view



Marking codes:
BF545A: M65.
BF545B: M66.
BF545C: M67.

Fig.1 Simplified outline (SOT23) and symbol.

N-channel silicon junction field-effect transistor

BF545A; BF545B; BF545C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

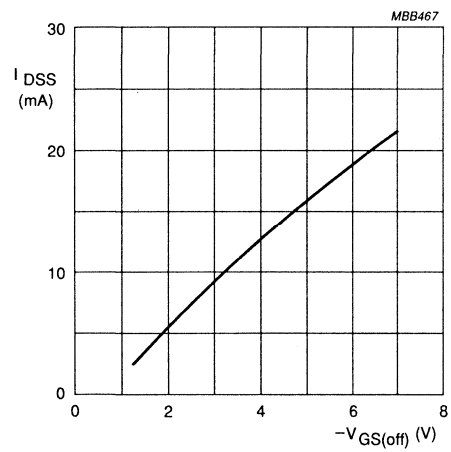
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{DS}$ = 0; $-V_{GS}$ = 20 V	–	0.5	1000	pA
		$-V_{DS}$ = 0; $-V_{GS}$ = 20 V; T_j = 125 °C	–	–	100	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF545A		2	–	6.5	mA
	BF545B		6	–	15	mA
	BF545C		12	–	25	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 µA	30	–	–	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 µA				
	BF545A		0.4	–	2.2	V
	BF545B		1.6	–	3.8	V
	BF545C		3.2	–	7.8	V
		V_{DS} = 15 V; I_D = 1 µA	0.4	–	7.5	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	–	6.5	mS
Y_{os}	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	µS

DYNAMIC CHARACTERISTICS

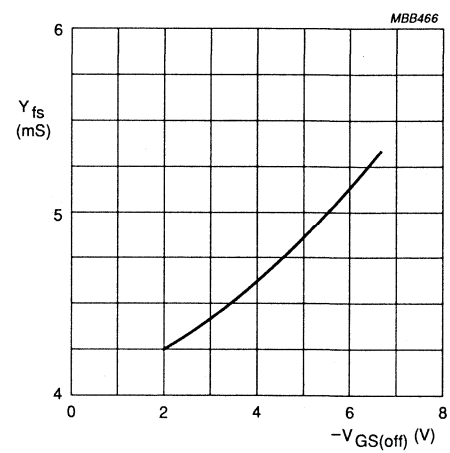
T_a = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	3	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	µS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
$-g_{rs}$	common source feedback conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	6	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	40	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	µS



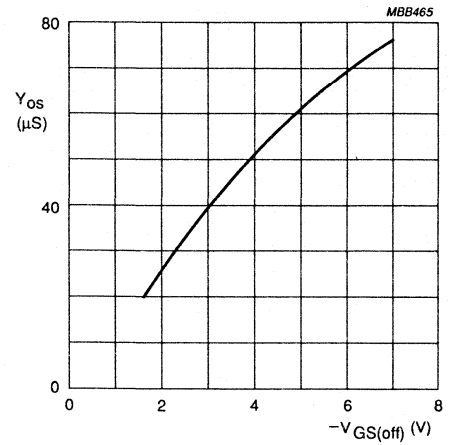
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage.



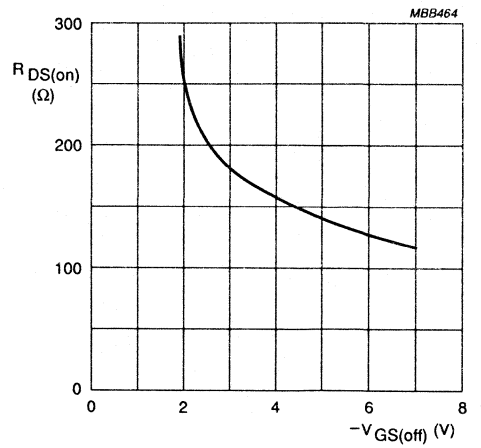
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



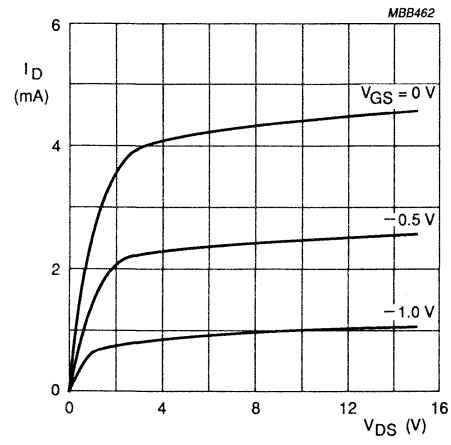
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.4 Common source output admittance as a function of gate-source cut-off voltage.



V_{DS} = 100 mV; V_{GS} = 0; T_j = 25 °C.

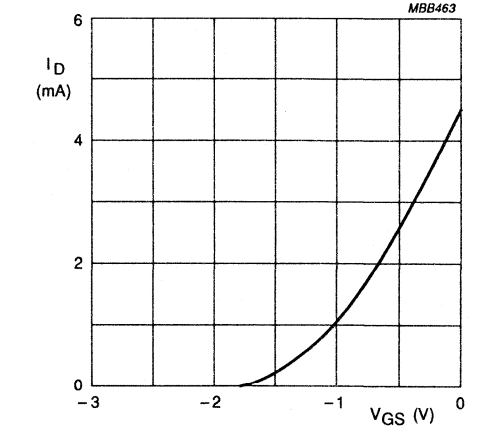
Fig.5 Drain-source on-resistance as a function of gate-source cut-off voltage.



BF545A

T_j = 25 °C.

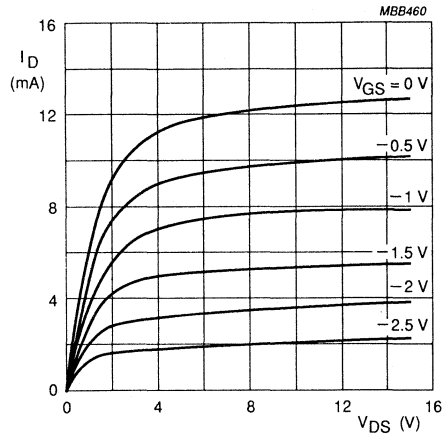
Fig.6 Typical output characteristics.



BF545A

V_{DS} = 15 V; T_j = 25 °C.

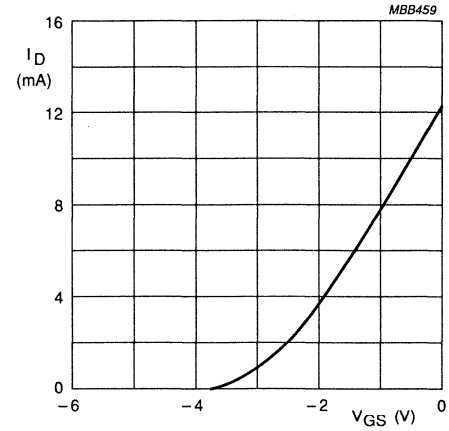
Fig.7 Typical input characteristics.



BF545B

T_j = 25 °C.

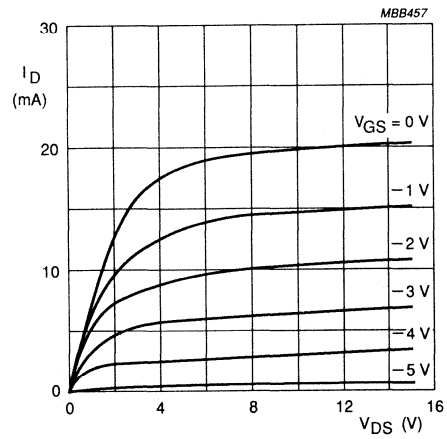
Fig.8 Typical output characteristics.



BF545B

V_{DS} = 15 V; T_j = 25 °C.

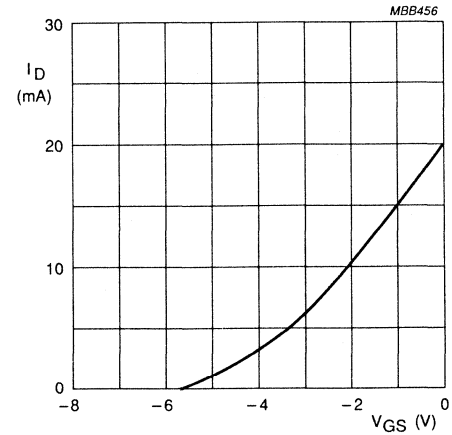
Fig.9 Typical input characteristics.



BF545C

T_j = 25 °C.

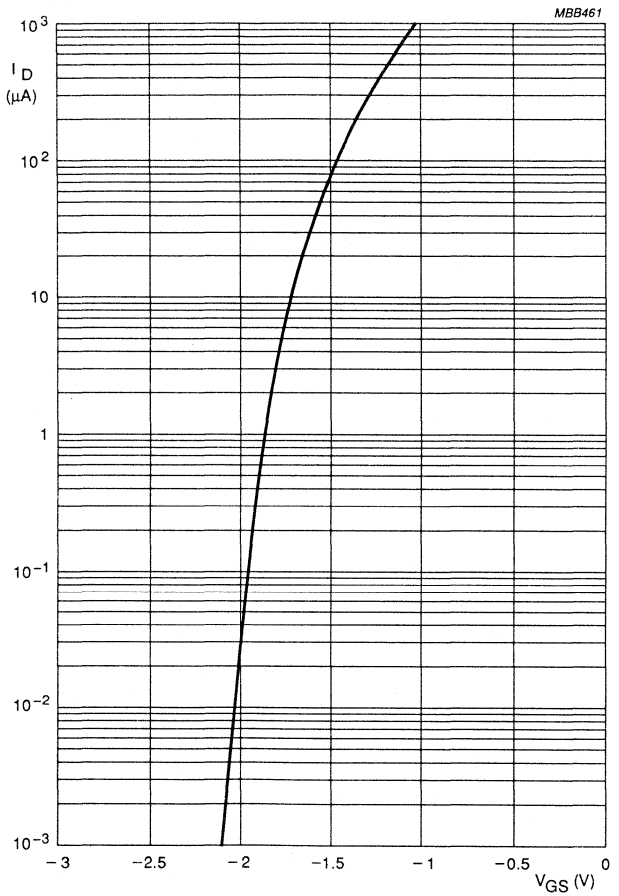
Fig.10 Typical output characteristics.



BF545C

V_{DS} = 15 V; T_j = 25 °C.

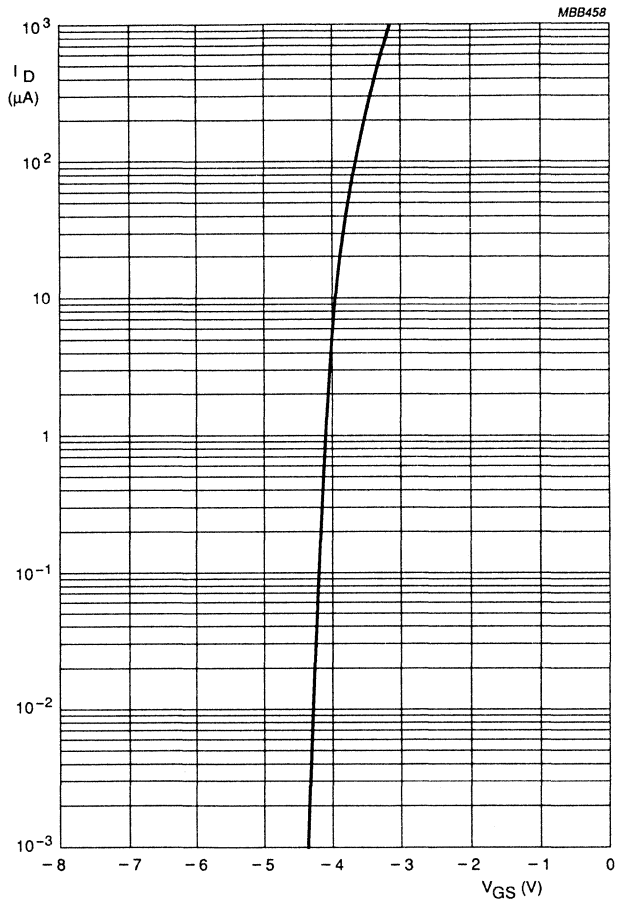
Fig.11 Typical input characteristics.



BF545A

V_{DS} = 15 V; T_j = 25 °C.

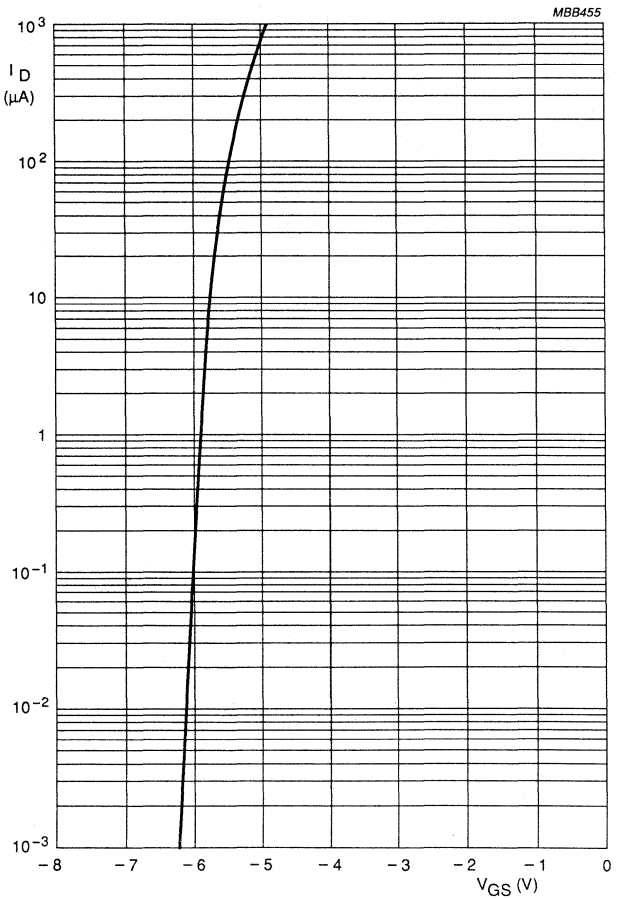
Fig.12 Drain current as a function of gate-source voltage; typical values.



BF545B

V_{DS} = 15 V; T_j = 25 °C.

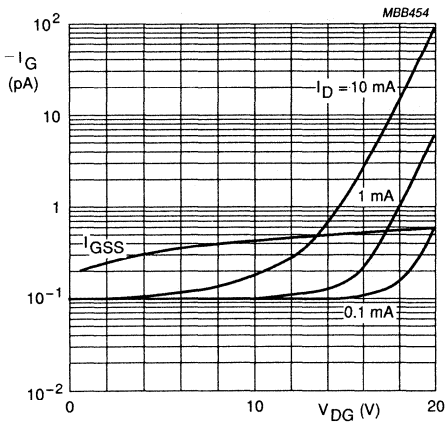
Fig.13 Drain current as a function of gate-source voltage; typical values.



BF545C

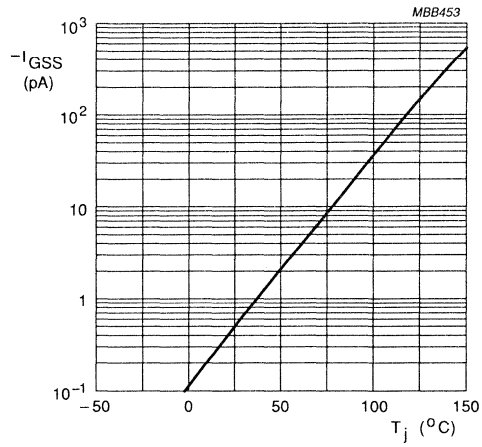
V_{DS} = 15 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage; typical values.



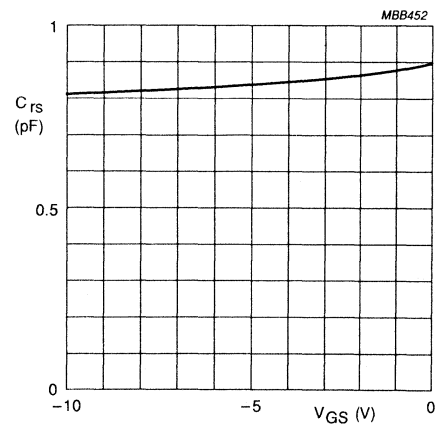
I_D = 10 mA (BF545B and C only); T_j = 25 °C.

Fig.15 Gate current as a function of drain-gate voltage, typical values.



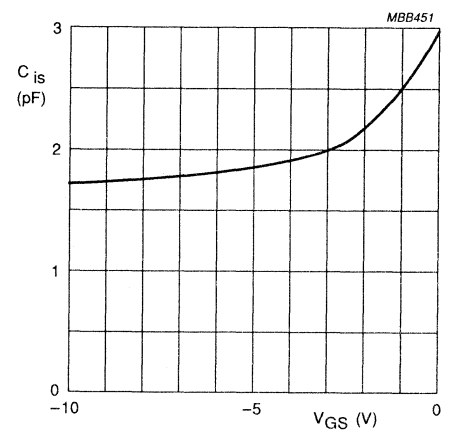
V_{DS} = 0; $-V_{GS}$ = 20 V.

Fig.16 Gate current as a function of junction temperature, typical values.



V_{DS} = 15 V; T_j = 25 °C.

Fig.17 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.18 Typical input capacitance.

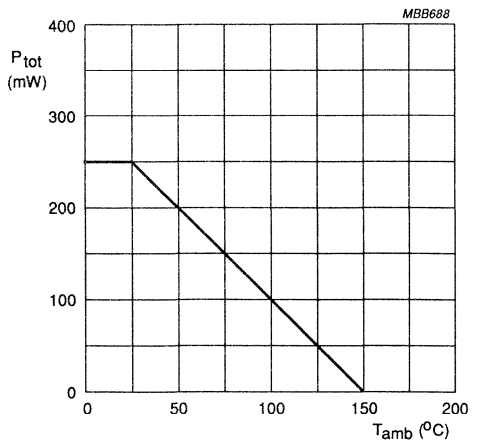
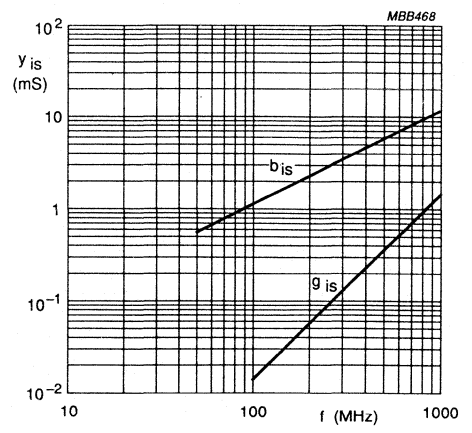
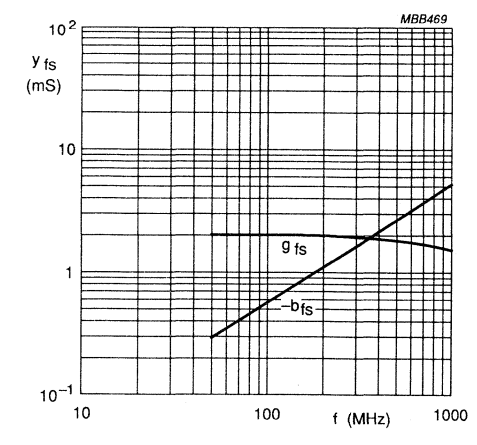


Fig.19 Power derating curve.



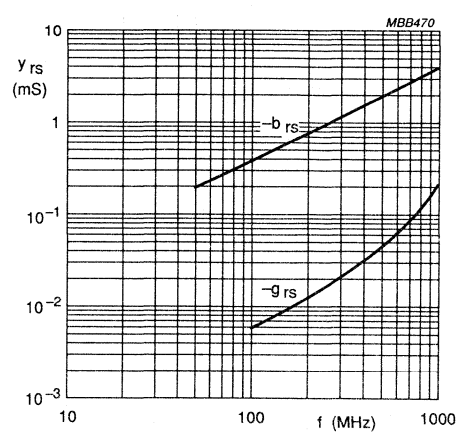
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.20 Common source input conductance.



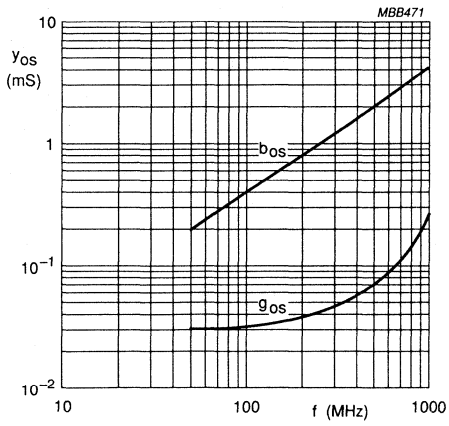
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.21 Common source transfer conductance.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.22 Common source feedback conductance.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.23 Common source output conductance.

N-channel field-effect transistors BF556A;BF556B;BF556C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING - SOT23

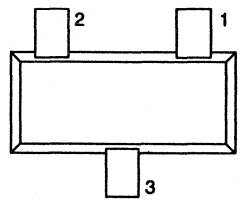
PIN	DESCRIPTION
1	source
2	drain
3	gate

CAUTION

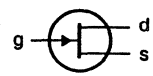
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF556A		3	7	mA
	BF556B		6	13	mA
	BF556C		11	18	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 μA	0.5	7.5	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	–	mS



Top view



MAM036

Marking codes:
BF556A: M84.
BF556B: M85.
BF556C: M86.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead 10 mm².

STATIC CHARACTERISTICS

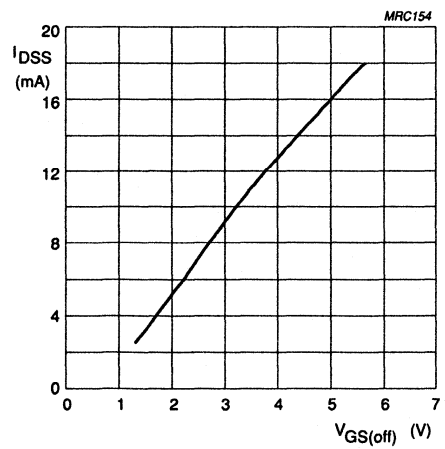
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 µA	30	–	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF556A		3	–	7	mA
	BF556B		6	–	13	mA
	BF556C		11	–	18	mA
$-I_{GSS}$	reverse gate leakage current	V_{DS} = 0; $-V_{GS}$ = 20 V	–	0.5	5000	pA
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 µA	0.5	–	7.5	V
$\lvert Y_{fs}\rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	–	–	mS
$\lvert Y_{os}\rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	µS

DYNAMIC CHARACTERISTICS

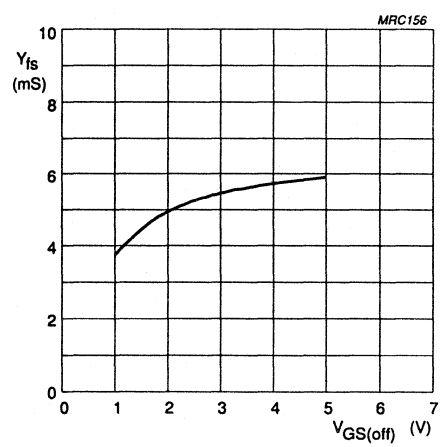
T_a = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	3	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	µS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
$-g_{rs}$	common source feedback conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	6	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	40	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	µS
V_n	equivalent input noise voltage	VDS = 10 V; I_D = 1 mA; f = 100 Hz	40	nV/√Hz



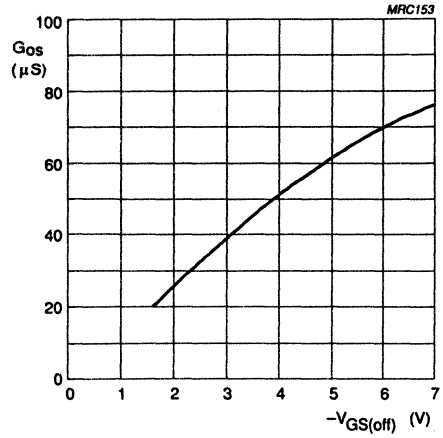
V_{DS} = 15 V.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



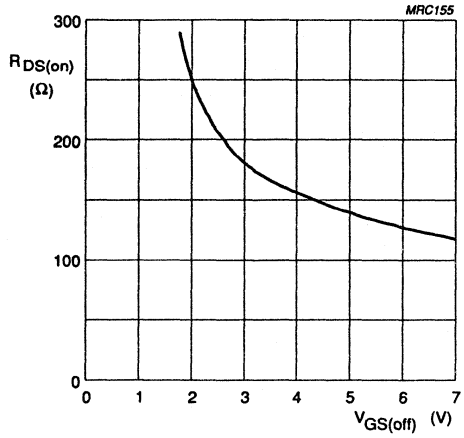
V_{DS} = 15 V; I_D = 1 µA.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



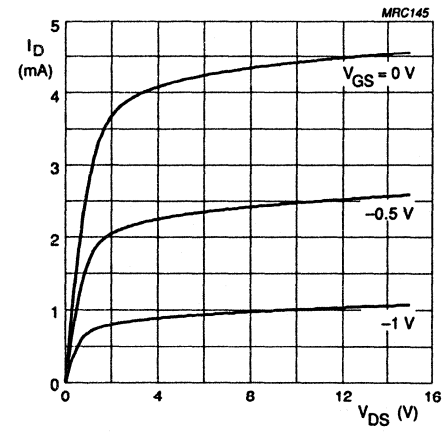
V_{DS} = 15 V.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



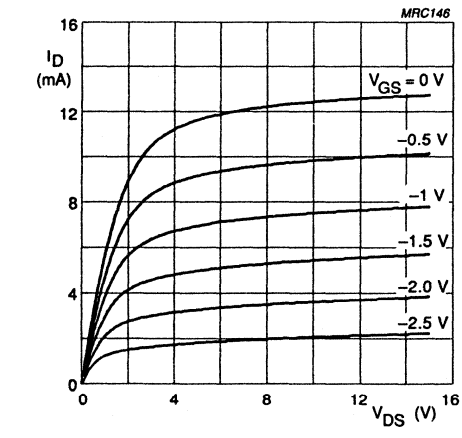
V_{DS} = 100 mV; V_{GS} = 0.

Fig.5 Drain-source on-resistance as a function of gate-source cut-off voltage; typical values.



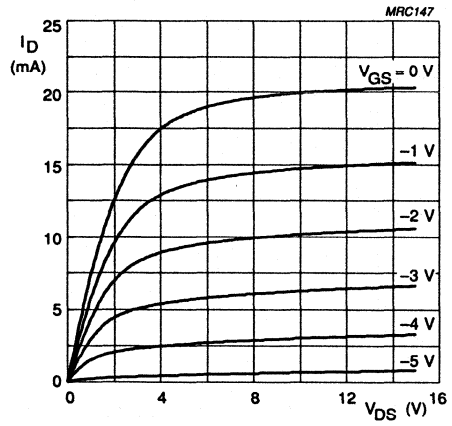
BF556A

Fig.6 Typical output characteristics.



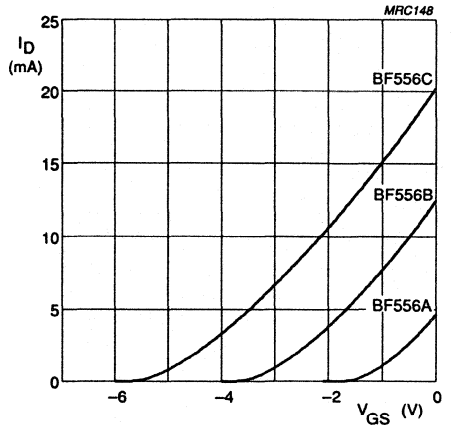
BF556B

Fig.7 Typical output characteristics.



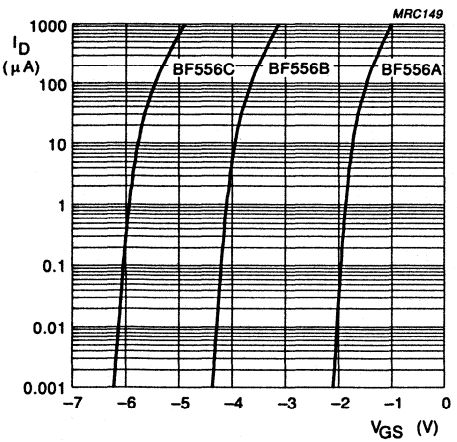
BF556C

Fig.8 Typical output characteristics.



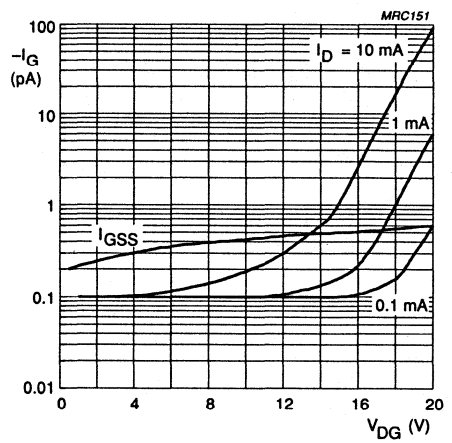
V_{DS} = 15 V.

Fig.9 Typical input characteristics.



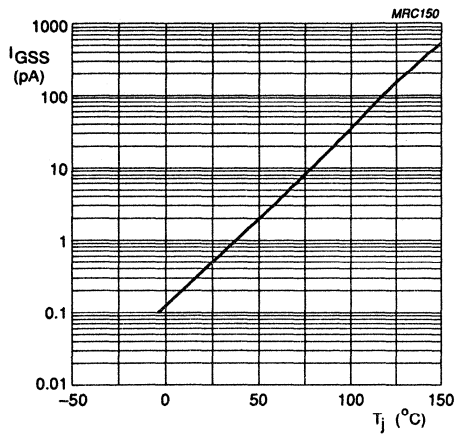
V_{DS} = 15 V.

Fig.10 Drain current as a function of gate-source voltage; typical values.



(I_D = 10 mA only for BF556B and BF556C).

Fig.11 Gate current as a function of drain-gate voltage; typical values.



V_{DS} = 0; $-V_{GS}$ = 20 V.

Fig.12 Gate current as a function of junction temperature; typical values.

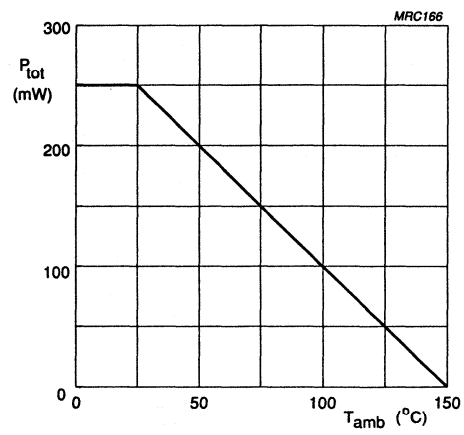
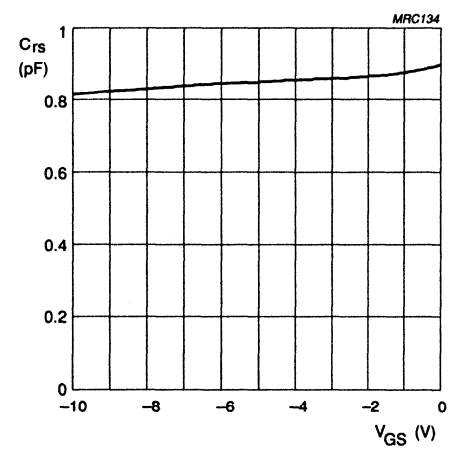
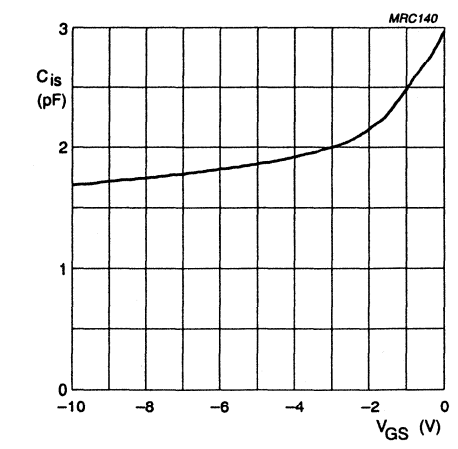


Fig.13 Power derating curve.



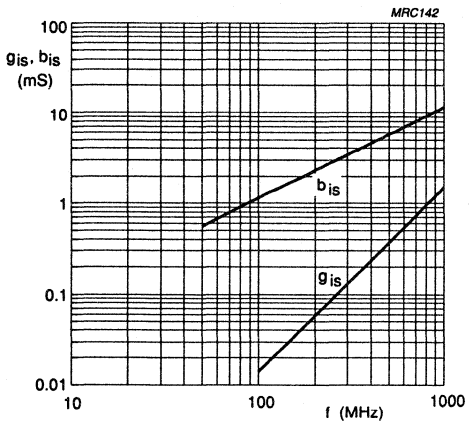
V_{DS} = 15 V.

Fig.14 Typical feedback capacitance.



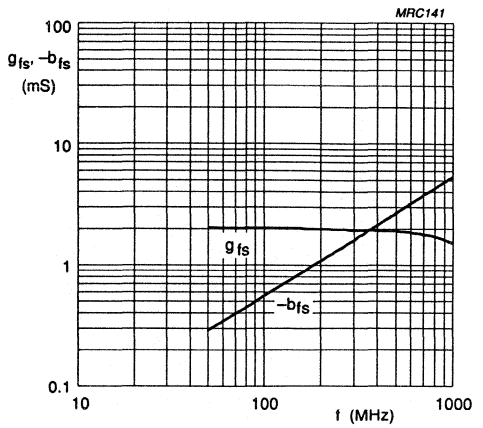
V_{DS} = 15 V.

Fig.15 Typical input capacitance.



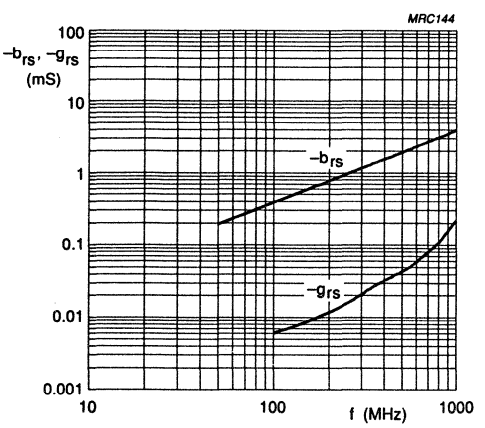
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.16 Common source input conductance; typical values.



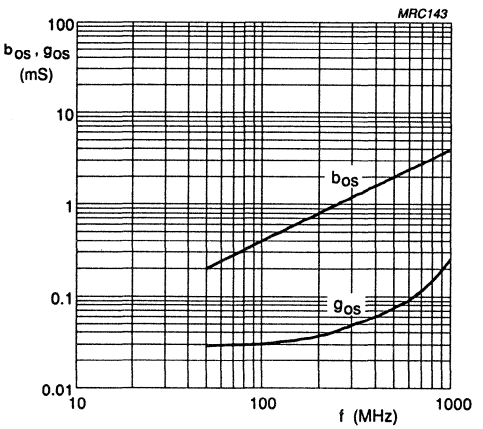
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.17 Common source transfer conductance; typical values.



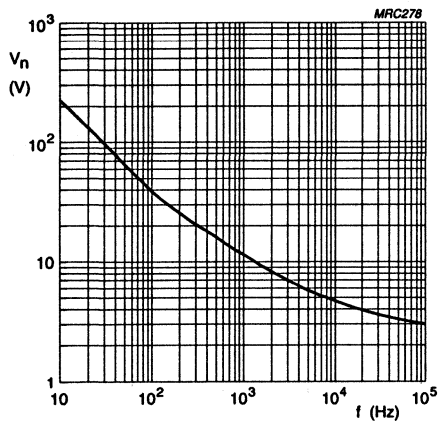
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.18 Common source feedback conductance; typical values.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.19 Common source output conductance; typical values.



V_{DS} = 10 V; I_D = 1 mA.

Fig.20 Equivalent noise voltage as a function of frequency.

N-channel junction FETs BF851A; BF851B; BF851C

FEATURES

- High transfer admittance
- Low input capacitance
- Low feedback capacitance
- Low noise.

APPLICATIONS

- Preamplifiers for AM tuners in car radios.

DESCRIPTION

N-channel symmetrical junction field effect transistors in a SOT54 (TO-92) package.

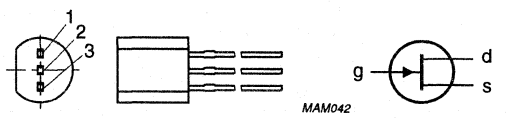


Fig.1 Simplified outline and symbol.

PINNING - SOT54 (TO-92)

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 8 V			
	BF851A		2	6.5	mA
	BF851B		6	15	mA
	BF851C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 40 °C	–	400	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 8 V			
	BF851A		12	20	mS
	BF851B		16	25	mS
	BF851C		20	30	mS
C_{iss}	input capacitance	f = 1 MHz	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	3	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
V_{GSO}	gate-source voltage	open drain	–	25	V
V_{DGO}	drain-gate voltage (DC)	open source	–	25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 40 °C; note 1	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board; maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

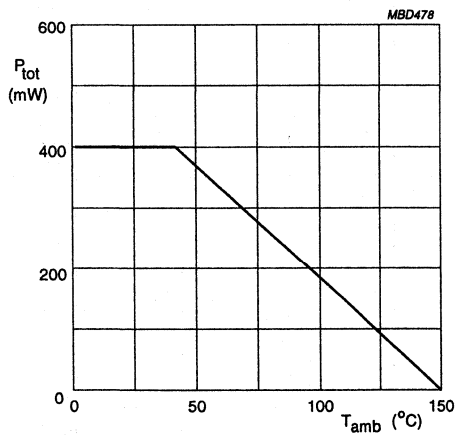


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	250	K/W

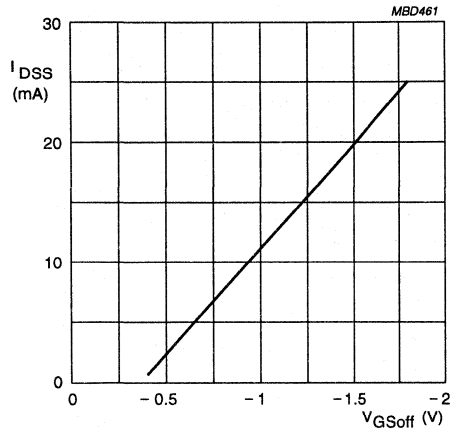
Note

1. Device mounted on an epoxy printed-circuit board; maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

CHARACTERISTICS

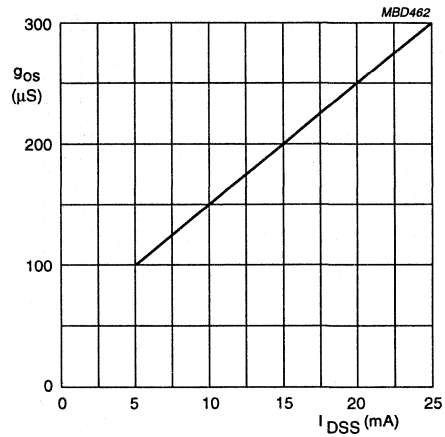
T_j = 25 °C; V_{DS} = 8 V; V_{GS} = 0; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA	−25	–	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA				
	BF851A		−0.2	–	−1	V
	BF851B		−0.5	–	−1.5	V
	BF851C		−0.8	–	−2	V
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
I_{DSS}	drain current					
	BF851A		2	–	6.5	mA
	BF851B		6	–	15	mA
	BF851C		12	–	25	mA
I_{GSS}	gate cut-off current	V_{GS} = −20 V; V_{DS} = 0	–	–	−1	nA
$\lvert y_{fs} \rvert$	forward transfer admittance					
	BF851A		12	–	20	mS
	BF851B		16	–	25	mS
	BF851C		20	–	30	mS
g_{os}	common source output conductance					
	BF851A		–	–	200	μS
	BF851B		–	–	250	μS
	BF851C		–	–	300	μS
C_{iss}	input capacitance	f = 1 MHz	–	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	2.4	3	pF
$V_n/\sqrt{B}$	equivalent input noise voltage	V_{GS} = 0; f = 1 MHz	–	1.5	–	nV/√Hz



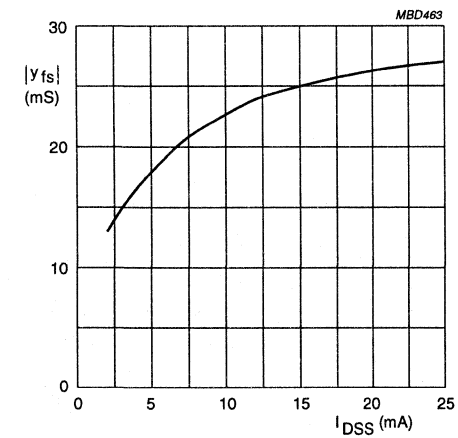
V_{DS} = 8 V.

Fig.3 Drain current as a function of gate-source cut-off voltage; typical values.



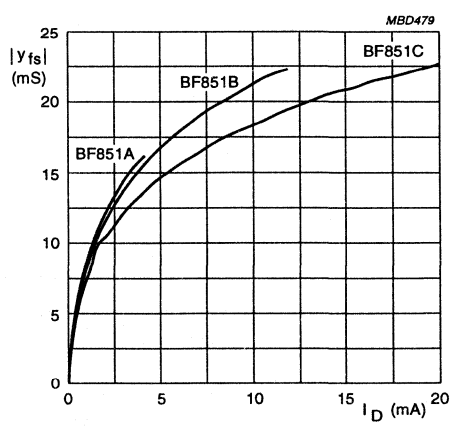
V_{DS} = 8 V.
V_{GS} = 0.

Fig.4 Common-source output conductance as a function of drain current; typical values.



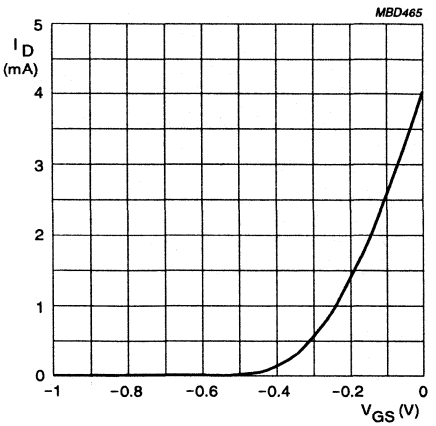
V_{DS} = 8 V.
V_{GS} = 0.

Fig.5 Forward transfer admittance as a function of drain current; typical values.



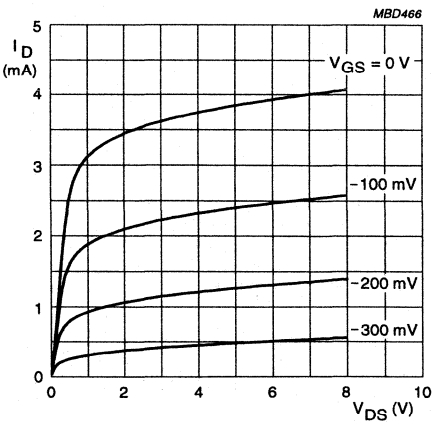
V_{DS} = 8 V.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



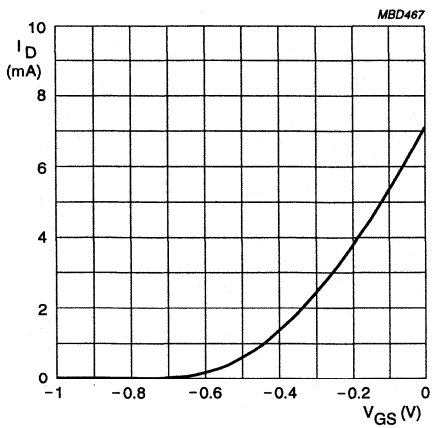
BF851A
V_{DS} = 8 V.

Fig.7 Typical input characteristics.



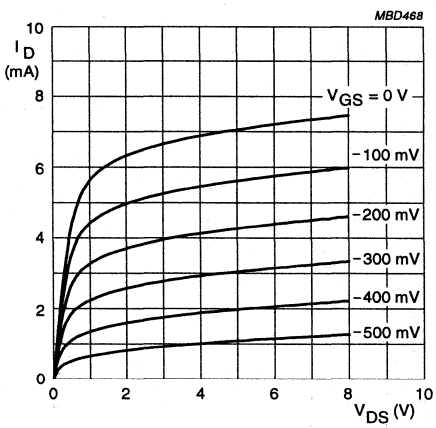
BF851A
V_{DS} = 8 V.

Fig.8 Typical output characteristics.



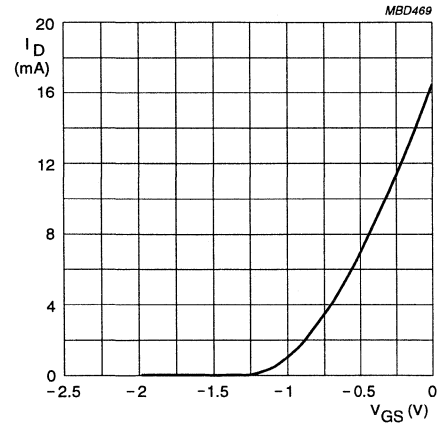
BF851B
V_{DS} = 8 V.

Fig.9 Typical input characteristics.



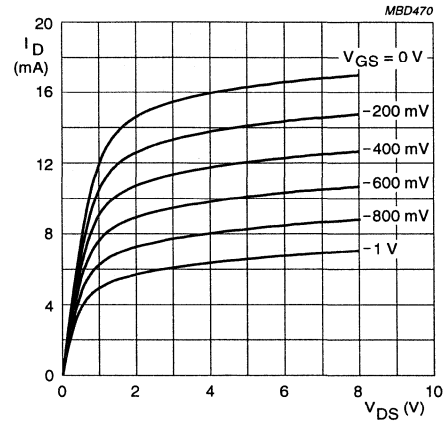
BF851B
V_{DS} = 8 V.

Fig.10 Typical output characteristics.



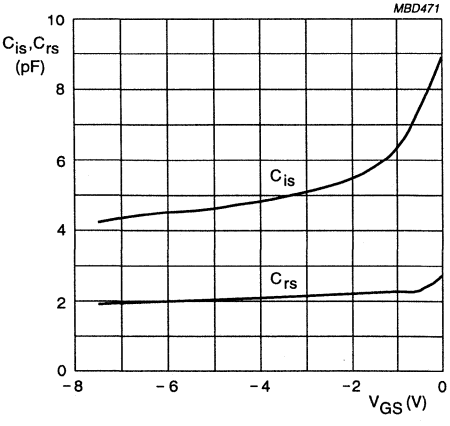
BF851C
V_{DS} = 8 V.

Fig.11 Typical input characteristics.



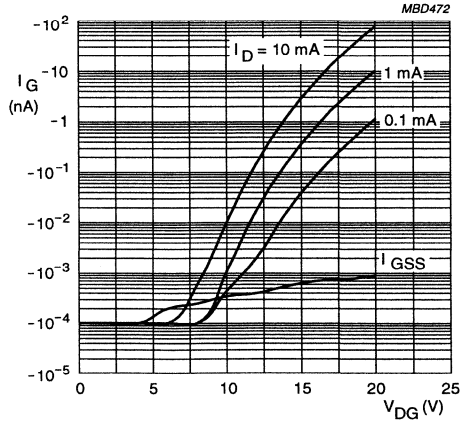
BF851C
V_{DS} = 8 V.

Fig.12 Typical output characteristics.



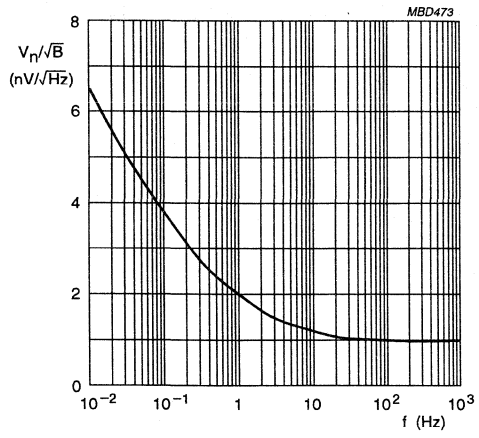
V_{DS} = 8 V.
f = 1 MHz.

Fig.13 Input and reverse transfer capacitance as functions of gate-source voltage; typical values.



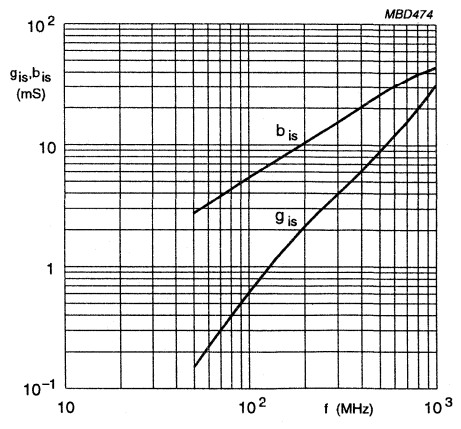
V_{DS} = 8 V.

Fig.14 Gate current as a function of drain-gate voltage; typical values.



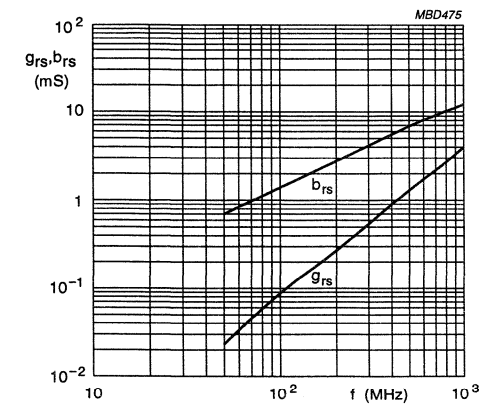
V_{DS} = 8 V.
V_{GS} = 0.

Fig.15 Equivalent input noise as a function of frequency; typical values.



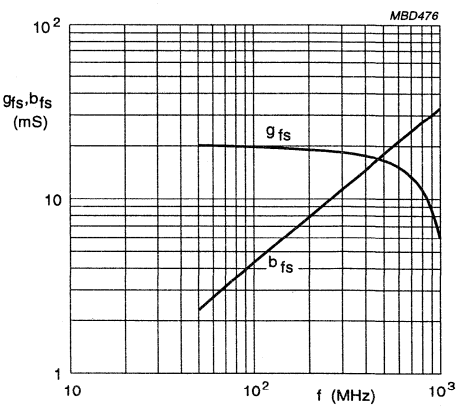
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.16 Common-source input admittance; typical values.



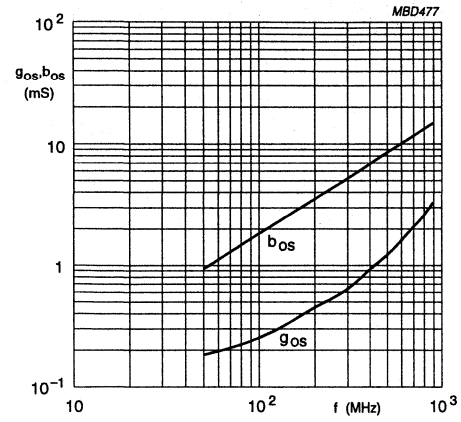
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.17 Common-source reverse admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.18 Common-source forward transfer admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.19 Common-source output admittance; typical values.

N-channel junction FETs BF861A; BF861B; BF861C

FEATURES

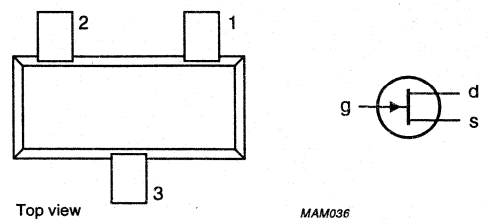
- High transfer admittance
- Low input capacitance
- Low feedback capacitance
- Low noise.

APPLICATIONS

- Preamplifiers for AM tuners in car radios.

DESCRIPTION

N-channel symmetrical junction field effect transistors in a SOT23 package.



Marking codes:
BF861A: M33.
BF861B: M34.
BF861C: M35.

Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
I_{DSS}	drain current	V_{GS} = 0; V_{DS} = 8 V			
	BF861A		2	6.5	mA
	BF861B		6	15	mA
	BF861C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{GS} = 0; V_{DS} = 8 V			
	BF861A		12	20	mS
	BF861B		16	25	mS
	BF861C		20	30	mS
C_{iss}	input capacitance	f = 1 MHz	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	2.7	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	25	V
V_{GSO}	gate-source voltage	open drain	–	25	V
V_{DGO}	drain-gate voltage (DC)	open source	–	25	V
I_G	forward gate current (DC)		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board.

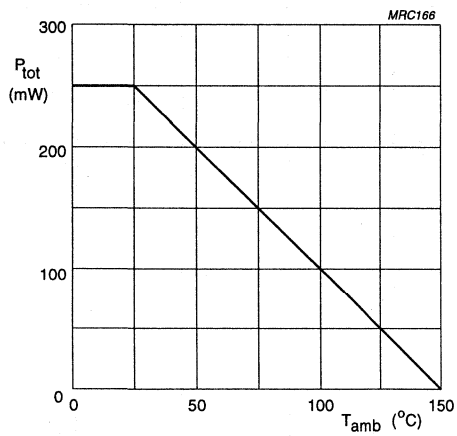


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

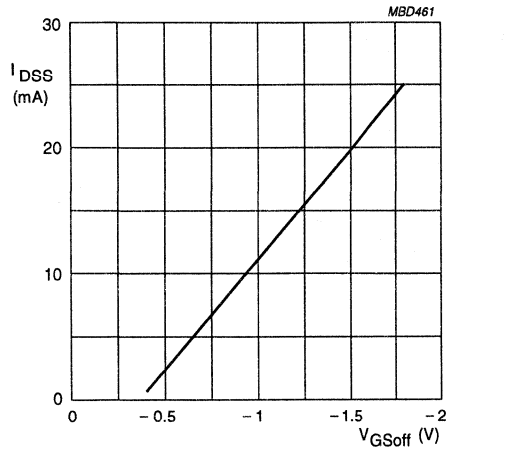
Note

1. Device mounted on an FR4 printed-circuit board.

CHARACTERISTICS

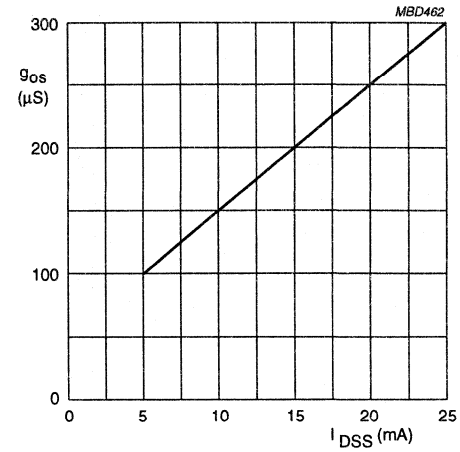
T_j = 25 °C; V_{DS} = 8 V; V_{GS} = 0; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = −1 μA	−25	–	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 1 μA				
	BF861A		−0.2	–	−1	V
	BF861B		−0.5	–	−1.5	V
	BF861C		−0.8	–	−2	V
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
I_{DSS}	drain current					
	BF861A		2	–	6.5	mA
	BF861B		6	–	15	mA
	BF861C		12	–	25	mA
I_{GSS}	gate cut-off current	V_{GS} = −20 V; V_{DS} = 0	–	–	−1	nA
$\lvert y_{fs} \rvert$	forward transfer admittance					
	BF861A		12	–	20	mS
	BF861B		16	–	25	mS
	BF861C		20	–	30	mS
g_{os}	common source output conductance					
	BF861A		–	–	200	μS
	BF861B		–	–	250	μS
	BF861C		–	–	300	μS
C_{iss}	input capacitance	f = 1 MHz	–	–	10	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	2.1	2.7	pF
$V_n/\sqrt{B}$	equivalent input noise voltage	V_{GS} = 0; f = 1 MHz	–	1.5	–	nV/√Hz



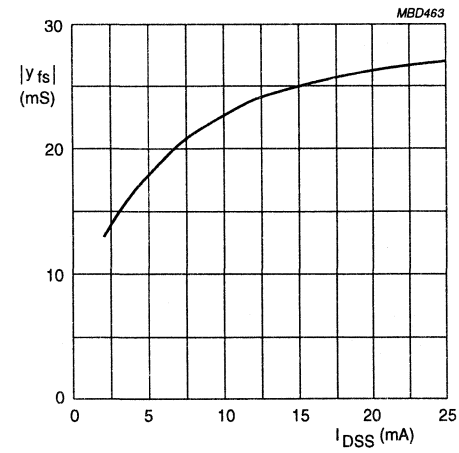
V_{DS} = 8 V.

Fig.3 Drain current as a function of gate-source cut-off voltage; typical values.



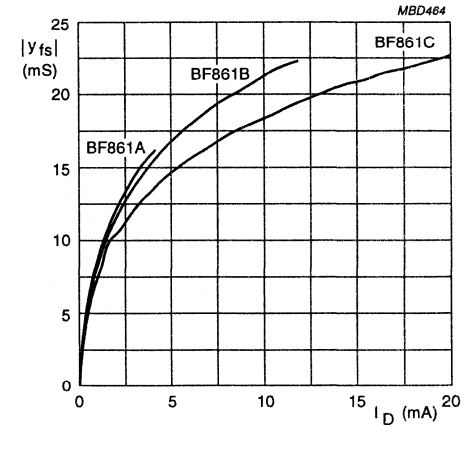
V_{DS} = 8 V.
V_{GS} = 0.

Fig.4 Common-source output conductance as a function of drain current; typical values.



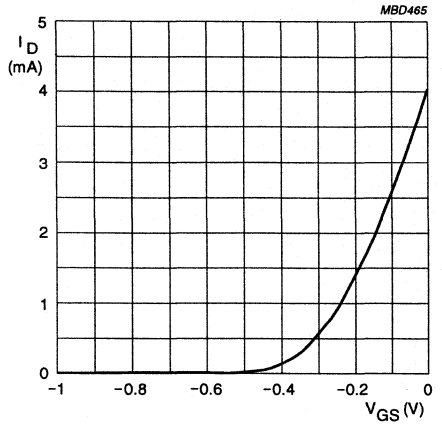
V_{DS} = 8 V.
V_{GS} = 0.

Fig.5 Forward transfer admittance as a function of drain current; typical values.



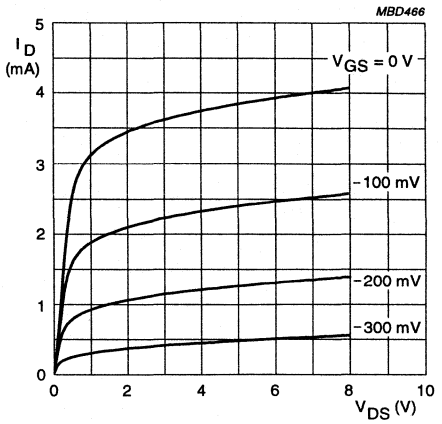
V_{DS} = 8 V.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



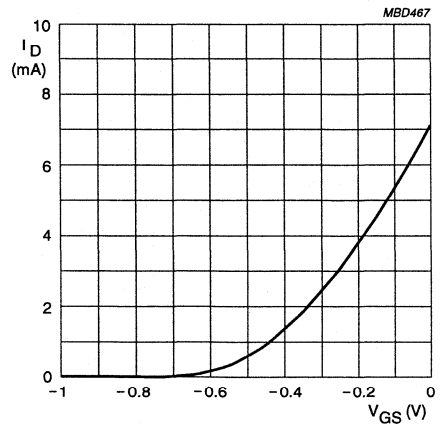
BF861A
V_{DS} = 8 V.

Fig.7 Typical input characteristics.



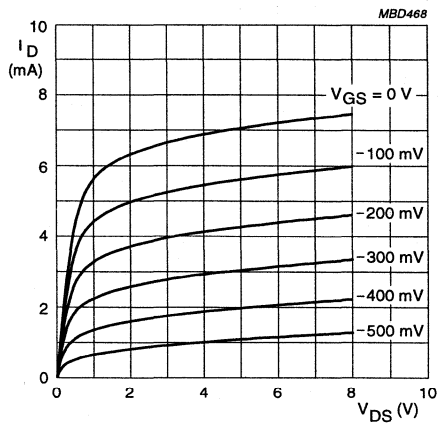
BF861A
V_{DS} = 8 V.

Fig.8 Typical output characteristics.



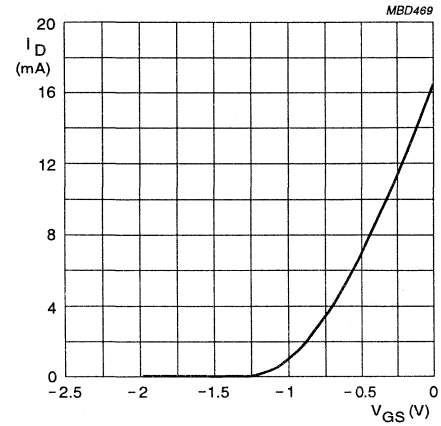
BF861B
V_{DS} = 8 V.

Fig.9 Typical input characteristics.



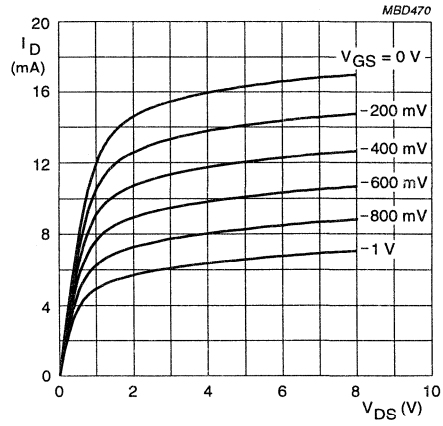
BF861B
V_{DS} = 8 V.

Fig.10 Typical output characteristics.



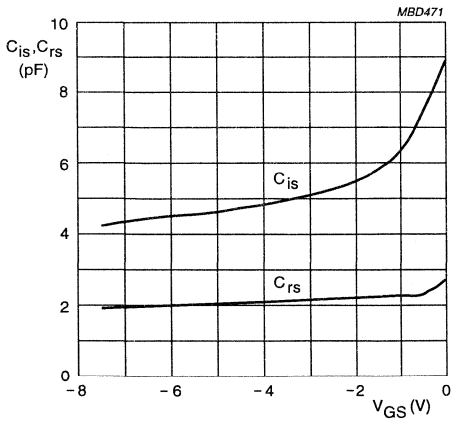
BF861C
V_{DS} = 8 V.

Fig.11 Typical input characteristics.



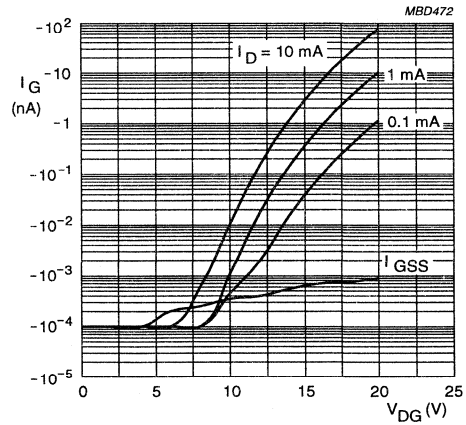
BF861C
V_{DS} = 8 V.

Fig.12 Typical output characteristics.



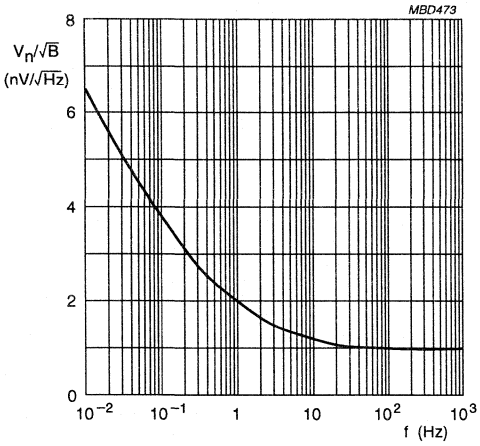
V_{DS} = 8 V.
f = 1 MHz.

Fig.13 Input and reverse transfer capacitance as functions of gate-source voltage; typical values.



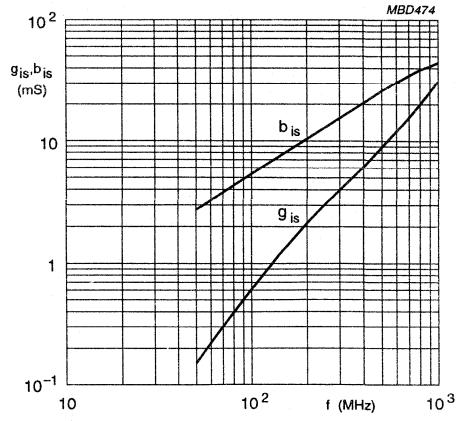
V_{DS} = 8 V.

Fig.14 Gate current as a function of drain-gate voltage; typical values.



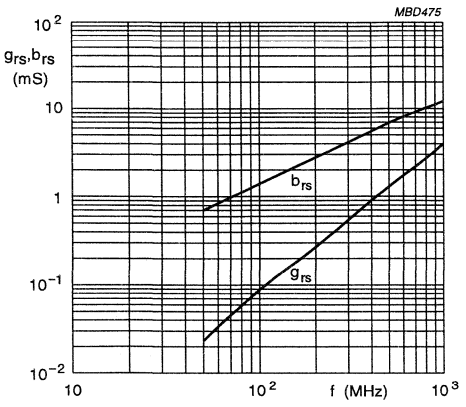
V_{DS} = 8 V.
V_{GS} = 0.

Fig.15 Equivalent input noise as a function of frequency; typical values.



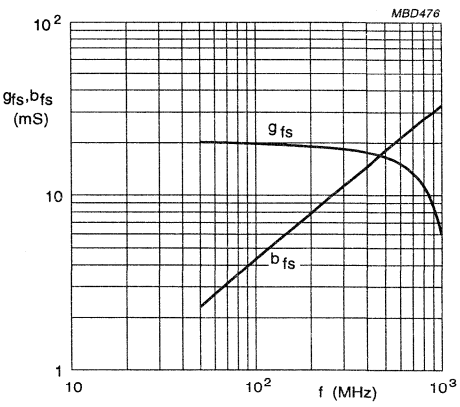
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.16 Common-source input admittance; typical values.



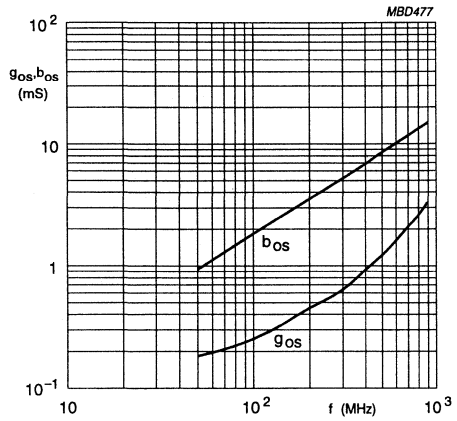
V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.17 Common-source reverse admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.18 Common-source forward transfer admittance; typical values.



V_{DS} = 8 V.
V_{GS} = 0.
T_{amb} = 25 °C.

Fig.19 Common-source output admittance; typical values.

Silicon n-channel dual gate MOS-FETs

BF901; BF901R

FEATURES

- Intended for low voltage operation
- Short channel transistor with high ratio $|Y_{fs}|:C_{is}$
- Low noise gain-controlled amplifier to 1 GHz
- BF901R has reverse pinning.

DESCRIPTION

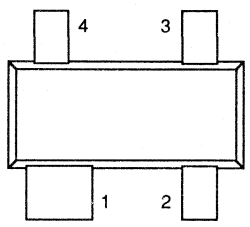
Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes, with source and substrate interconnected. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment especially suited for low voltage operation. These MOS-FET tetrodes are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

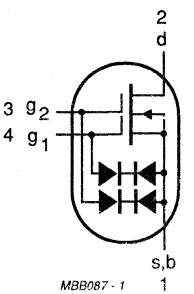
PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

QUICK REFERENCE DATA

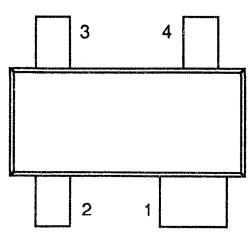
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	12	V
I_D	drain current	–	30	mA
P_{tot}	total power dissipation	–	200	mW
T_j	junction temperature	–	150	°C
$\|Y_{fs}\|$	transfer admittance	28	35	mS
C_{ig1-s}	input capacitance at gate 1	2.35	2.75	pF
C_{rs}	feedback capacitance	25	–	fF
F	noise figure at 800 MHz	1.7	–	dB

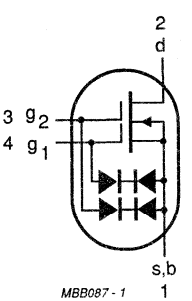




Marking code: MO1.

Fig.1 Simplified outline (SOT143) and symbol.





Marking code: MO2.

Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
V_{D-G2}	drain-gate 2 voltage		–	6	V
I_D	DC drain current		–	30	mA
$\pm I_{G1-S}$	gate 1-source current		–	10	mA
$\pm I_{G2-S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF901	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF901R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	thermal resistance from junction to ambient (note 1)	
	BF901	500 K/W
	BF901R	550 K/W

Note

1. Device mounted on an FR4 printboard.

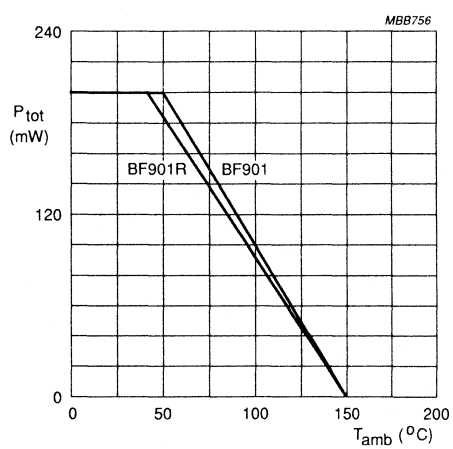


Fig.3 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS} = 0$	–	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS} = 0$	–	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	6	20	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	I_D = 20 µA; V_{DS} = 8 V; V_{G2-S} = 4 V	0	0.7	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	I_D = 20 µA; V_{DS} = 8 V; $V_{G1-S} = 0$	0.3	1	V
I_{DSX}	drain-source current	V_{DS} = 4 V; V_{G1-S} = 1.1 V; V_{G2-S} = 3.4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 14 mA; V_{DS} = 5 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	pulsed; T_j = 25 °C	25	28	35	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	–	2.35	2.75	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_s = 2 mS; $B_s = B_{sopt.}$	–	0.7	–	dB
		f = 800 MHz; G_s = 3.3 mS; $B_s = B_{sopt.}$	–	1.7	–	dB

N-channel dual gate MOS-FETs BF904; BF904R

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

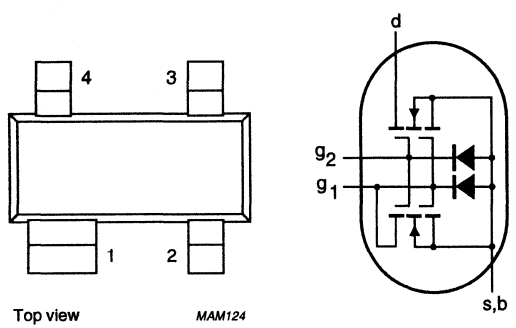
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 and SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

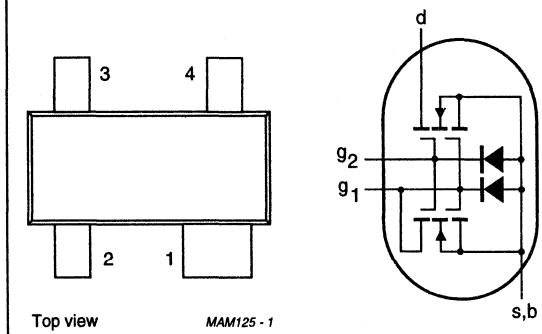
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF904 marking code: M04.

Fig.1 Simplified outline (SOT143) and symbol.



BF904R marking code: M06.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF904	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF904R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

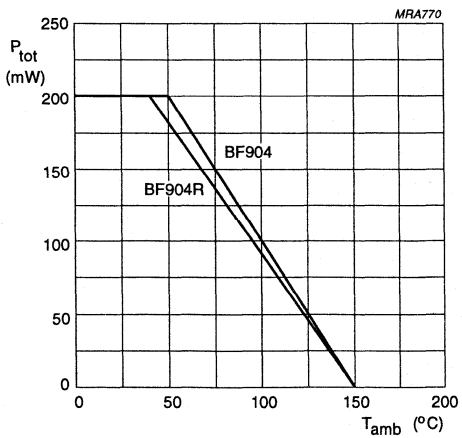


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF904		500	K/W
	BF904R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF904	T_s = 92 °C	290	K/W
	BF904R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = V_{DS} = 5 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	50	nA

Note

1. R_G connects gate 1 to V_{GG} = 5 V; see Fig.20.

DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.2	2.6	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1	1.5	2	pF
C_{os}	drain-source capacitance	f = 1 MHz	1	1.3	1.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	1	1.5	dB
		f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	2	2.8	dB

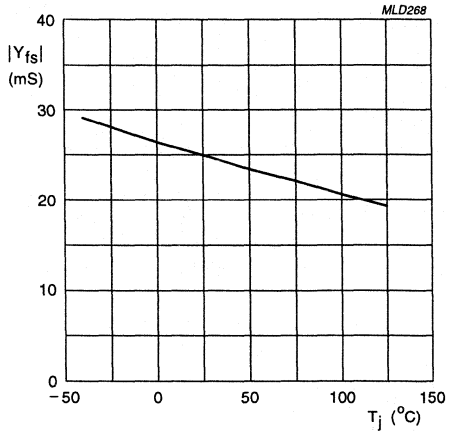
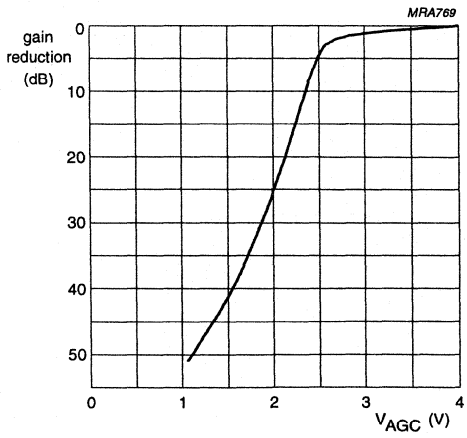
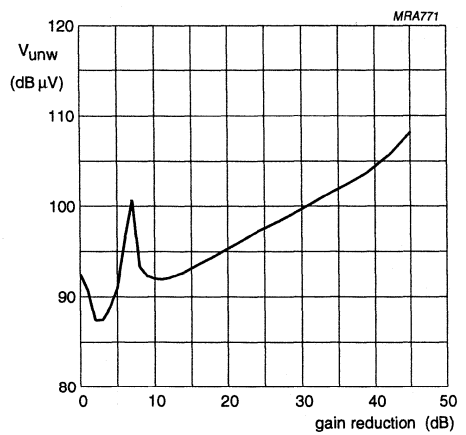


Fig.4 Transfer admittance as a function of the junction temperature; typical values.



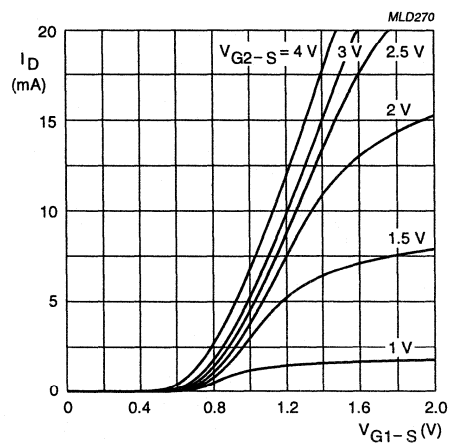
f = 50 MHz.

Fig.5 Typical gain reduction as a function of the AGC voltage.



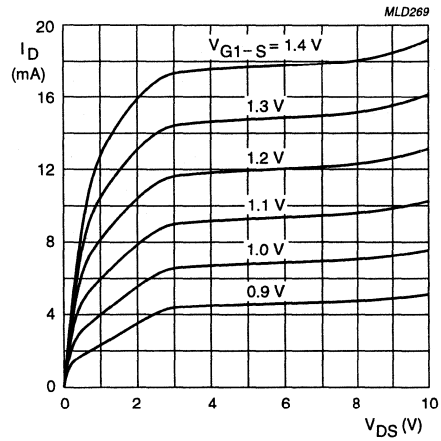
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.20.



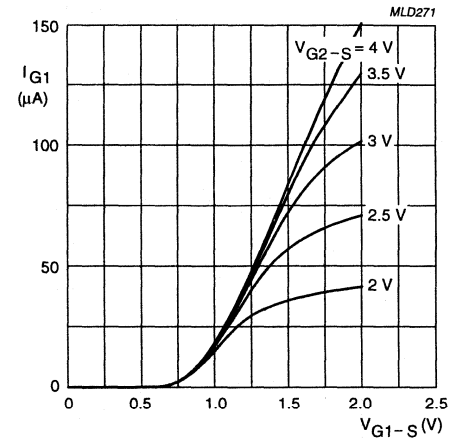
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



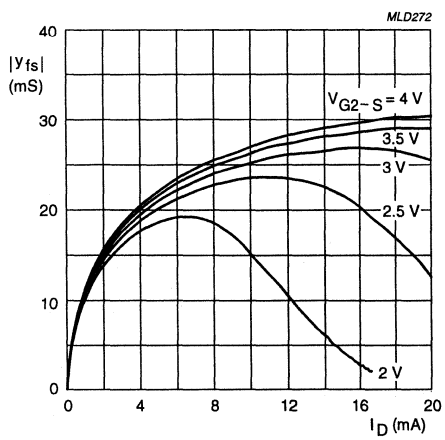
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.8 Output characteristics; typical values.



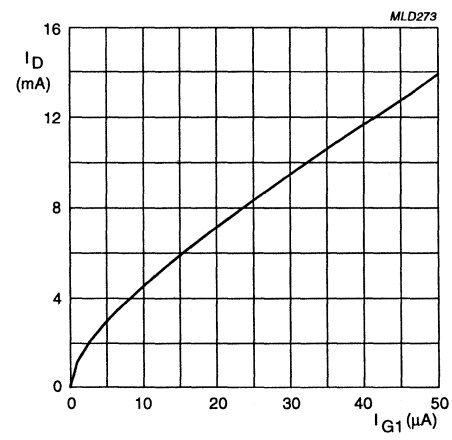
V_{DS} = 5 V.
T_j = 25 °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



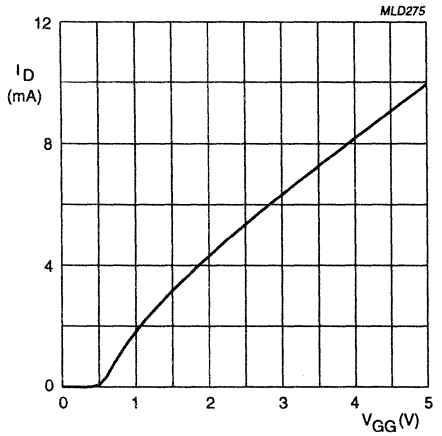
V_{DS} = 5 V.
T_j = 25 °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.



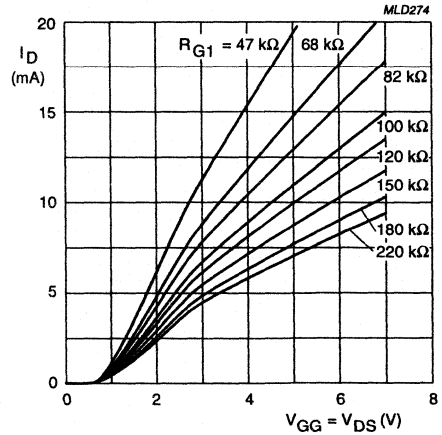
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 current; typical values.



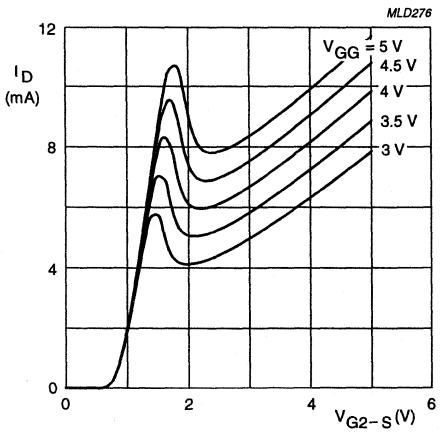
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.20.



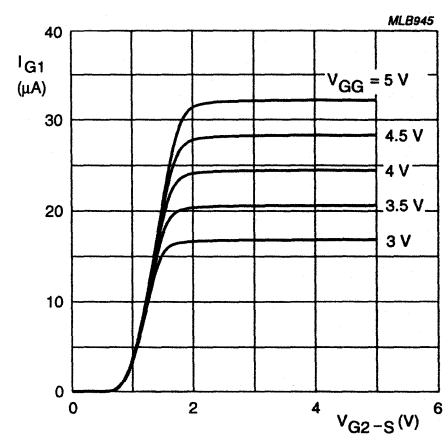
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.20.



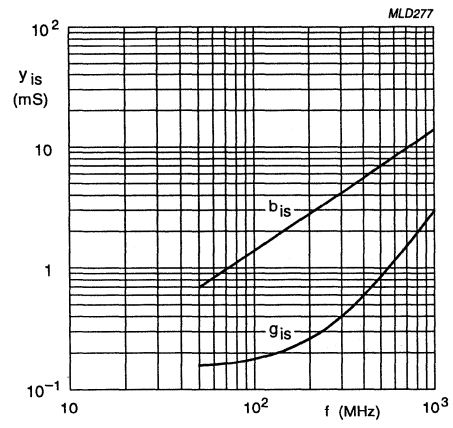
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.14 Drain current as a function of gate 2 voltage; typical values; see Fig.20.



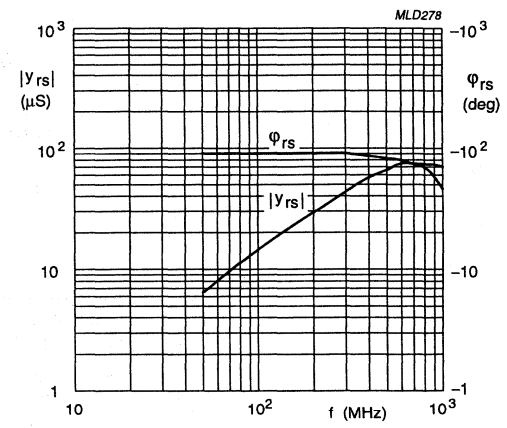
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.20.



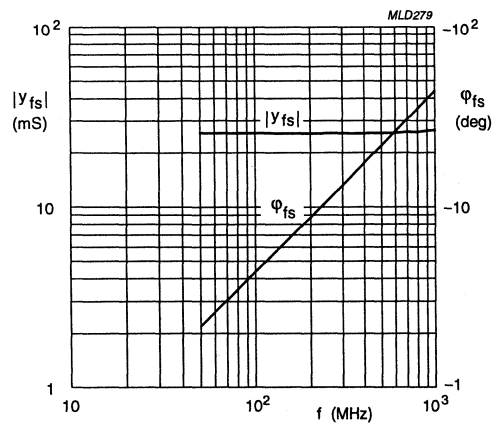
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Input admittance as a function of frequency; typical values.



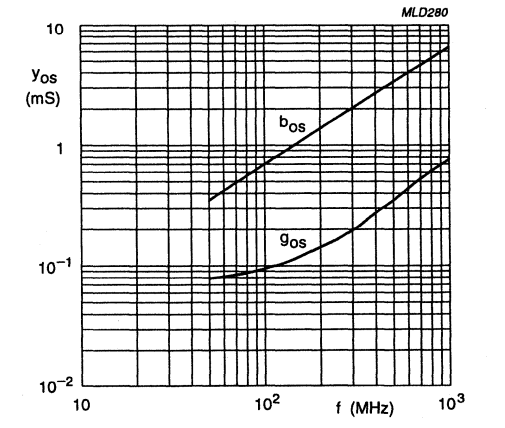
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.17 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.18 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.19 Output admittance as a function of frequency; typical values.

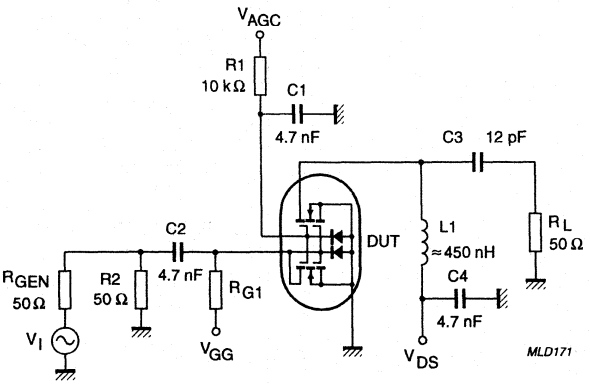


Fig.20 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} =5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	−3.4	2.420	175.7	0.000	79.9	0.993	−1.6
100	0.985	−8.3	2.414	169.1	0.001	78.3	0.992	−3.9
200	0.976	−16.4	2.368	158.8	0.003	80.3	0.987	−7.8
300	0.958	−24.1	2.301	148.5	0.004	73.7	0.980	−11.4
400	0.942	−32.0	2.251	138.8	0.005	70.7	0.974	−15.2
500	0.918	−39.3	2.170	129.5	0.005	67.2	0.966	−18.7
600	0.899	−46.0	2.080	120.7	0.005	67.8	0.958	−22.2
700	0.876	−52.6	2.001	112.1	0.005	68.6	0.951	−25.5
800	0.852	−58.8	1.924	103.2	0.005	72.9	0.944	−28.9
900	0.823	−64.9	1.829	94.7	0.005	78.7	0.937	−32.1
1000	0.800	−70.9	1.747	86.5	0.005	88.3	0.933	−35.2
1200	0.750	−82.4	1.621	70.7	0.005	120.5	0.928	−41.7
1400	0.719	−92.7	1.535	54.6	0.008	139.8	0.930	−48.4
1600	0.682	−102.5	1.424	39.4	0.010	137.8	0.924	−54.9
1800	0.642	−109.8	1.349	22.5	0.013	156.8	0.928	−62.9
2000	0.602	−116.5	1.283	1.1	0.018	175.1	0.928	−73.1
2200	0.547	−124.9	1.130	−15.1	0.014	172.6	0.887	−81.0
2400	0.596	−128.7	1.018	−49.1	0.040	−163.9	0.837	−95.8
2600	0.682	−132.6	0.979	−79.4	0.077	−164.0	0.778	−109.6
2800	0.771	−142.5	0.804	−116.2	0.120	178.8	0.629	−119.5
3000	0.793	−157.5	0.541	−153.5	0.149	158.3	0.479	−119.9

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	o.686	49.6	50.40

N-channel dual-gate MOS-FET BF904WR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

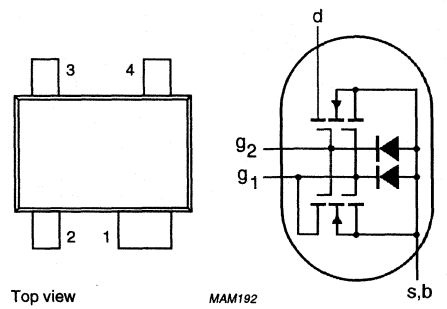
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MC.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C; see Fig.2; note 1	–	280	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

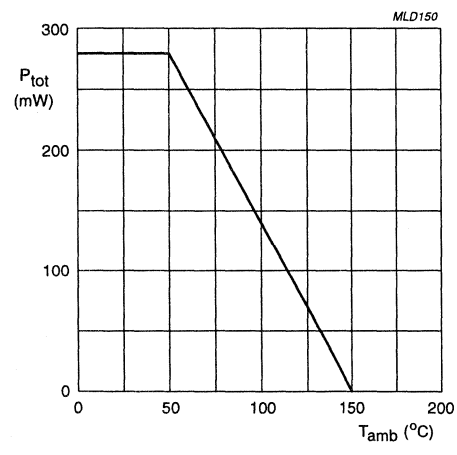


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4V; V_{DS} = 5 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = V_{DS} = 5 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	50	nA

Note

1. R_G connects gate 1 to V_{GG} = 5 V.

DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	30	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.2	2.6	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1	1.5	2	pF
C_{os}	drain-source capacitance	f = 1 MHz	1	1.3	1.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	1	1.5	dB
		f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	2	2.8	dB

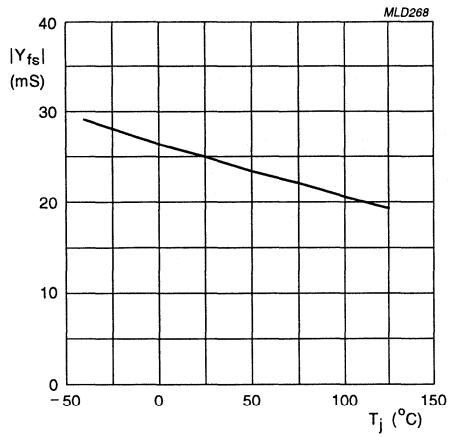
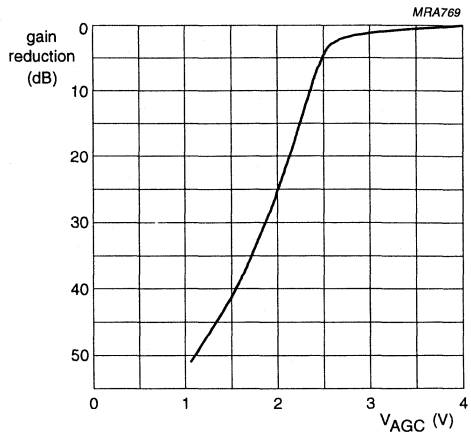
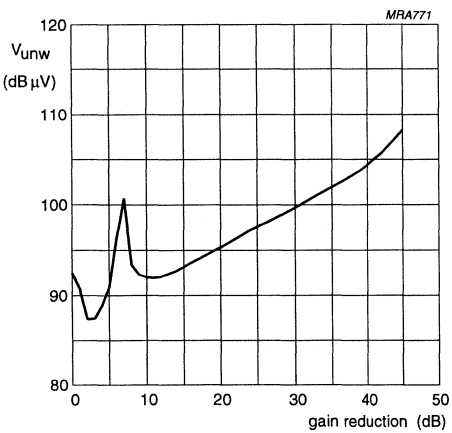


Fig.3 Forward transfer admittance as a function of junction temperature; typical values.



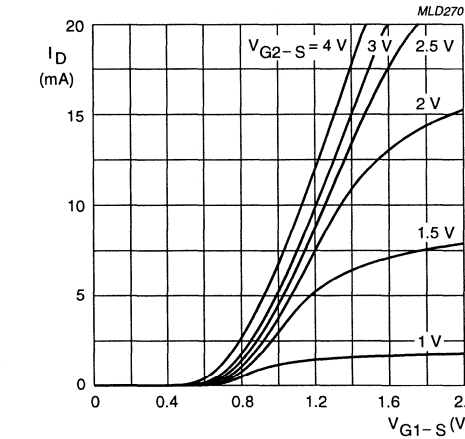
f = 50 MHz.
T_j = 25 °C.

Fig.4 Typical gain reduction as a function of AGC voltage.



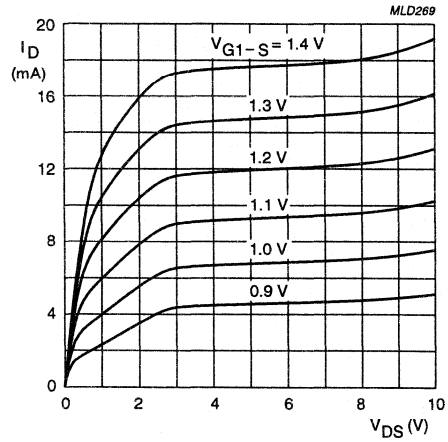
V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.5 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.19.



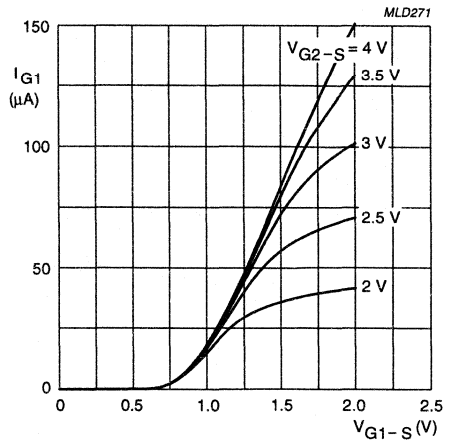
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Transfer characteristics; typical values.



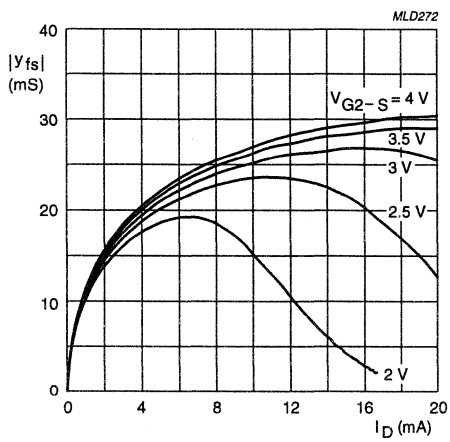
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.7 Output characteristics; typical values.



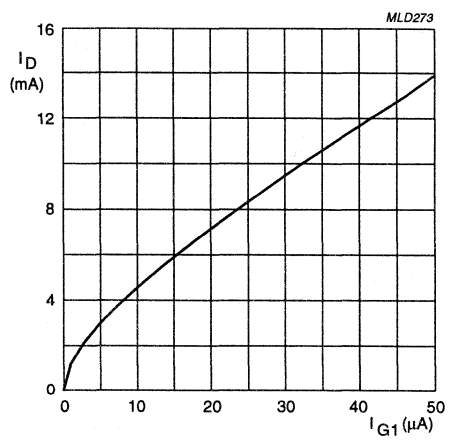
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Gate 1 current as a function of gate 1 voltage; typical values.



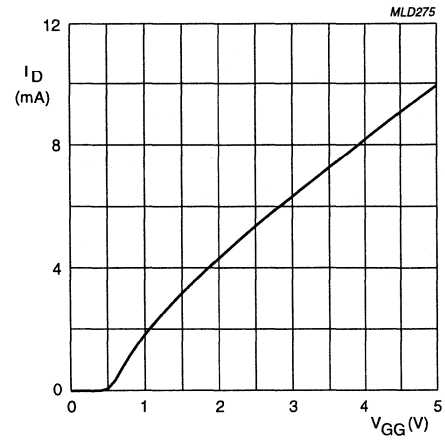
V_{DS} = 5 V.
T_j = 25 °C.

Fig.9 Forward transfer admittance as a function of drain current; typical values.



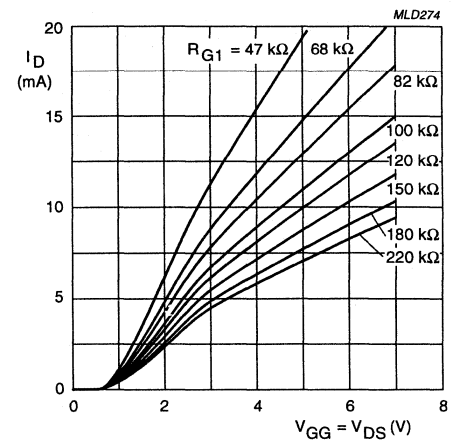
V_{DS} = 5 V; V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



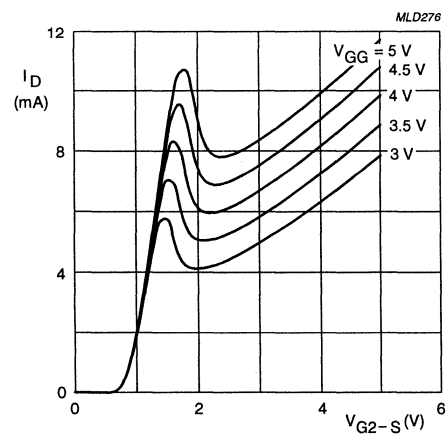
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.19.



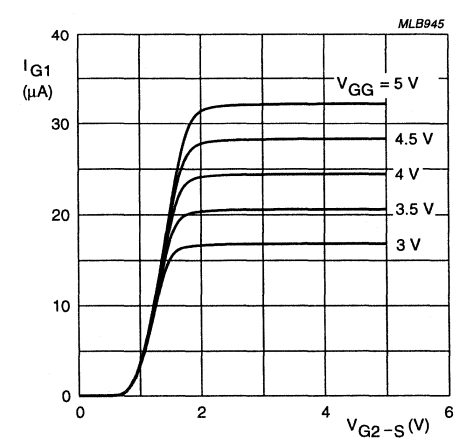
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.19.



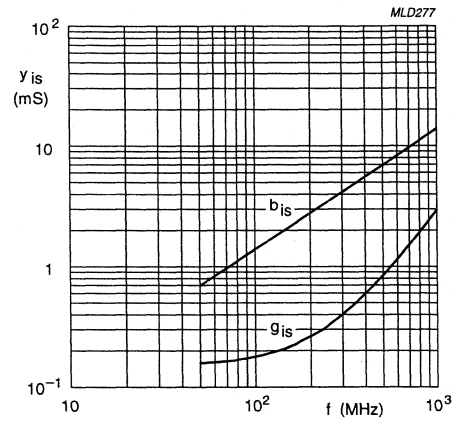
V_{DS} = 5 V; T_j = 25 °C.
R_G = 120 kΩ (connected to V_{GG}).

Fig.13 Drain current as a function of gate 2 voltage; typical values; see Fig.19.



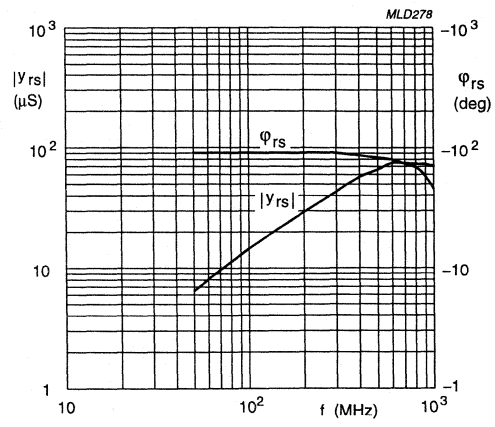
V_{DS} = 5 V; T_j = 25 °C.
R_G = 120 kΩ (connected to V_{GG}).

Fig.14 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.19.



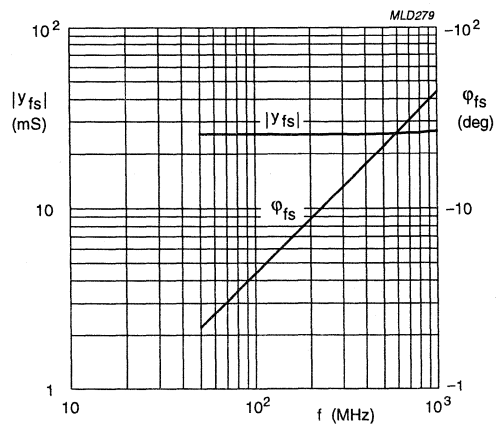
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.15 Input admittance as a function of frequency; typical values.



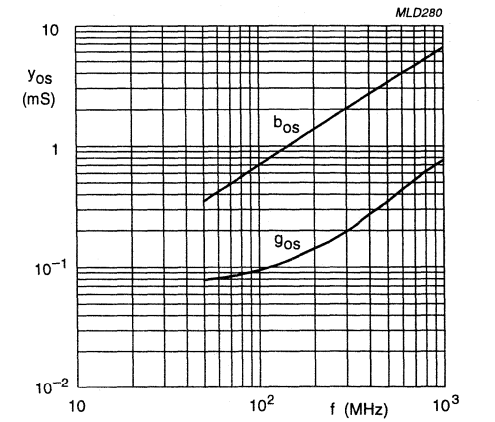
V_{DS} = 5 V; V_{G2} = 4 V.
I_D =10 mA; T_{amb} = 25 °C.

Fig.16 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.17 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.18 Output admittance as a function of frequency; typical values.

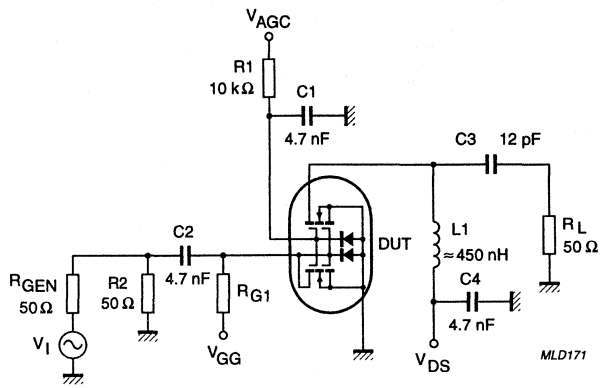


Fig.19 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} =5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	–3.4	2.420	175.7	0.000	79.9	0.993	–1.6
100	0.985	–8.3	2.414	169.1	0.001	78.3	0.992	–3.9
200	0.976	–16.4	2.368	158.8	0.003	80.3	0.987	–7.8
300	0.958	–24.1	2.301	148.5	0.004	73.7	0.980	–11.4
400	0.942	–32.0	2.251	138.8	0.005	70.7	0.974	–15.2
500	0.918	–39.3	2.170	129.5	0.005	67.2	0.966	–18.7
600	0.899	–46.0	2.080	120.7	0.005	67.8	0.958	–22.2
700	0.876	–52.6	2.001	112.1	0.005	68.6	0.951	–25.5
800	0.852	–58.8	1.924	103.2	0.005	72.9	0.944	–28.9
900	0.823	–64.9	1.829	94.7	0.005	78.7	0.937	–32.1
1000	0.800	–70.9	1.747	86.5	0.005	88.3	0.933	–35.2
1200	0.750	–82.4	1.621	70.7	0.005	120.5	0.928	–41.7
1400	0.719	–92.7	1.535	54.6	0.008	139.8	0.930	–48.4
1600	0.682	–102.5	1.424	39.4	0.010	137.8	0.924	–54.9
1800	0.642	–109.8	1.349	22.5	0.013	156.8	0.928	–62.9
2000	0.602	–116.5	1.283	1.1	0.018	175.1	0.928	–73.1
2200	0.547	–124.9	1.130	–15.1	0.014	172.6	0.887	–81.0
2400	0.596	–128.7	1.018	–49.1	0.040	–163.9	0.837	–95.8
2600	0.682	–132.6	0.979	–79.4	0.077	–164.0	0.778	–109.6
2800	0.771	–142.5	0.804	–116.2	0.120	178.8	0.629	–119.5
3000	0.793	–157.5	0.541	–153.5	0.149	158.3	0.479	–119.9

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	.686	49.6	50.40

Dual gate MOS-FETs

BF908; BF908R

FEATURES

- High $|Y_{fs}|$ dual gate MOS-FET
- Short channel transistor with high $|Y_{fs}| : C_{is}$ ratio
- Low noise gain-controlled amplifier to 1 GHz

DESCRIPTION

Depletion type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes. They are intended for UHF and VHF applications with 12 V supply voltage such as television tuners and professional communications equipment. These transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

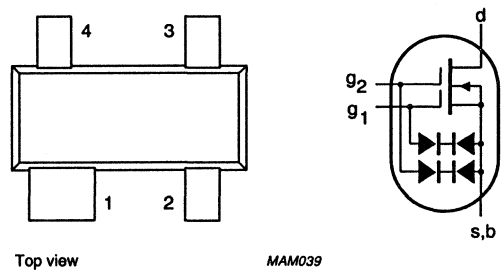
PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

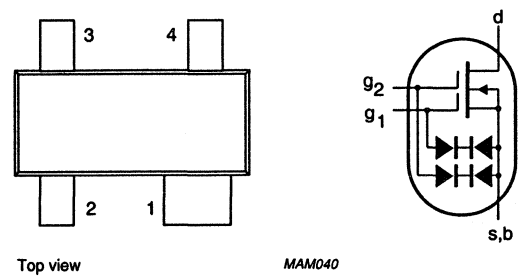
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	–	12	V
I_D	drain current	–	–	40	mA
P_{tot}	total power dissipation	–	–	200	mW
T_j	junction temperature	–	–	150	°C
$\|Y_{fs}\|$	transfer admittance	36	43	50	mS
C_{ig1-s}	input capacitance at gate 1	2.4	3.1	4	fF
C_{rs}	feedback capacitance	20	30	45	pF
F	noise figure at 800 MHz	–	1.5	2.5	dB



BF908

Fig.1 Simplified outline (SOT143) and symbol.



BF908R

Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	DC drain current		–	40	mA
$\pm I_{G1-S}$	gate 1-source current		–	10	mA
$\pm I_{G2-S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF908	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF908R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	
	BF908	500 K/W
	BF908R	550 K/W

Note

1. Device mounted on a printed-circuit board.

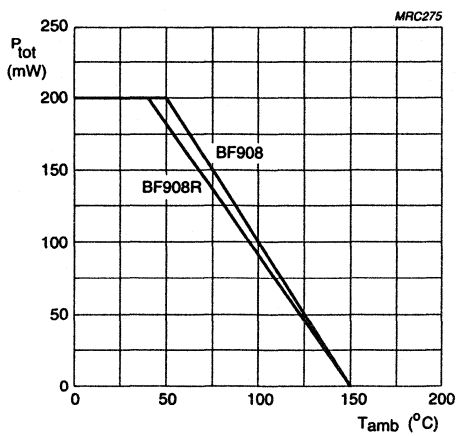


Fig.3 Power derating curve.

STATIC CHARACTERISTICS

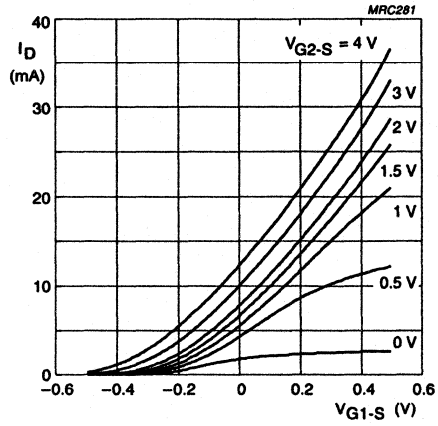
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm I_{G1-S}$	gate 1 cut-off current	V_{G1-S} = 5 V; $V_{G2-S} = V_{DS}$ = 0	–	–	50	nA
$\pm I_{G2-S}$	gate 2 cut-off current	V_{G2-S} = 5 V; $V_{G1-S} = V_{DS}$ = 0	–	–	50	nA
$V_{(BR)G1-S}$	gate 1-source breakdown voltage	I_{G1-S} = 10 mA; $V_{G2-S} = V_{DS}$ = 0	8	–	20	V
$V_{(BR)G2-S}$	gate 2-source breakdown voltage	I_{G2-S} = 10 mA; $V_{G1-S} = V_{DS}$ = 0	8	–	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 μA; V_{DS} = 8 V; V_{G2-S} = 4 V	–	–	2	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 μA; V_{DS} = 8 V; V_{G1-S} = 4 V	–	–	1.5	V
I_{DSS}	drain current	V_{DS} = 8 V; V_{G1-S} = 0; V_{G2-S} = 4 V	3	15	27	mA

DYNAMIC CHARACTERISTICS

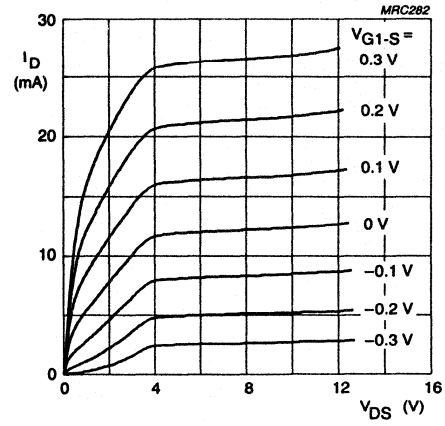
Measuring conditions (common source): I_D = 15 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs}\rvert$	transfer admittance	pulsed; T_j = 25 °C; f = 1 kHz	36	43	50	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	2.4	3.1	4	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	1.2	1.8	2.5	pF
C_{os}	output capacitance	f = 1 MHz	1.2	1.7	2.2	pF
C_{rs}	feedback capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt.}$	–	0.6	1.2	dB
		f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt.}$	–	1.5	2.5	dB



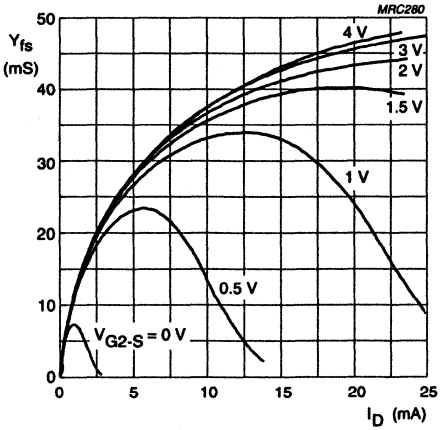
V_{DS} = 8 V; T_j = 25 °C.

Fig.4 Typical transfer characteristics.



V_{G2-S} = 4 V; T_j = 25 °C.

Fig.5 Typical output characteristics.



V_{DS} = 8 V; T_j = 25 °C.

Fig.6 Transfer admittance as a function of drain current, typical values.

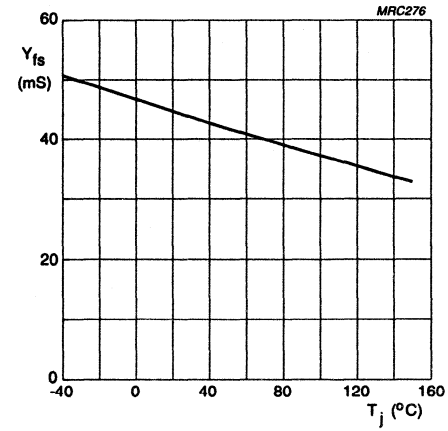


Fig.7 Transfer admittance as a function of junction temperature, typical values.

Table 1 Scattering parameters.
I_D = 10 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)
50	0.998	−5.1	3.537	173.5	0.001	98.2	0.996	−2.4
100	0.994	−10.4	3.502	167.7	0.001	88.8	0.994	−4.9
200	0.979	−20.8	3.450	154.9	0.003	74.6	0.987	−9.5
300	0.962	−30.3	3.318	143.7	0.004	69.5	0.983	−13.9
400	0.939	−40.1	3.234	131.9	0.005	65.6	0.980	−18.5
500	0.914	−49.1	3.093	120.7	0.006	64.4	0.974	−22.8
600	0.892	−57.1	2.912	111.1	0.005	63.1	0.969	−27.0
700	0.865	−64.4	2.774	101.0	0.005	65.2	0.966	−31.2
800	0.837	−71.6	2.616	91.4	0.004	70.8	0.965	−35.4
900	0.811	−78.1	2.479	81.9	0.004	87.4	0.965	−39.4
1000	0.785	−84.5	2.329	72.5	0.003	108.0	0.966	−43.7

Table 2 Noise data.
I_D = 10 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(RAT)	(DEG)	
800	1.50	0.720	56.7	0.580

Table 3 Scattering parameters.
I_D = 15 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)	MAG. (RAT)	ANG. (DEG)
50	0.998	−5.3	3.983	173.4	0.001	95.5	0.994	−2.4
100	0.994	−10.9	3.943	167.5	0.001	93.6	0.991	−5.0
200	0.976	−21.6	3.878	154.7	0.003	74.3	0.984	−9.7
300	0.957	−31.7	3.722	143.3	0.004	70.0	0.979	−14.2
400	0.934	−41.7	3.614	131.6	0.005	63.5	0.975	−18.8
500	0.907	−51.1	3.446	120.4	0.006	62.2	0.969	−23.2
600	0.885	−59.1	3.240	110.9	0.005	59.6	0.964	−27.4
700	0.851	−66.8	3.072	100.9	0.005	64.8	0.961	−31.6
800	0.826	−73.9	2.891	91.3	0.004	67.8	0.959	−35.9
900	0.797	−80.7	2.733	81.9	0.004	85.0	0.958	−40.0
1000	0.773	−87.0	2.569	72.8	0.004	102.9	0.958	−44.2

Table 4 Noise data.
I_D = 15 mA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(RAT)	(DEG)	
800	1.50	0.700	59.2	0.520

N-channel dual-gate MOS-FET BF908WR

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

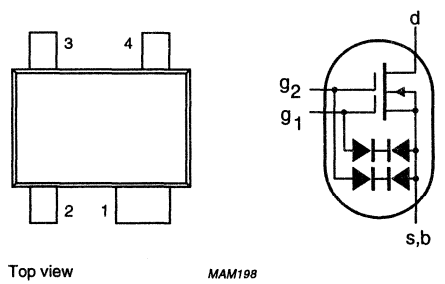
DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT343R package. The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MD.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	300	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		2.4	3.1	4	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 800 MHz	–	1.5	2.5	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 45 °C; see Fig.2; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

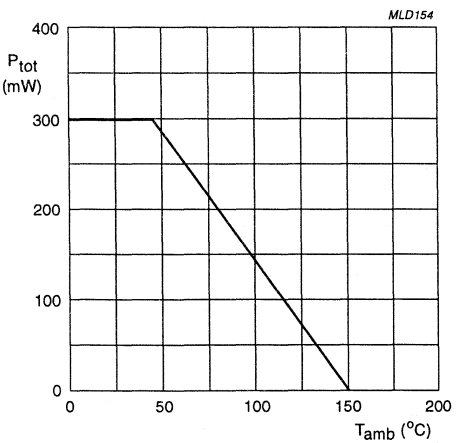


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 87 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

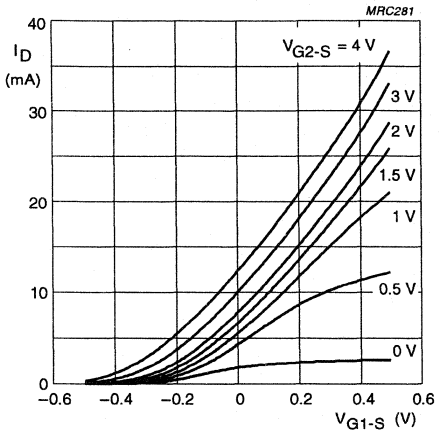
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	8	–	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	8	–	20	V
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 µA	–	–	–2	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 µA	–	–	–1.5	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0	3	15	27	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	–	50	nA

DYNAMIC CHARACTERISTICS

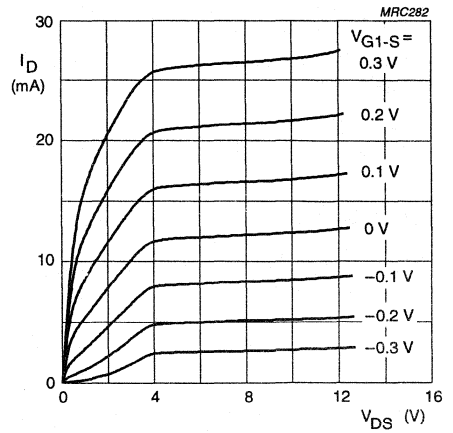
Common source; T_{amb} = 25 °C; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	2.4	3.1	4	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	1.2	1.8	2.5	pF
C_{os}	drain-source capacitance	f = 1 MHz	1.2	1.7	2.2	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	20	30	45	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; B_S = B_{Sopt}	–	0.6	1.2	dB
		f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	1.5	2.5	dB



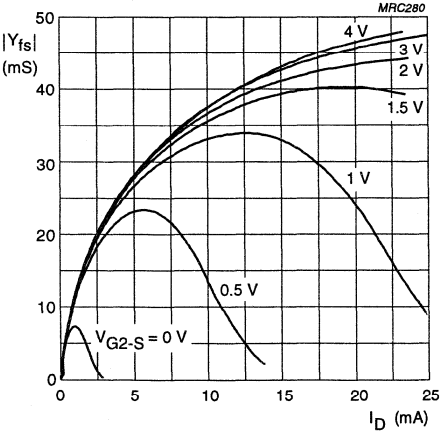
V_{DS} = 8 V.
T_j = 25 °C.

Fig.3 Transfer characteristics; typical values.



V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



V_{DS} = 8 V.
T_j = 25 °C.

Fig.5 Forward transfer admittance as a function of drain current; typical values.

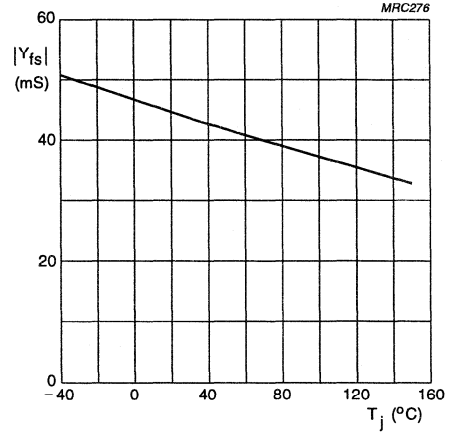


Fig.6 Forward transfer admittance as a function of junction temperature; typical values.

N-channel dual gate MOS-FETs BF909; BF909R

FEATURES

- Specially designed for use at 5 V supply voltage
- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

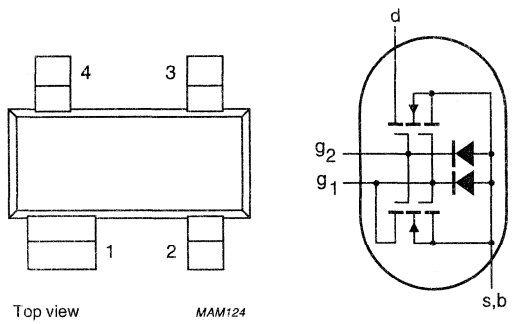
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

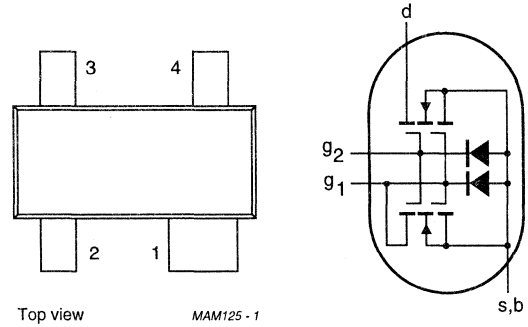
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF909 marking code: M28.

Fig.1 Simplified outline (SOT143) and symbol.



BF909R marking code: M29.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	3.6	4.3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF909	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF909R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

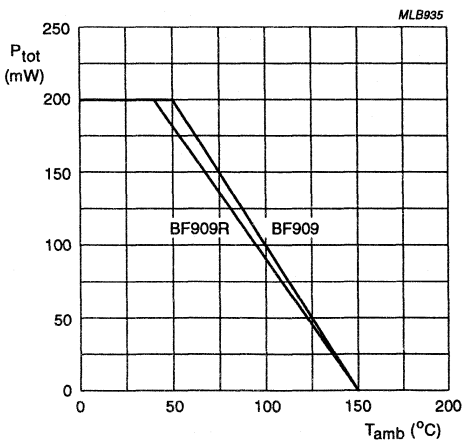


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF909		500	K/W
	BF909R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF909	T_s = 92 °C	290	K/W
	BF909R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = V_{DS} = 5 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	12	20	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S}$ = V_{DS} = 0	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S}$ = V_{DS} = 0	–	50	nA

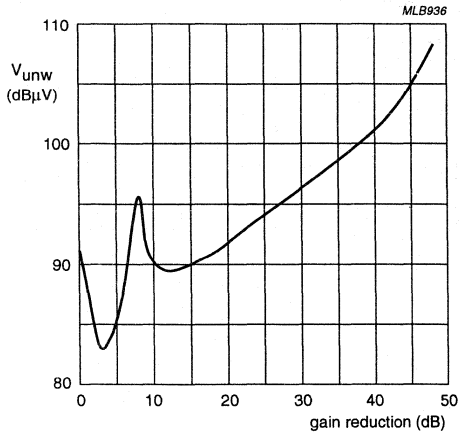
Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V; see Fig.18.

DYNAMIC CHARACTERISTICS

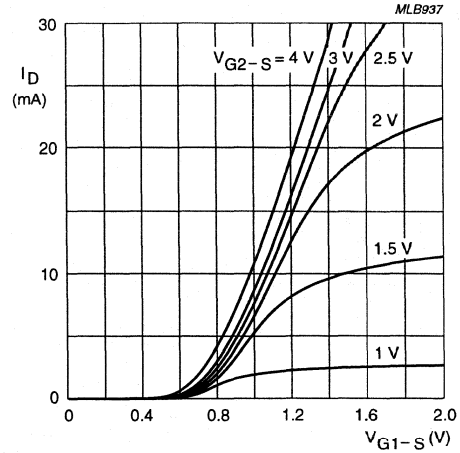
Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	3.6	4.3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	2.3	3	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	2.3	3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	2	2.8	dB



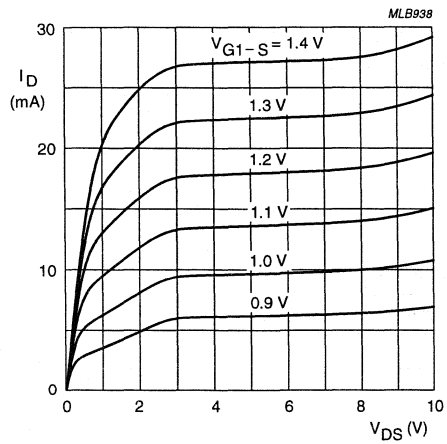
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.4 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.18.



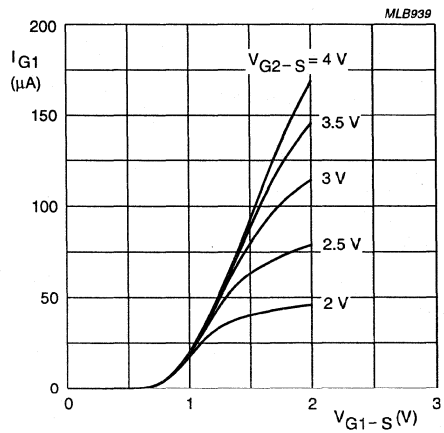
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



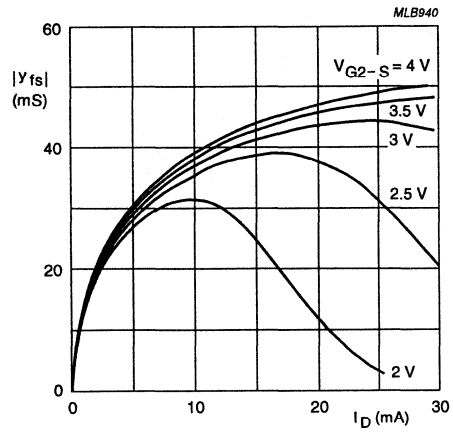
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



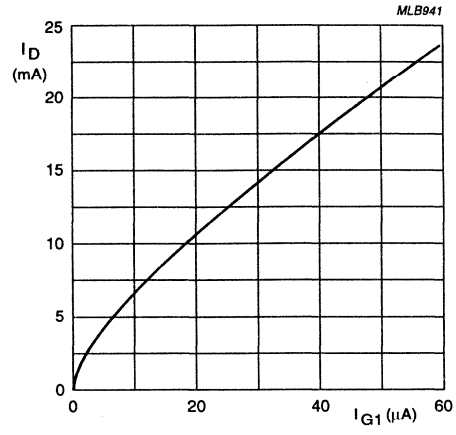
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



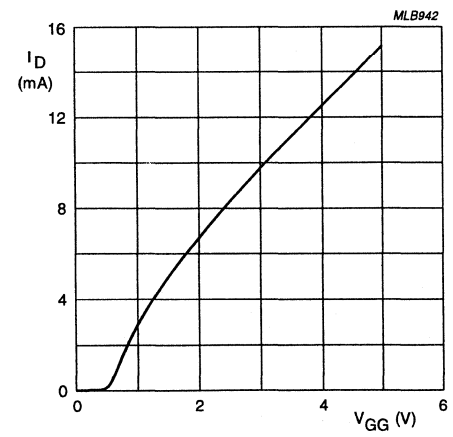
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



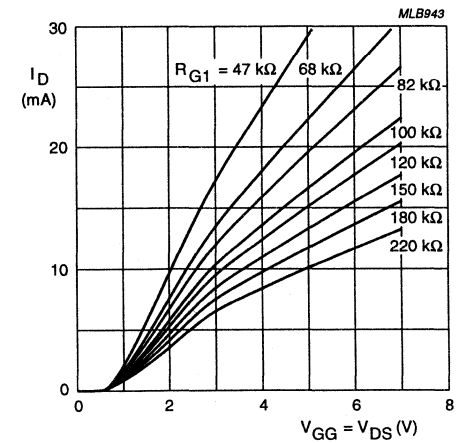
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



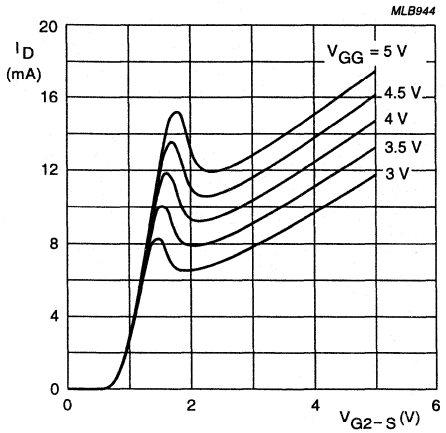
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.18.



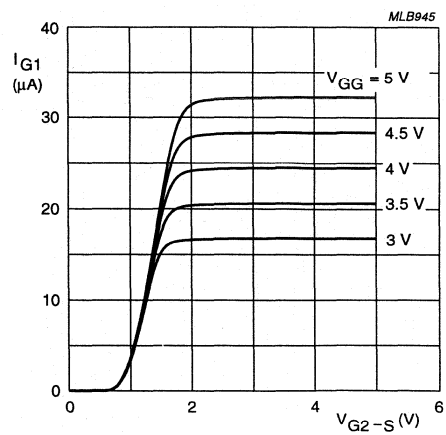
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.18.



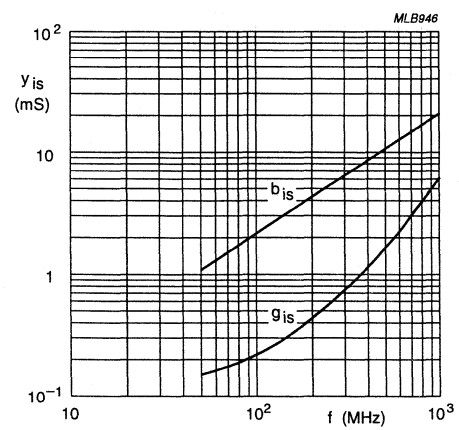
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.12 Drain current as a function of gate 2 voltage; typical values; see Fig.18.



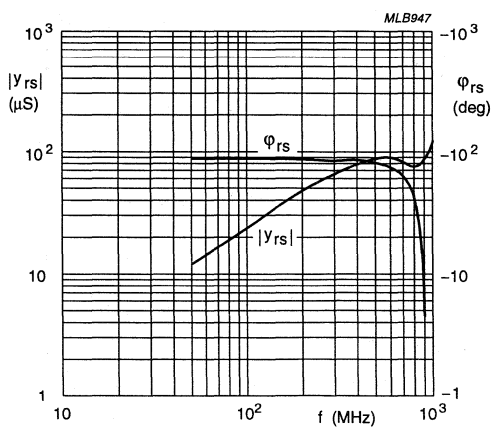
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.18.



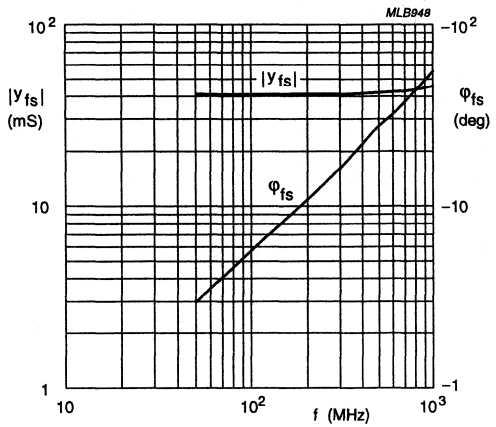
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Input admittance as a function of frequency; typical values.



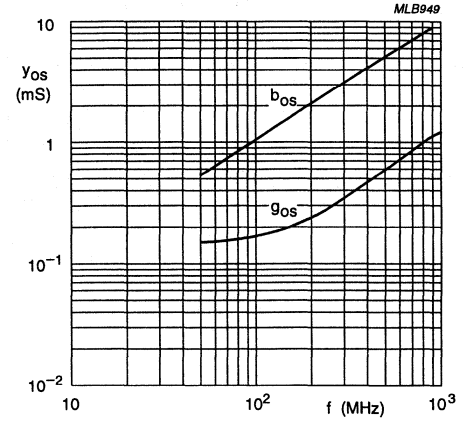
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.17 Output admittance as a function of frequency; typical values.

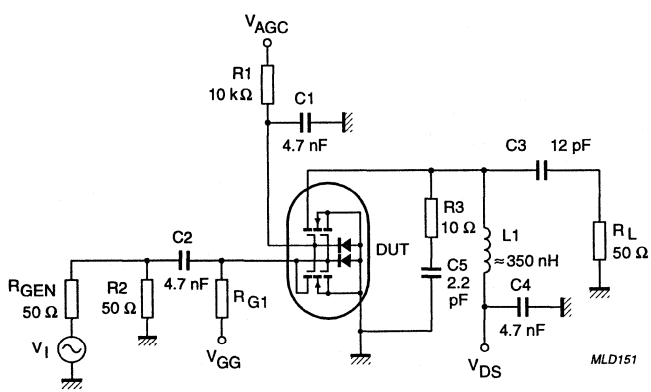


Fig.18 Cross-modulation test set-up.

Table 1 Scattering parameters: T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−6.4	4.064	172.3	0.001	86.9	0.985	−3.2
100	0.978	−12.6	3.997	164.9	0.002	82.7	0.982	−6.4
200	0.957	−25.0	3.886	150.8	0.005	74.3	0.973	−12.6
300	0.931	−36.5	3.682	137.3	0.006	68.9	0.960	−18.6
400	0.899	−47.6	3.484	123.8	0.007	59.6	0.947	−24.2
500	0.868	−57.4	3.260	111.7	0.007	57.9	0.936	−29.6
600	0.848	−66.6	3.053	101.0	0.006	58.5	0.927	−34.8
700	0.816	−74.6	2.829	90.3	0.005	65.5	0.919	−39.8
800	0.792	−82.2	2.652	79.9	0.005	83.3	0.913	−44.6
900	0.772	−89.3	2.470	69.5	0.005	114.9	0.910	−49.5
1000	0.754	−95.6	2.328	59.5	0.006	138.7	0.909	−54.6

Table 2 Noise data: T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

N-channel dual-gate MOS-FET | BF909WR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

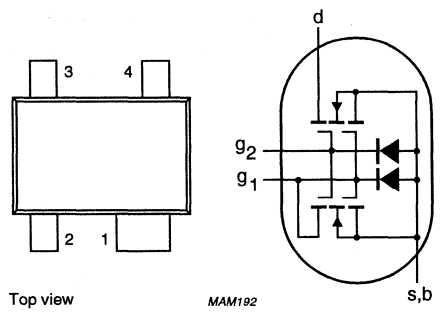
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: ME.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	3.6	4.3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C; see Fig.2; note 1	–	280	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

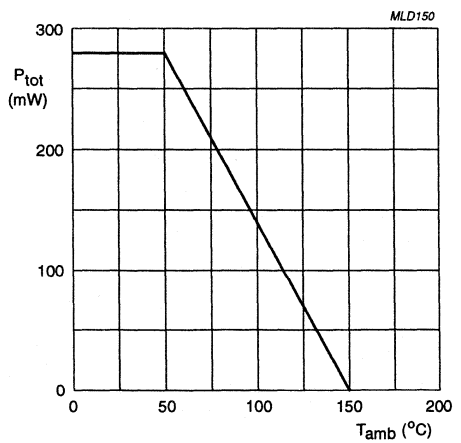


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = V_{DS} = 5 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	12	20	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	50	nA

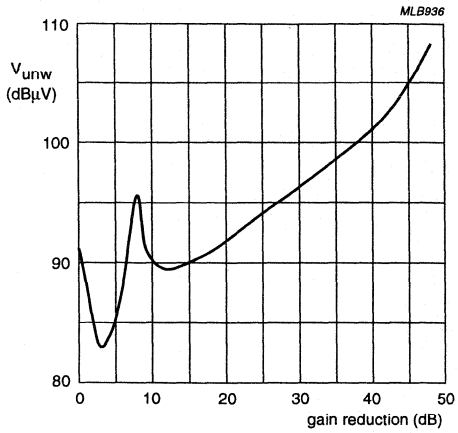
Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V.

DYNAMIC CHARACTERISTICS

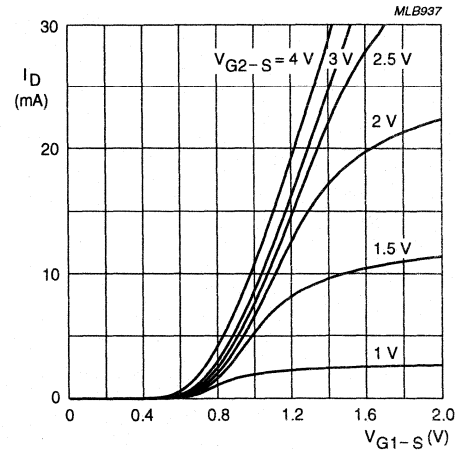
Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	3.6	4.3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	2.3	3	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	2.3	3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	2	2.8	dB



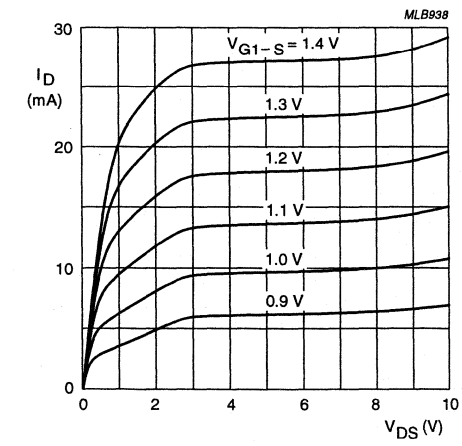
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.3 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.17.



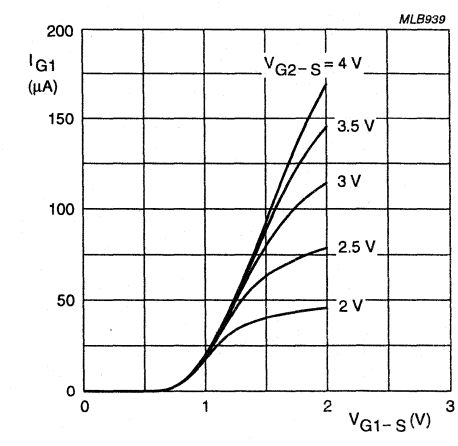
V_{DS} = 5 V.
T_j = 25 °C.

Fig.4 Transfer characteristics; typical values.



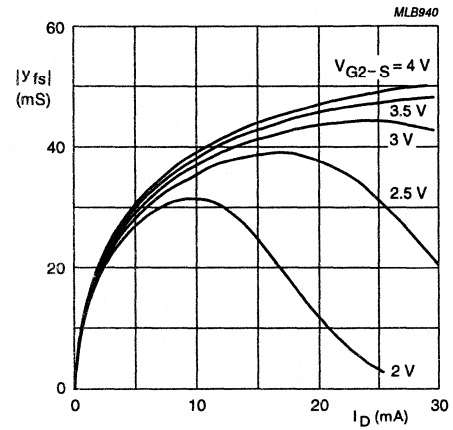
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



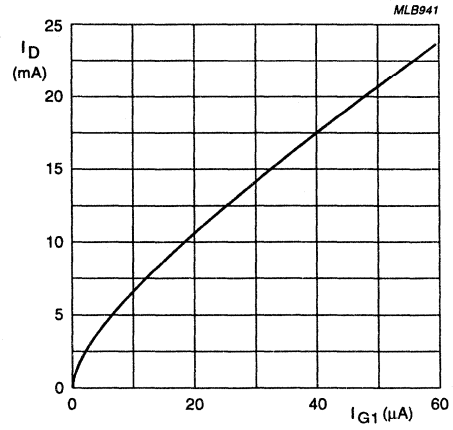
V_{DS} = 5 V.
T_j = 25 °C.

Fig.6 Gate 1 current as a function of gate 1 voltage; typical values.



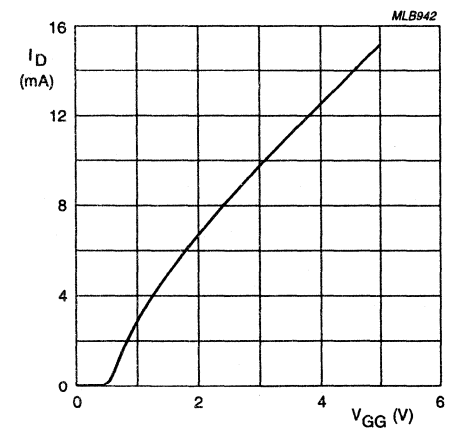
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of drain current; typical values.



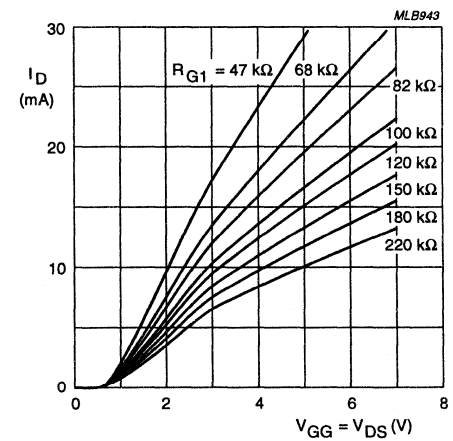
V_{DS} = 5 V.
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.8 Drain current as a function of gate 1 current; typical values.



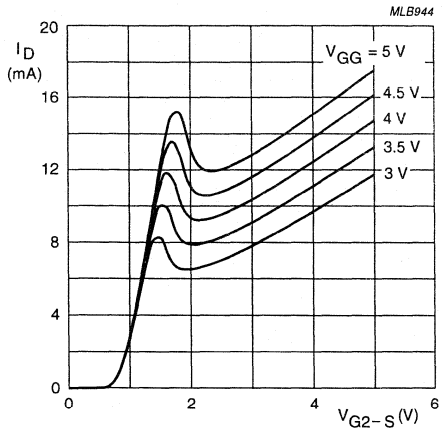
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.17.



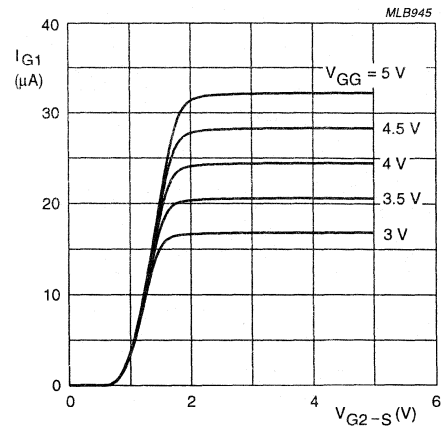
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.17.



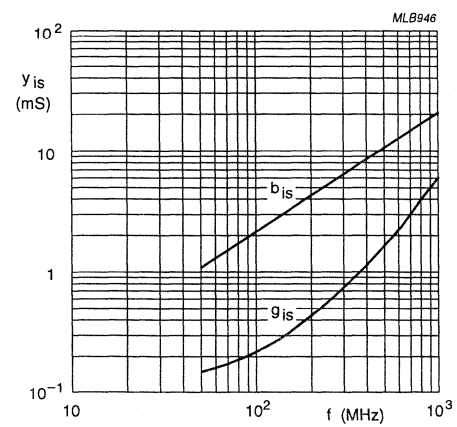
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.11 Drain current as a function of gate 2 voltage; typical values; see Fig.17.



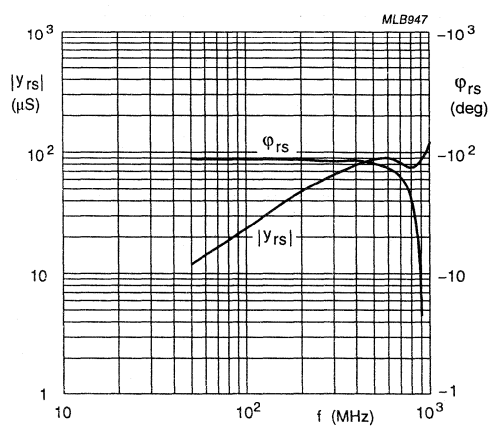
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.12 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.17.



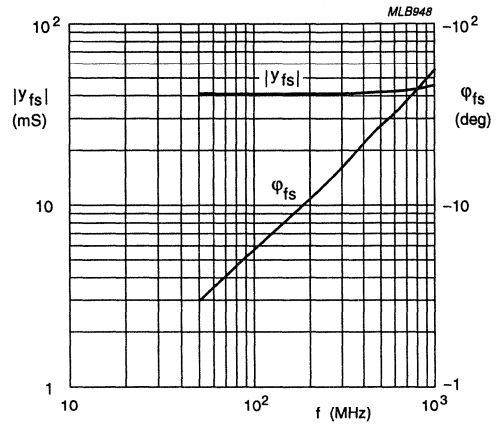
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of frequency; typical values.



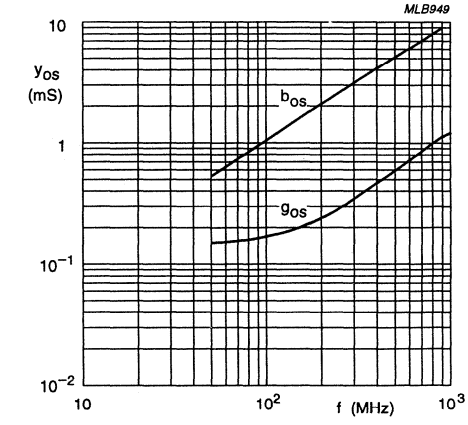
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of frequency; typical values.

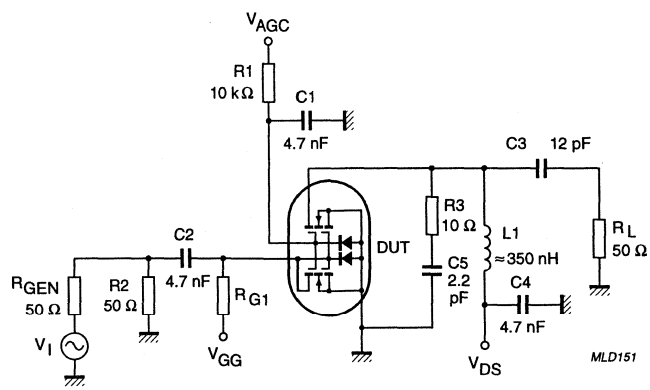


Fig.17 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−6.4	4.064	172.3	0.001	86.9	0.985	−3.2
100	0.978	−12.6	3.997	164.9	0.002	82.7	0.982	−6.4
200	0.957	−25.0	3.886	150.8	0.005	74.3	0.973	−12.6
300	0.931	−36.5	3.682	137.3	0.006	68.9	0.960	−18.6
400	0.899	−47.6	3.484	123.8	0.007	59.6	0.947	−24.2
500	0.868	−57.4	3.260	111.7	0.007	57.9	0.936	−29.6
600	0.848	−66.6	3.053	101.0	0.006	58.5	0.927	−34.8
700	0.816	−74.6	2.829	90.3	0.005	65.5	0.919	−39.8
800	0.792	−82.2	2.652	79.9	0.005	83.3	0.913	−44.6
900	0.772	−89.3	2.470	69.5	0.005	114.9	0.910	−49.5
1000	0.754	−95.6	2.328	59.5	0.006	138.7	0.909	−54.6

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.8 dB

MECHANICAL DATA

Fig.1 SOT143.

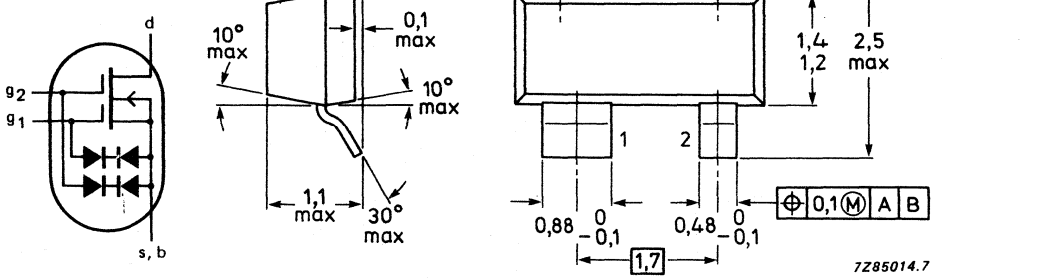
Dimensions in mm

Marking code:

BF989 = MAp

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	20 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

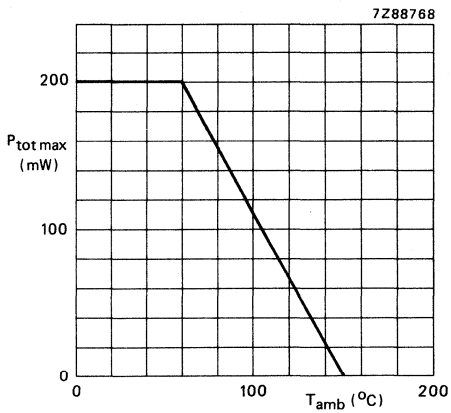


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Drain current			
V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2 to 20 mA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.7 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners with 12 V supply voltage and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ. max.	2.0 dB 3.0 dB

MECHANICAL DATA

Fig.1 SOT143.

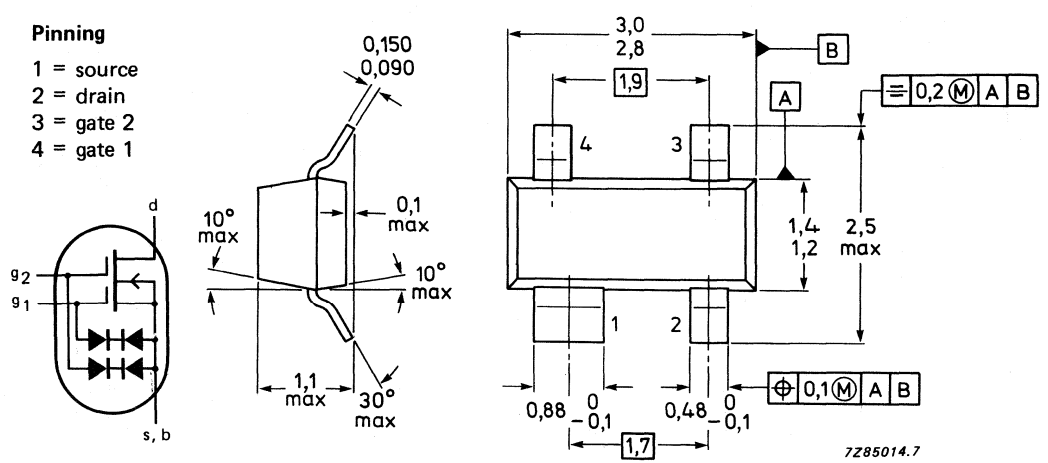
Marking code

BF990A = M87

Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

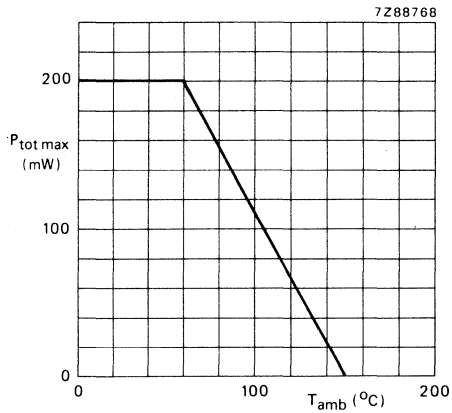


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1;			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
gate 2;			
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1;			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20 V
gate 2;			
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
gate 1;			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	1.3 V
gate 2;			
I_D = 20 μA; V_{DS} = 10 V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 mS 19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.6 pF 3.0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ. max.	2.0 dB 3.0 dB

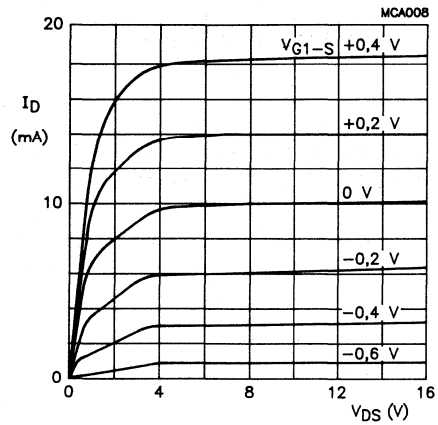


Fig.3 Output characteristics.
V_{G2-S} = 4 V; T_{amb} = 25 °C.

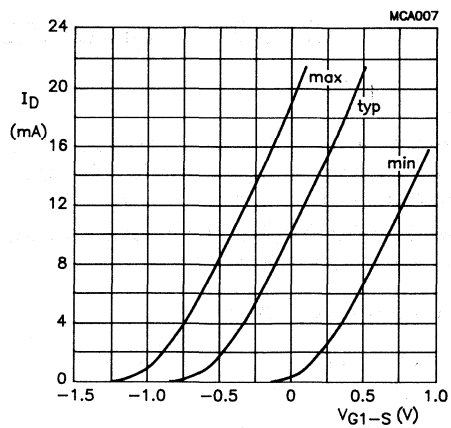


Fig.4 Transfer characteristics.
V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; 3 $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0 dB

MECHANICAL DATA

Fig.1 SOT143R.

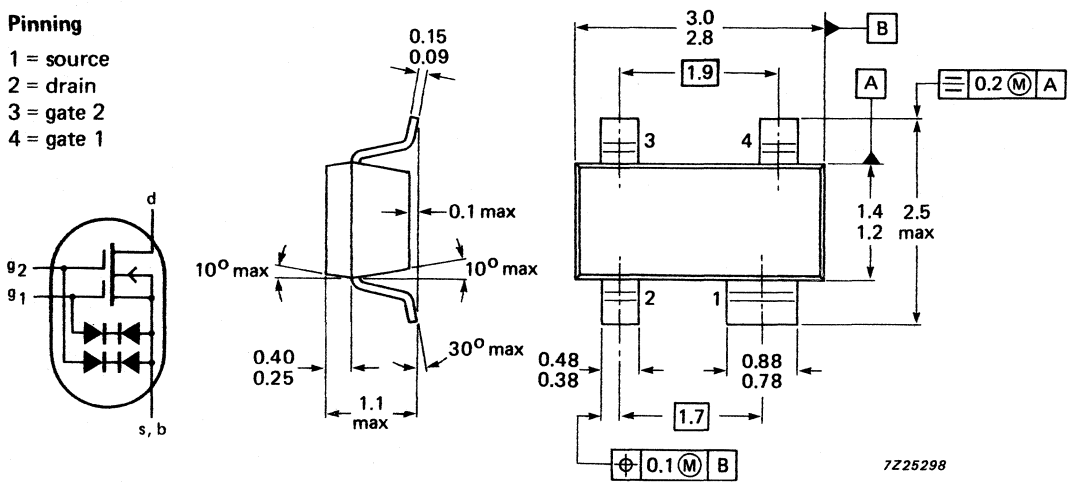
Marking code

BF990AR = M85

Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 50 °C*	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
gate 2; $\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	min.	8 to 20 V
gate 2; $\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	min.	8 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	1.3 V
gate 2; I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 mS 19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.6 pF 3.0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ.	2.0 dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,1 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7 dB

MECHANICAL DATA

Fig.1 SOT143.

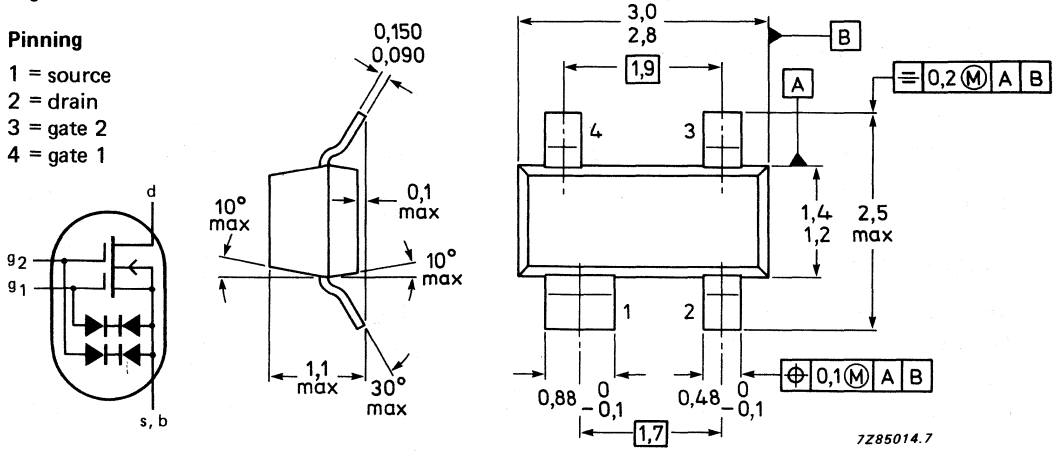
Dimensions in mm

Marking code

BF991 = M91

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	20 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

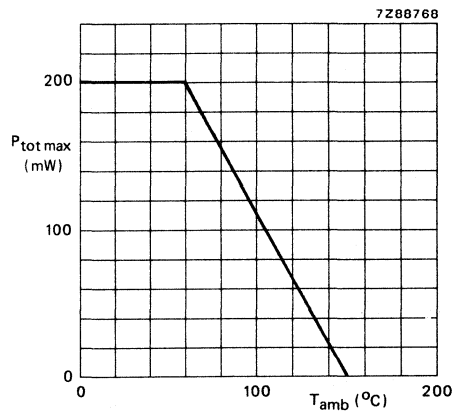


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50 nA
Drain current			
$V_{DS} = 10$ V; $V_{G1-S} = 0$; $+V_{G2-S} = 4$ V	I_{DSS}		4 to 25 mA
Gate-source breakdown voltages			
$\pm I_{G1-SS} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V
Gate-source cut-off voltages			
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	<	2,5 V
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	10 mS
		typ.	14 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,1 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1 pF
Noise figure			
f = 100 MHz; $G_S = 1$ mS; $B_S = B_S$ opt	F	typ.	0,7 dB
		<	1,7 dB
f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt	F	typ.	1,0 dB
		<	2,0 dB
Transducer gain (note 1)			
f = 100 MHz; $G_S = 1$ mS; $B_S = B_S$ opt; $G_L = 0{,}5$ mS; $B_L = B_L$ opt	G_{tr}	typ.	29 dB
f = 200 MHz; $G_S = 2$ mS; $B_S = B_S$ opt; $G_L = 0{,}5$ mS; $B_L = B_L$ opt	G_{tr}	typ.	26 dB

Note

1. Crystal mounted in a SOT103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Fig.1 SOT143.

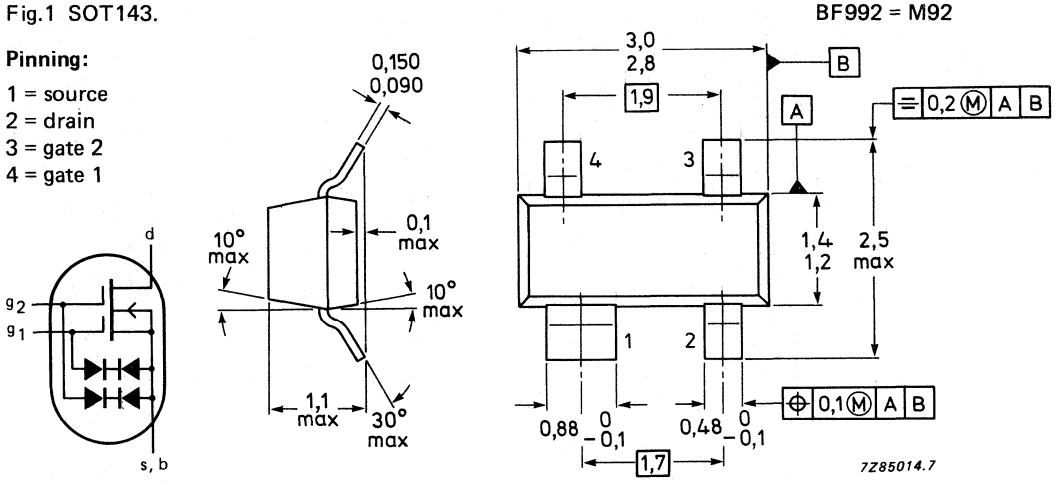
Dimensions in mm

Marking code:

BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

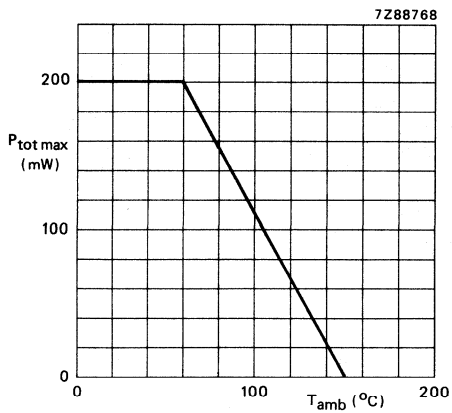


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	25 nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		8 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	20 mS 25 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. max.	30 fF 40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

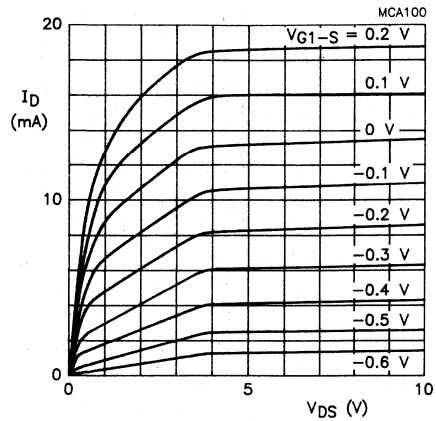


Fig.2 Output characteristics.

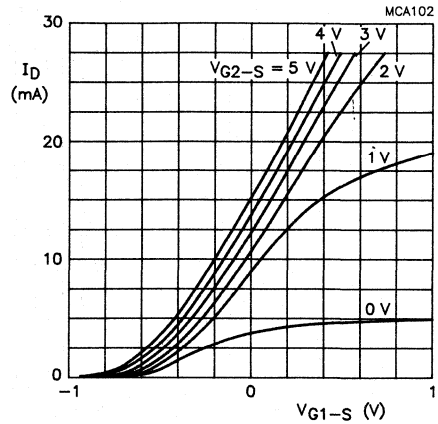


Fig.3 Transfer characteristics.

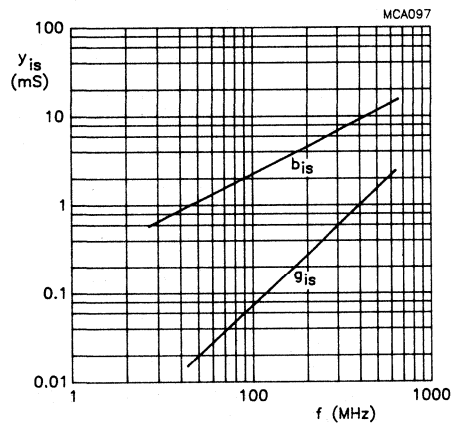


Fig.4 Input admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

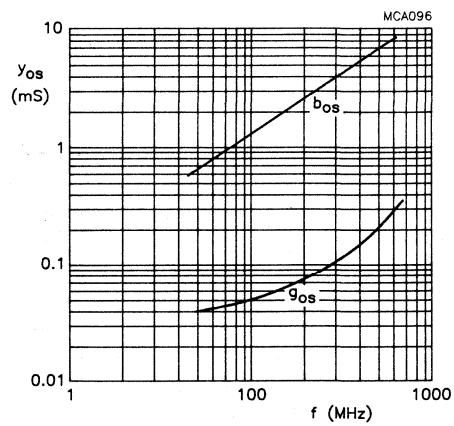


Fig.5 Output admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

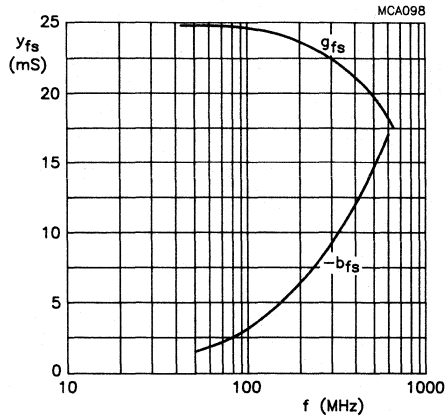


Fig.6 Transfer admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

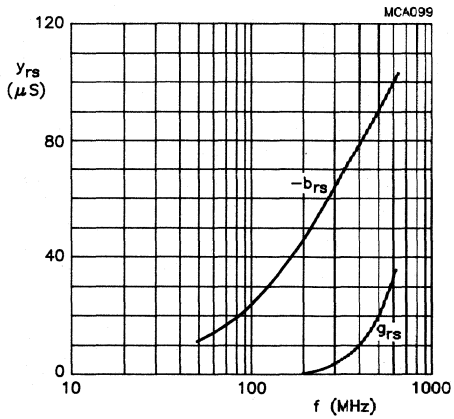


Fig.7 Feedback admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

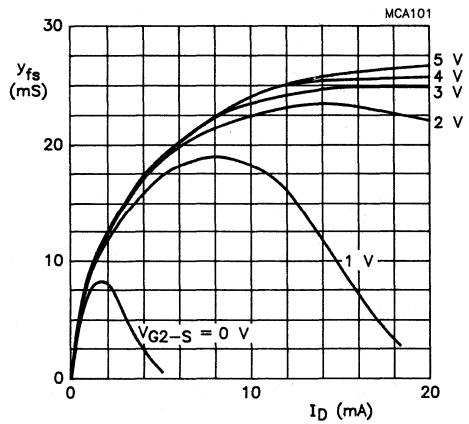


Fig.8 Transfer admittance as a function of drain current.

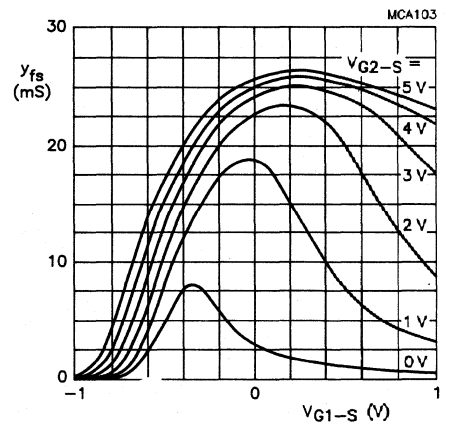


Fig.9 Transfer admittance as a function of gate 2 source voltage.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in VHF applications, such as VHF television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	40	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	200	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25	mS
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30	fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2	dB

MECHANICAL DATA

Dimensions in mm

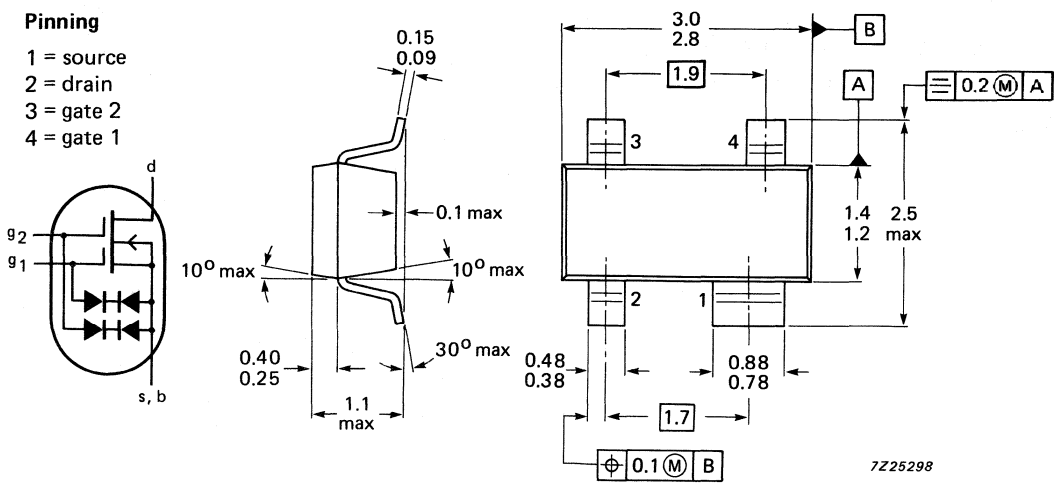
Fig.1 SOT143R.

Marking code

BF992R = M52

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 50 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	500	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25	nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25	nA
Gate-source breakdown voltages				
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20	V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20	V
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		0.2 to 1.3	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$		0.2 to 1.1	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	20	mS
		typ.	25	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
		max.	40	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2	pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2	dB

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for VHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

Dimensions in mm

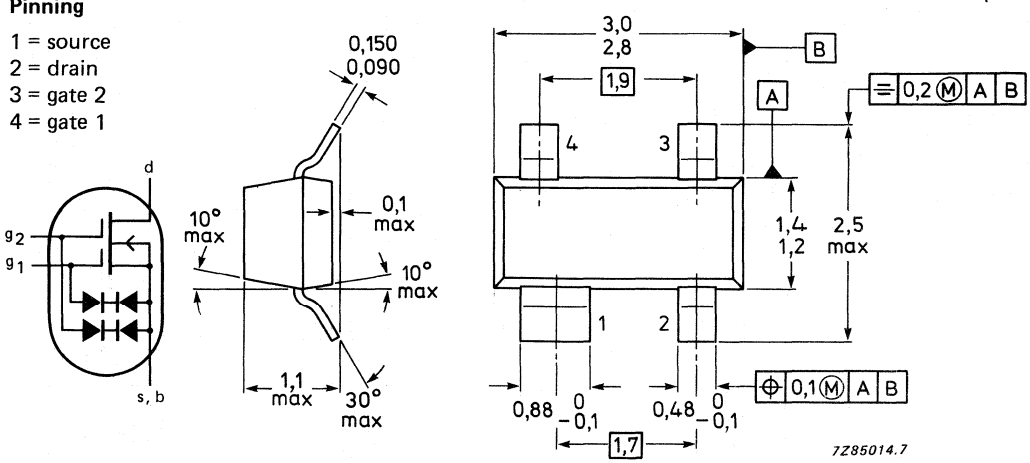
Fig.1 SOT143.

Marking code

BF994S = MGp

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

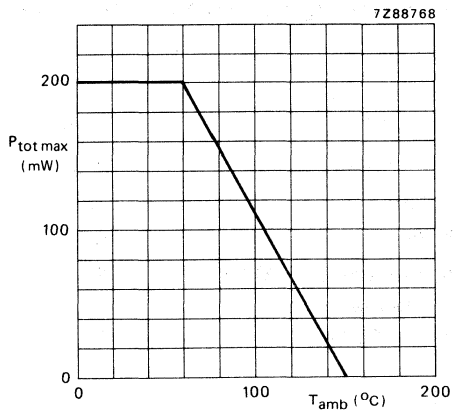


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}S}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}S}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; $V_{G2\text{-}S}$ = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1: f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.5 pF 3.0 pF
Input capacitance at gate 2: f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at G_S = 2 mS; B_S = B_S opt; f = 200 MHz	F	typ.	1.0 dB
Power gain at G_S = 2 mS; B_S = B_S opt G_L = 0.5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for UHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates ans source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1 : f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.8 dB

MECHANICAL DATA

Dimensions in mm

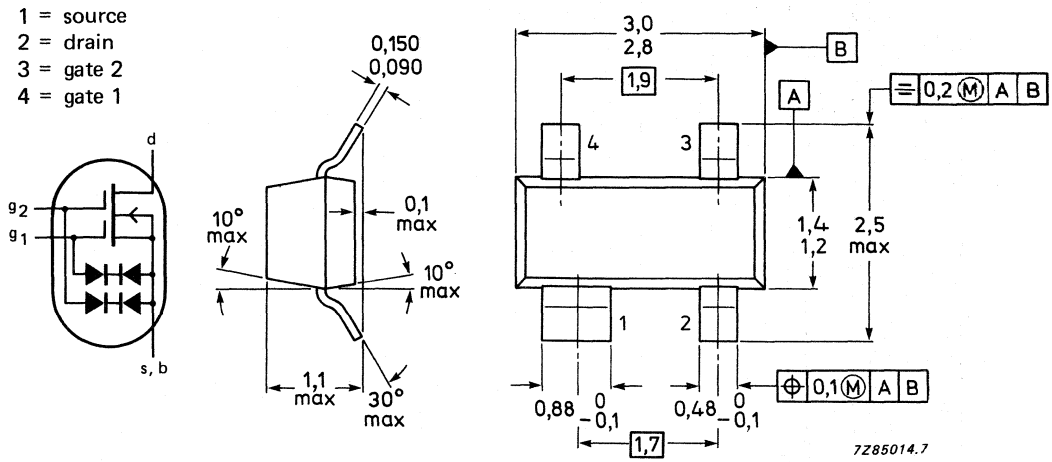
Fig.1 SOT143.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1

Marking code

BF996S = MHp



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

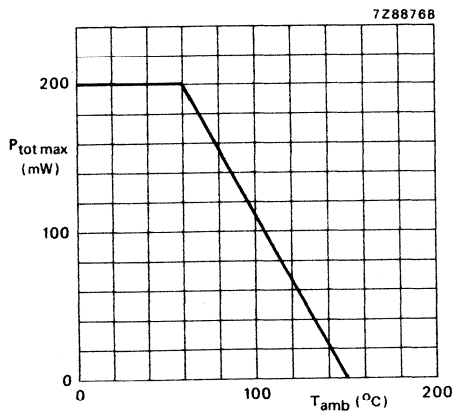


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	50 nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	50 nA
Gate-source breakdown voltages			
± I_{G1-S} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		6 to 20 V
± I_{G2-S} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.3 pF
		max.	2.6 pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8 pF
Noise figure			
f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1.0 dB
f = 800 MHz; G_S = 3.3 mS; B_S = B_S opt		typ.	1.8 dB
Power gain			
f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0.5 mS; B_L = B_L opt	G_p	typ.	25 dB
f = 800 MHz; G_S = 3.3 mS; B_S = B_S opt; G_L = 1.0 mS; B_L = B_L opt		typ.	18 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a large tuning range up to 500 MHz.

QUICK REFERENCE DATA

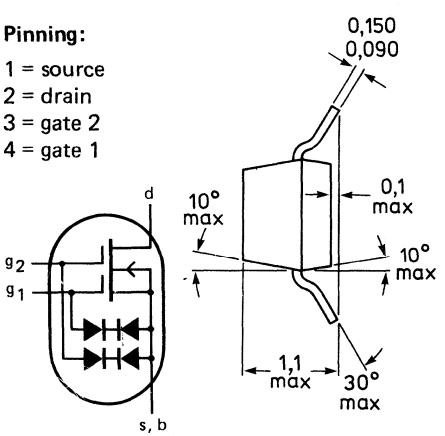
Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2.5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

Fig.1 SOT143.

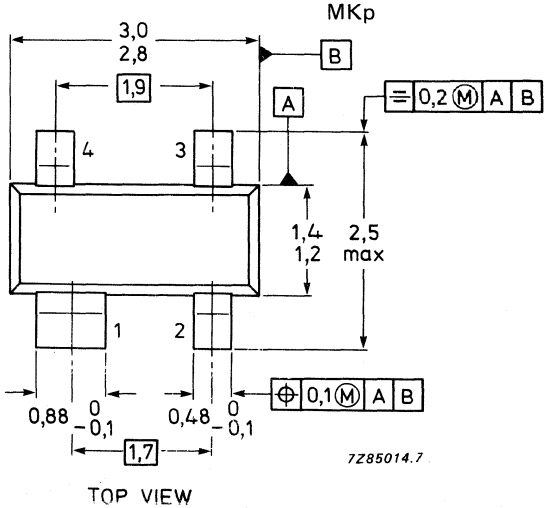
Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



See also *Soldering recommendations.*

Dimensions in mm



TOP VIEW

Marking code:

MKp

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

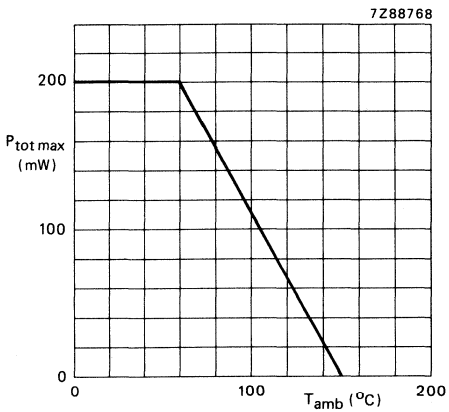


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50 nA
gate 2; $\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
gate 2; $\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
gate 2; I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V
Drain-source cut-off voltage V_{DS} = 15 V; V_{G2-S} = 4 V; V_{G1-S} = 0	I_{DSS}		2 to 20 mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.5 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1991

BF998

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

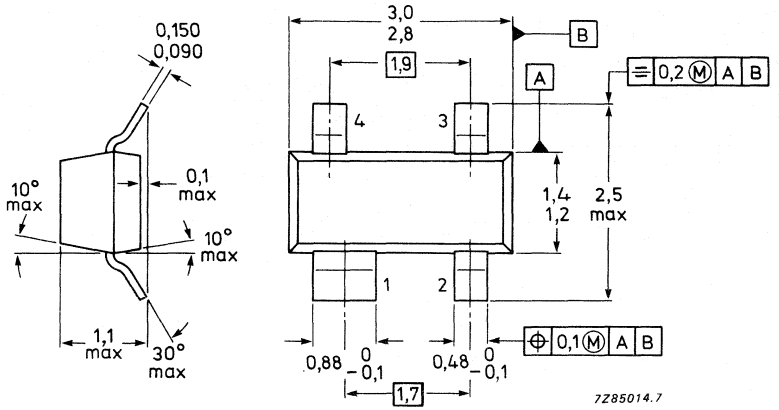
Silicon n-channel dual gate MOS-FET BF998

MECHANICAL DATA

Dimensions in mm

Marking code

BF998 = MOp



TOP VIEW

See also soldering recommendations.

Fig.1 SOT143.

PIN CONFIGURATION

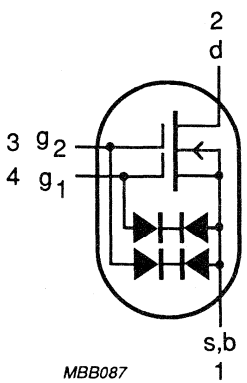


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF998

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C (note 1)	-	200	mW
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 2)	-	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (note 1)	460	K/W
$R_{th\ j-a}$	from junction to ambient in free air (note 2)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Device mounted on printed circuit board.

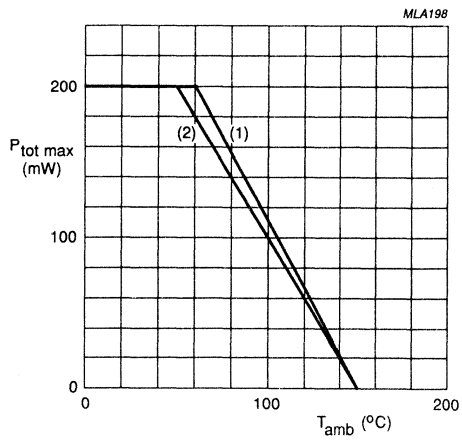


Fig.3 Power derating curve;
(1) ceramic substrate;
(2) printed-circuit board.

Silicon n-channel dual gate MOS-FET | BF998

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V $V_{G2S} = V_{DS}$ = **0**	-	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V $V_{G1S} = V_{DS}$ = 0	-	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA $V_{G2-S} = V_{DS}$ = 0	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA $V_{G1-S} = V_{DS}$ = 0	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2-S}$ = 4 V	-	2.5	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V V_{G1-S} = 0	-	2.0	V
I_{DSS}	drain current (measured under pulse condition)	V_{DS} = 8 V V_{G1-S} = 0 $+V_{G2-S}$ = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET BF998

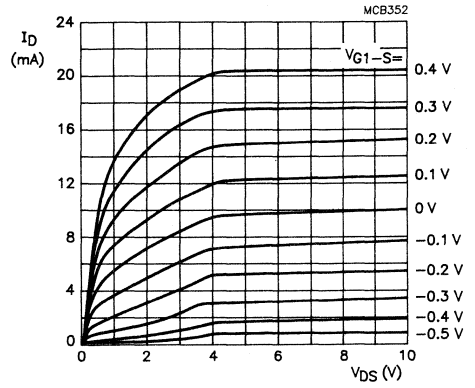


Fig.4 Output characteristics; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

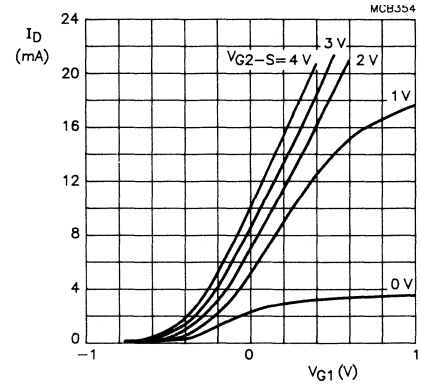


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

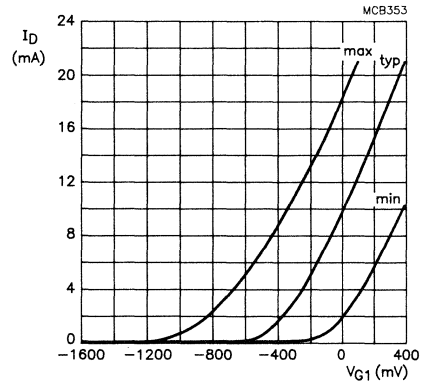


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

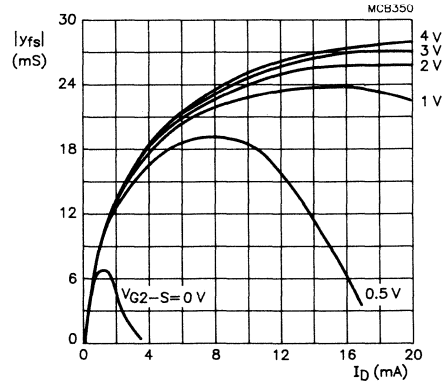


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF998

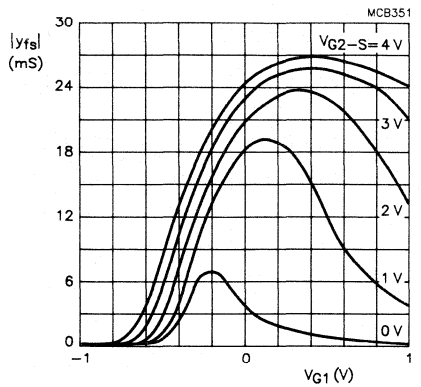


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

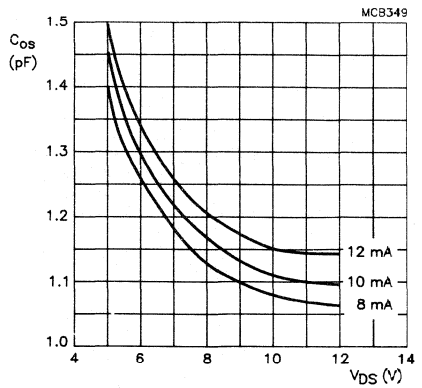


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

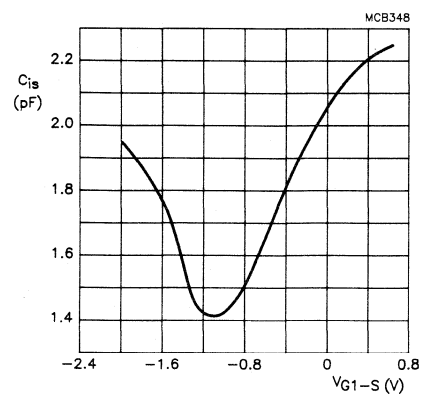


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

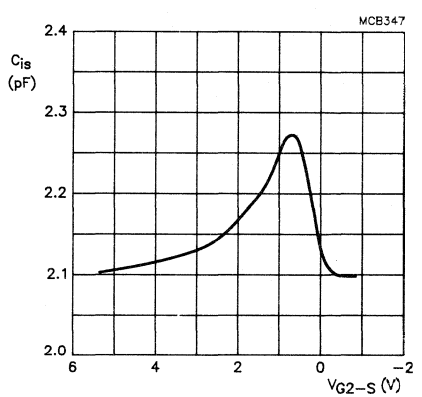


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF998

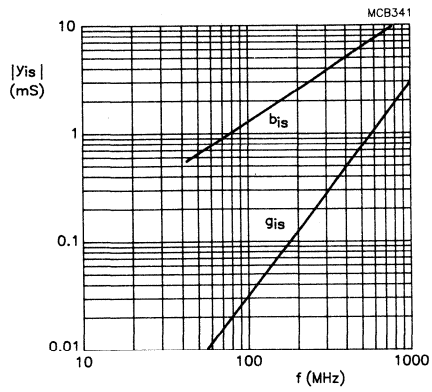


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

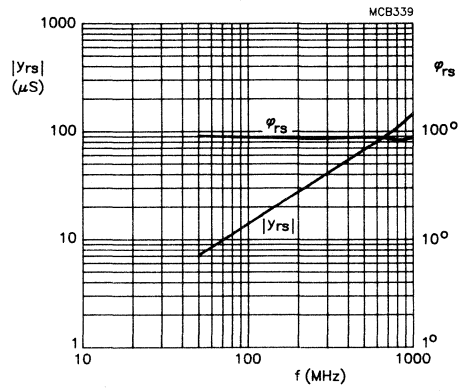


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

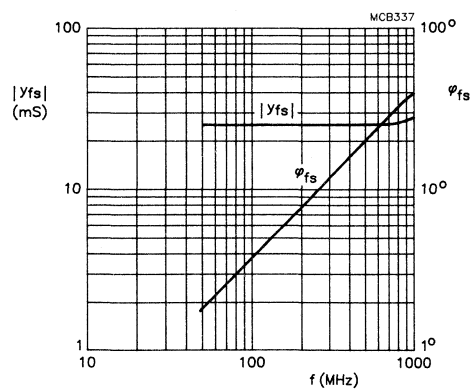


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

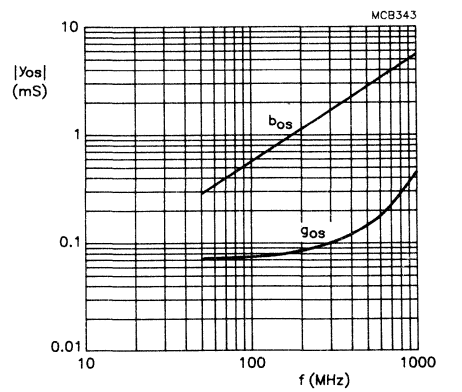
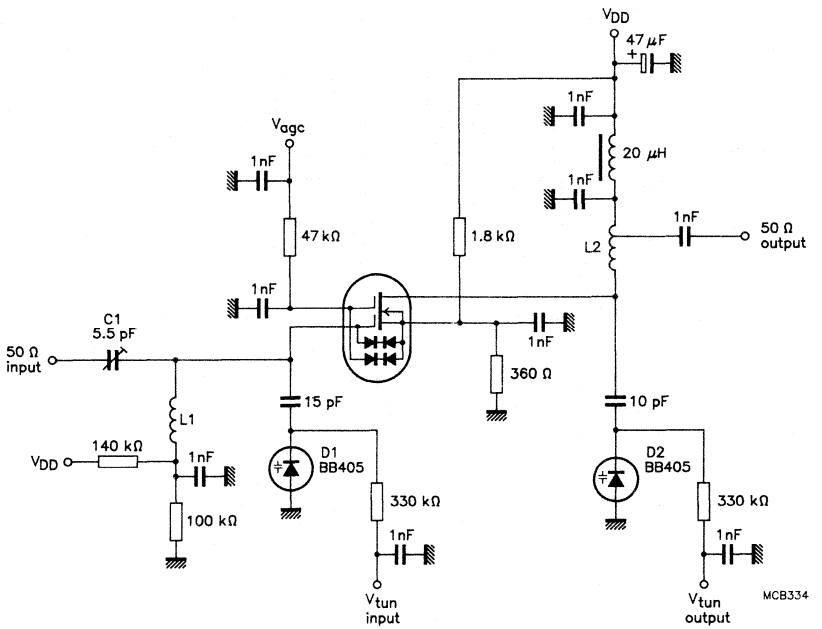
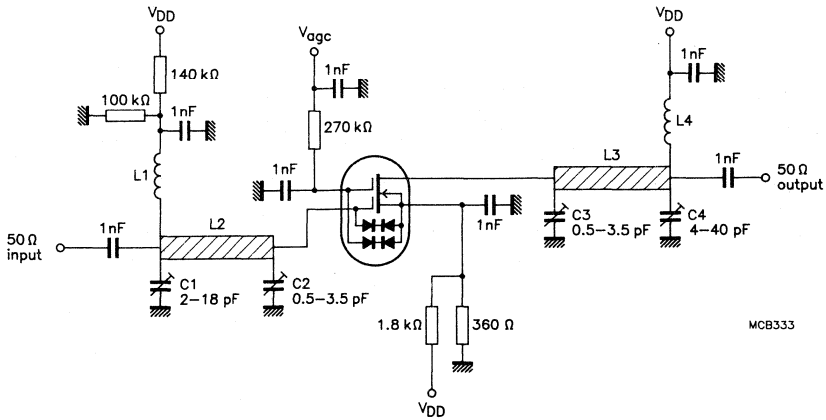


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.



L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

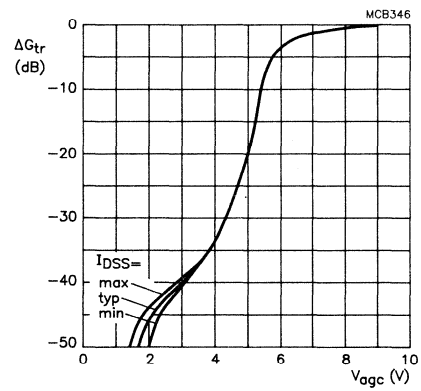


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

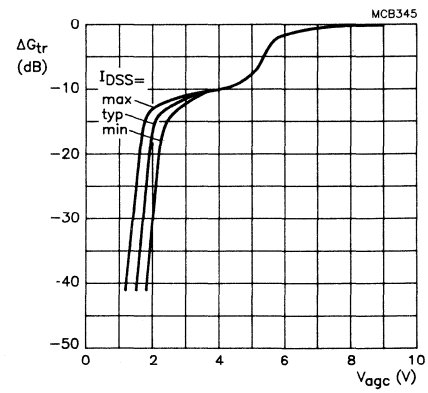


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Data sheet	
status	Product specification
date of issue	April 1995

BF998R

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

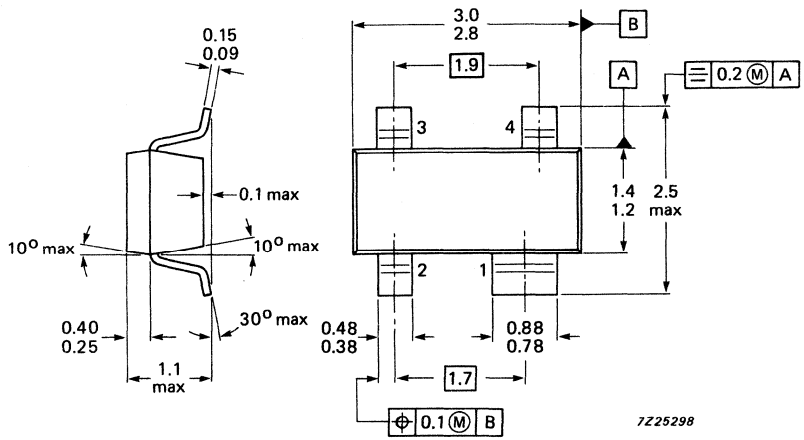
Silicon n-channel dual gate MOS-FET BF998R

MECHANICAL DATA

Dimensions in mm

Marking code

BF998R = MO$\overline{p}$



See also soldering recommendations.

Fig.1 SOT143R.

PIN CONFIGURATION

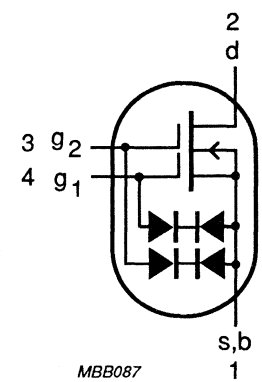


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF998R

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 1)	-	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (note 1)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.

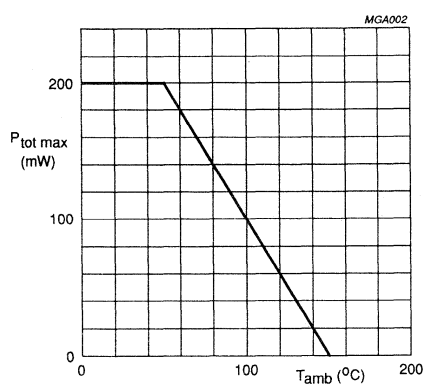


Fig.3 Power derating curve.

Silicon n-channel dual gate MOS-FET BF998R

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V $V_{G2S} = V_{DS} = O$	-	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V $V_{G1S} = V_{DS} = 0$	-	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA $V_{G2-S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA $V_{G1-S} = V_{DS} = 0$	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2-S}$ = 4 V	-	2.5	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V V_{G1-S} = 0	-	2.0	V
I_{DSS}	drain current	V_{DS} = 8 V V_{G1-S} = 0 + V_{G2-S} = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_S = 2 mS $B_S = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_S = 3.3 mS $B_S = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET BF998R

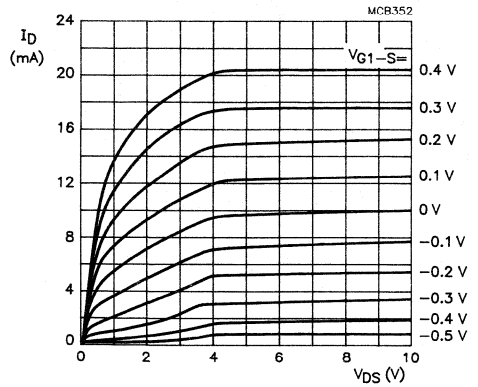


Fig.4 Output characteristics; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

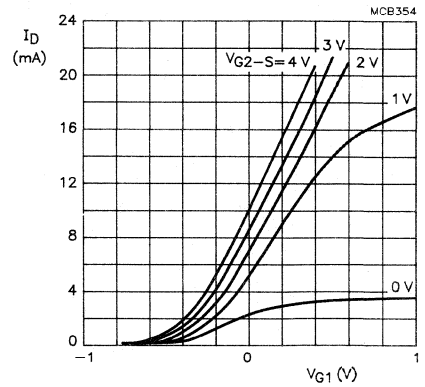


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

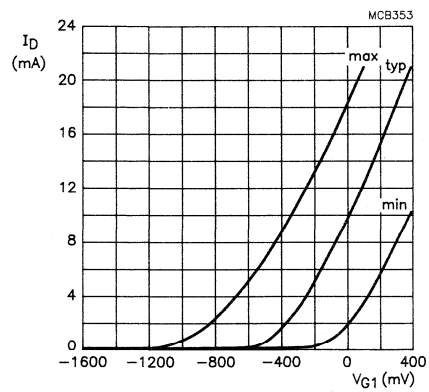


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

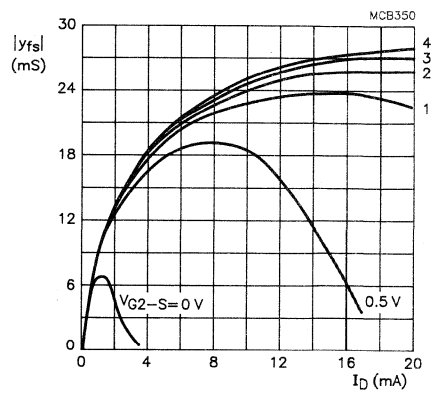


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

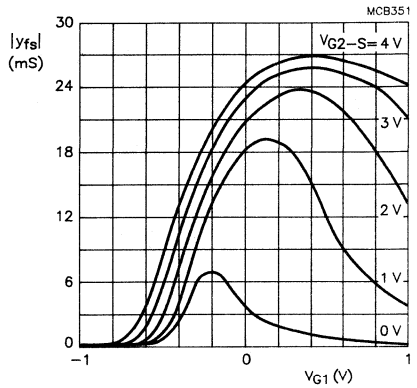


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

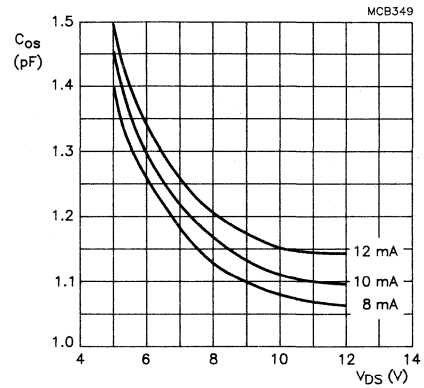


Fig.9 Output capacitance as a function of drain-source voltage; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

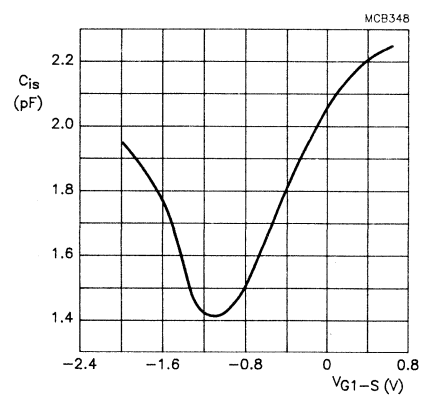


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

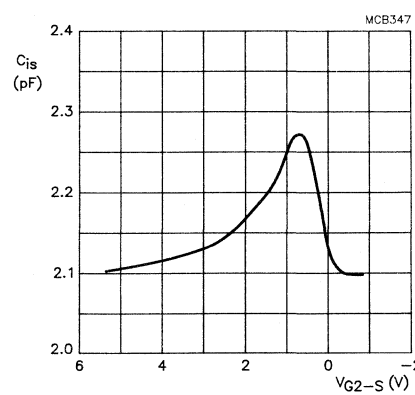


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; V_{G1-S} = 0; f = 1 MHz; T_{amb} = 25 °C.

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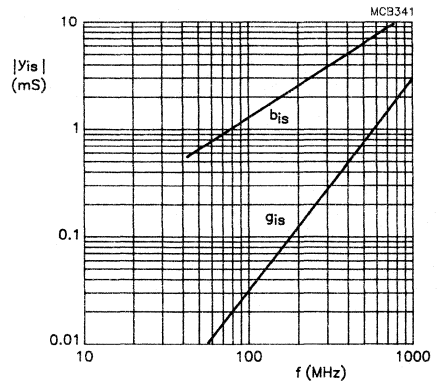


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

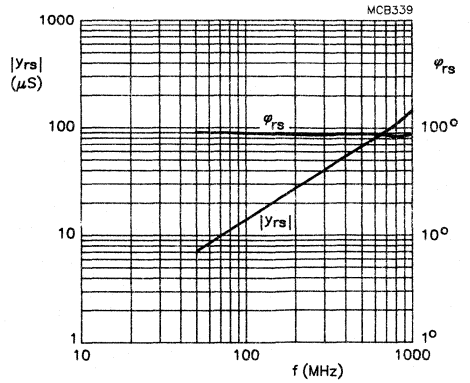


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

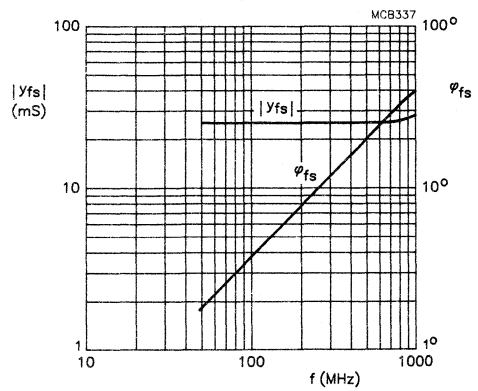


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

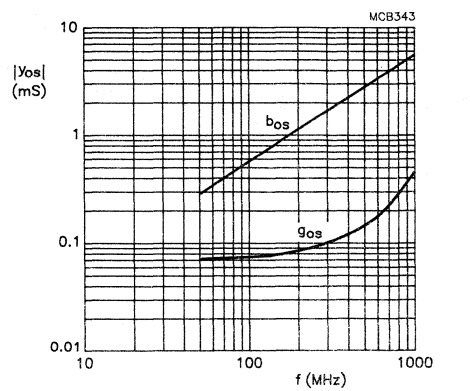
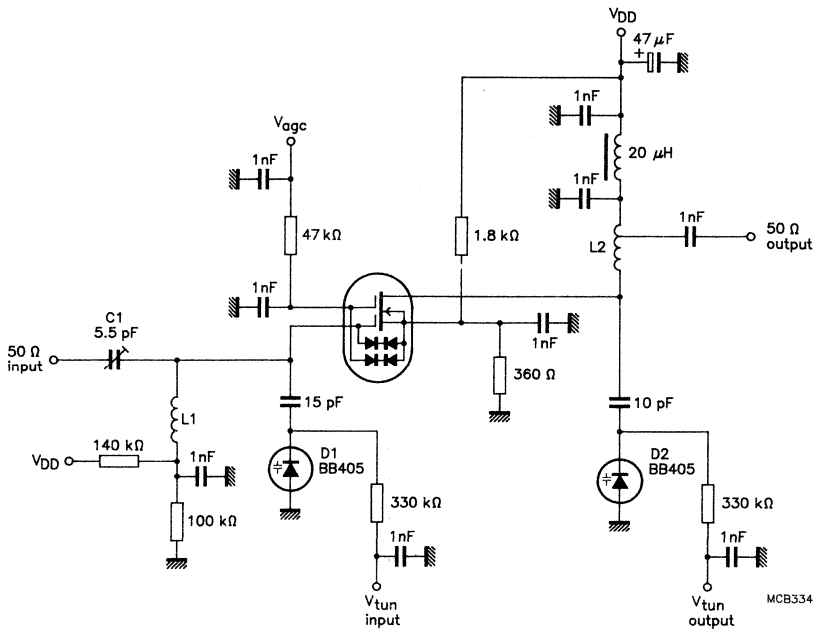


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

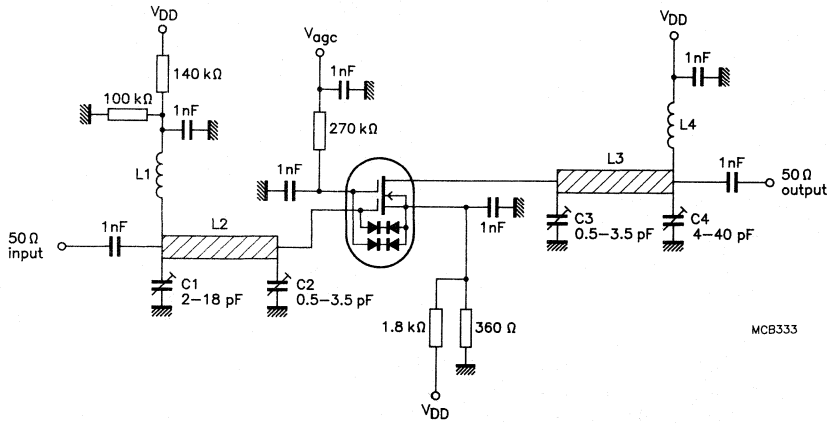


L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.

L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

Silicon n-channel dual gate MOS-FET BF998R



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

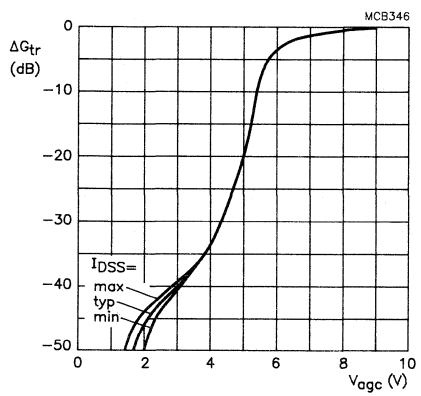


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

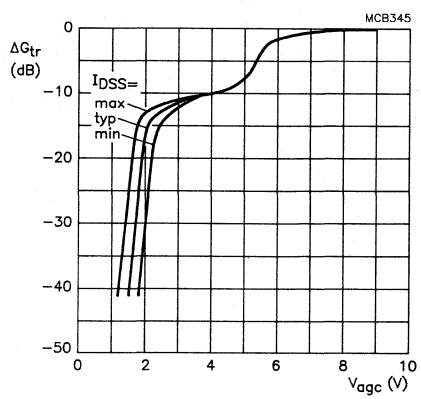


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

N-channel dual-gate MOS-FET BF998WR

FEATURES

- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

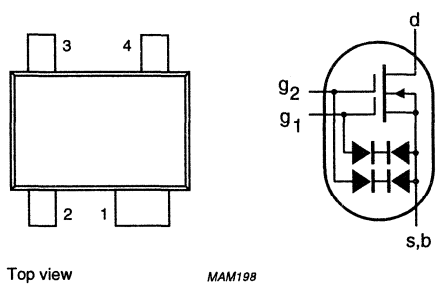
DESCRIPTION

Depletion type field-effect transistor in a plastic microminiature SOT343R package with source and substrate interconnected. The transistor is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MB.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	12	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	300	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		–	24	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.1	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 800 MHz	–	1	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 45 °C; see Fig.2; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

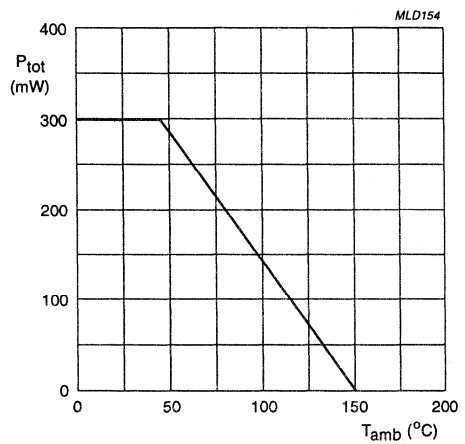


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2; T_s = 90 °C	200	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

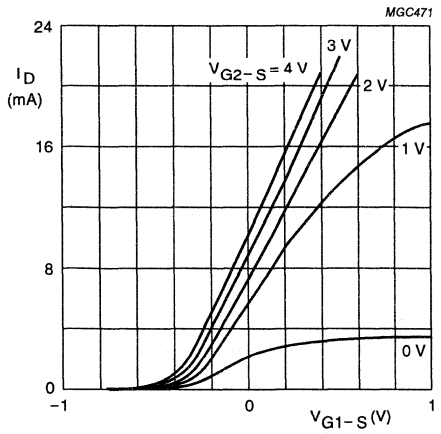
T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = V_{DS} = 0$; $I_{G1\text{-}S}$ = 10 mA	6	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S}$ = 10 mA	6	20	V
$V_{(P)G1\text{-}S}$	gate 1-source cut-off voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; I_D = 20 µA	–	–2.5	V
$V_{(P)G2\text{-}S}$	gate 2-source cut-off voltage	$V_{G1\text{-}S} = 0$; V_{DS} = 8 V; I_D = 20 µA	–	–2	V
I_{DSS}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 8 V; $V_{G1\text{-}S} = 0$	2	18	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS} = 0$; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S}$ = 5 V	–	50	nA

DYNAMIC CHARACTERISTICS

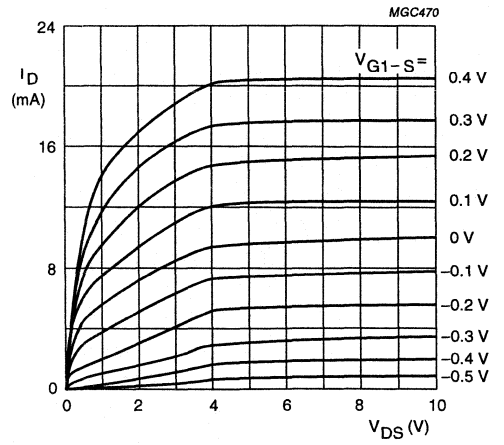
Common source; T_{amb} = 25 °C; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	22	25	–	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.1	2.5	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_S = 2 mS; $B_S = B_{Sopt}$	–	0.6	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{Sopt}$	–	1	–	dB



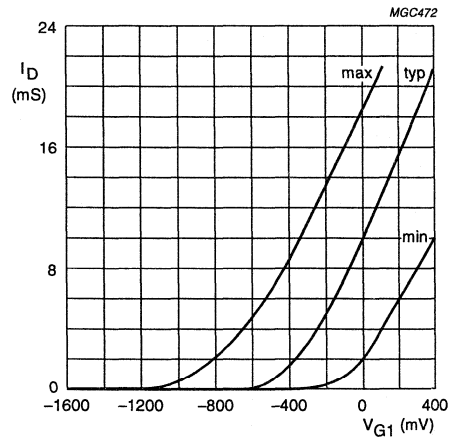
V_{DS} = 8 V.
T_{amb} = 25 °C.

Fig.3 Transfer characteristics; typical values.



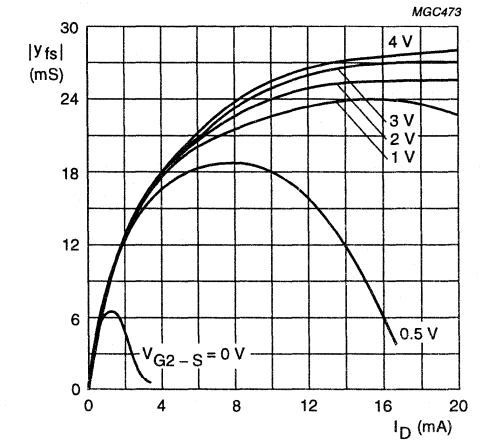
V_{G2-S} = 4 V.
T_{amb} = 25 °C.

Fig.4 Output characteristics; typical values.



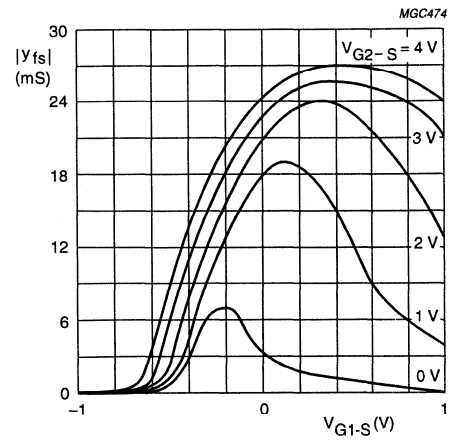
V_{DS} = 8 V; V_{G2} = 4 V; T_{amb} = 25 °C.

Fig.5 Drain current as a function of gate 1 voltage; typical values.



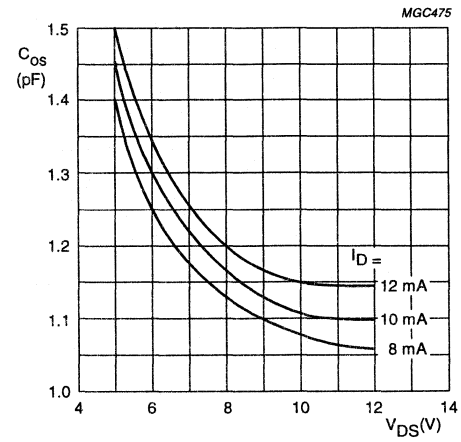
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.6 Forward transfer admittance as a function of drain current; typical values.



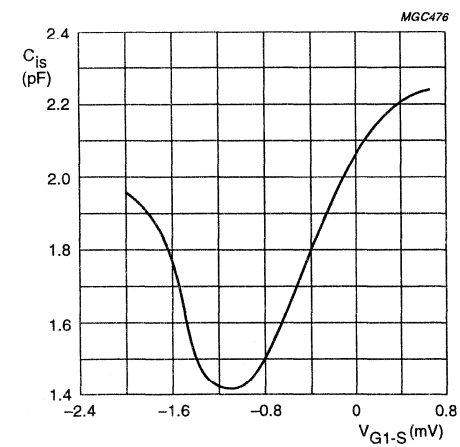
V_{DS} = 8 V; T_{amb} = 25 °C.

Fig.7 Forward transfer admittance as a function of gate 1 voltage; typical values.



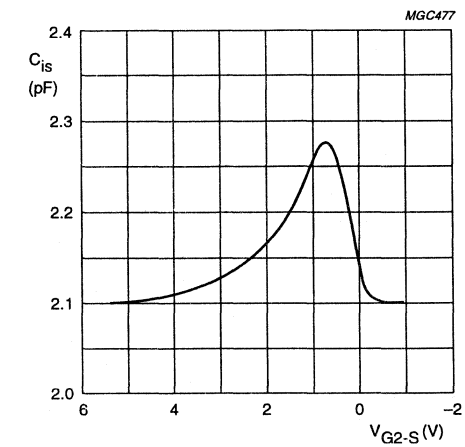
V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.8 Output capacitance as a function of drain-source voltage; typical values.



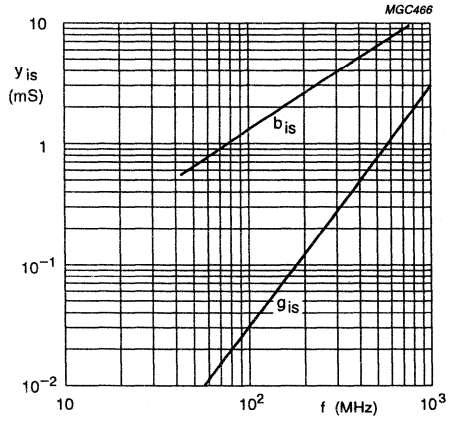
V_{DS} = 8 V; V_{G2-S} = 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.9 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.



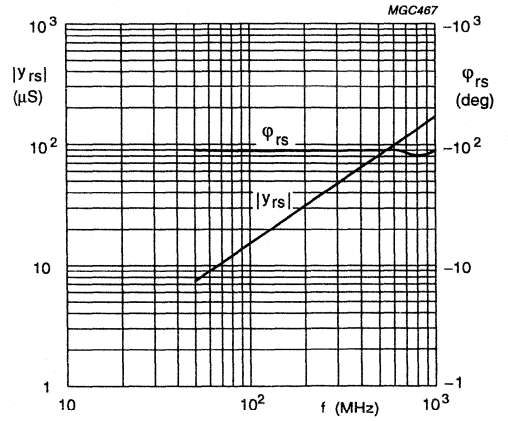
V_{DS} = 8 V; V_{G1-S} = 0 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.10 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.



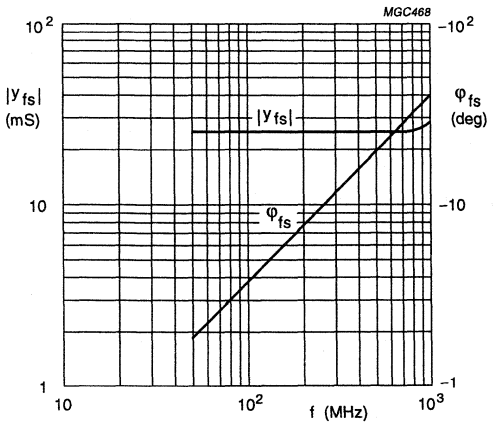
V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.11 Input admittance as a function of the frequency; typical values.



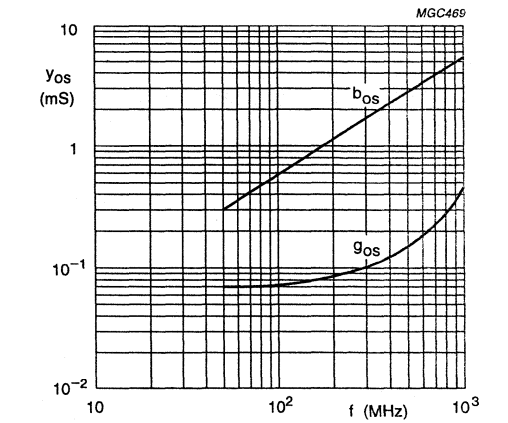
V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.12 Reverse transfer admittance and phase as a function of frequency; typical values.



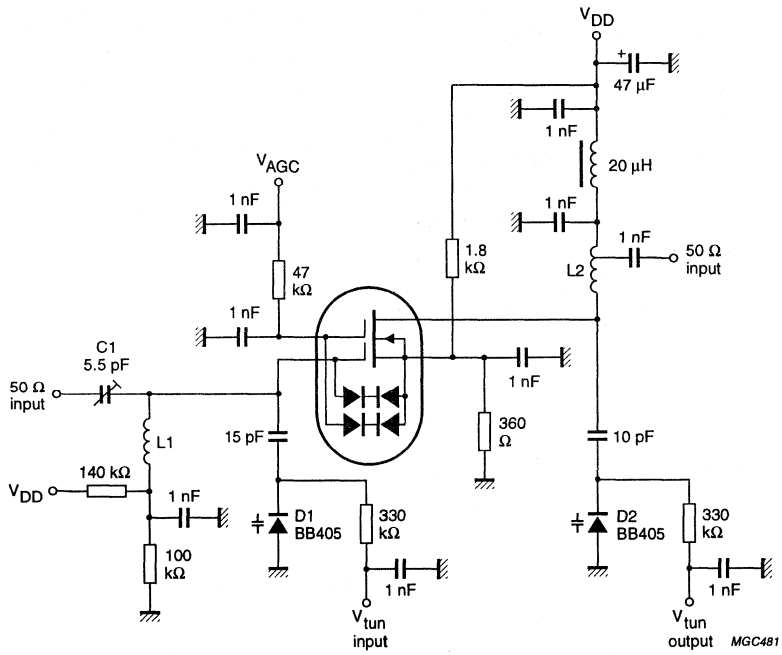
V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.13 Forward transfer admittance and phase as a function of frequency; typical values.



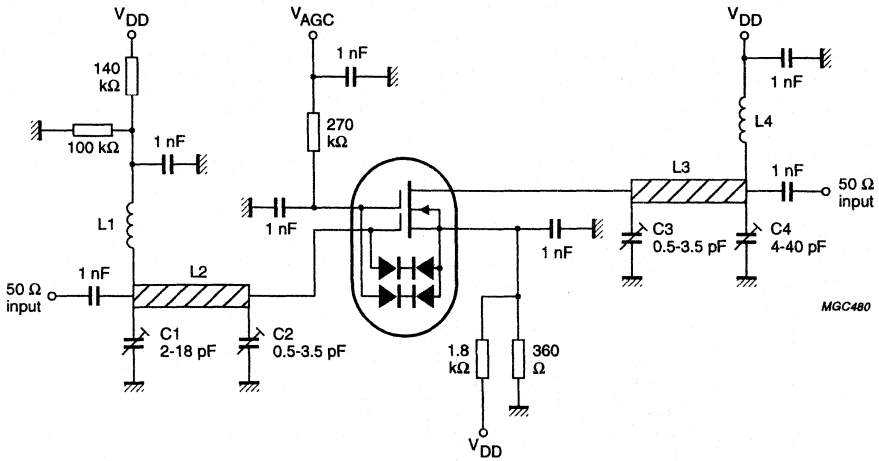
V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.14 Output admittance as a function of the frequency; typical values.



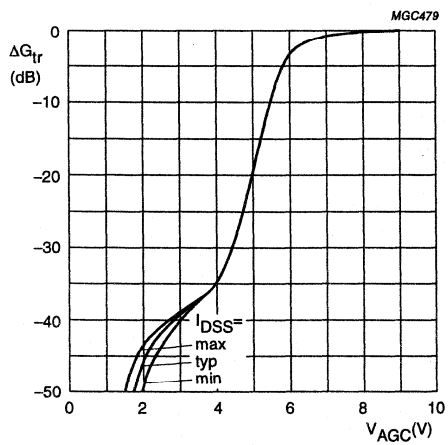
V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.
L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.
L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS. C1 adjusted for G_S = 2 mS.

Fig.15 Gain control testcircuit at f = 200 MHz.



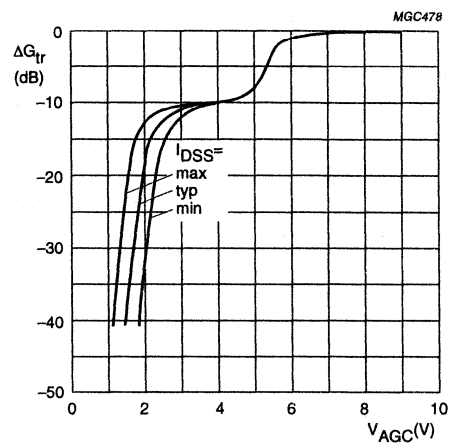
V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.
L1 = L4 = 200 nH; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.16 Gain control test circuit at f = 800 MHz.



V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

Fig.17 Automatic gain control characteristics measured in circuit of Fig.15.



V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Fig.18 Automatic gain control characteristics measured in circuit of Fig.16.

Dual-gate MOS-FETs | BF1100; BF1100R

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

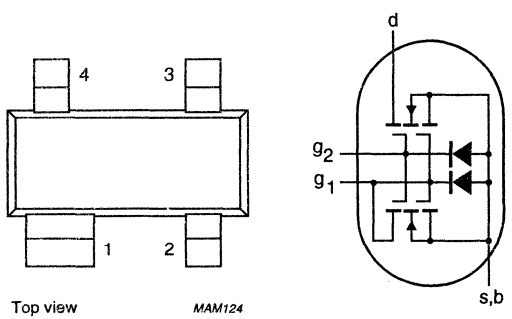
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

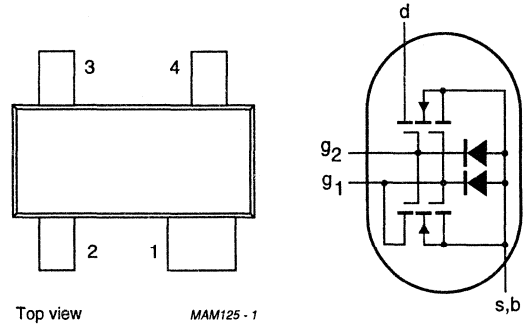
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF1100 marking code: M56.

Fig.1 Simplified outline (SOT143) and symbol.



BF1100R marking code: M57.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	14	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		24	28	33	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF1100	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF1100R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

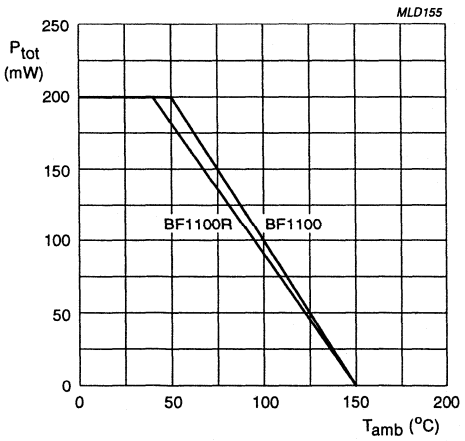


Fig.3 Power derating curves.

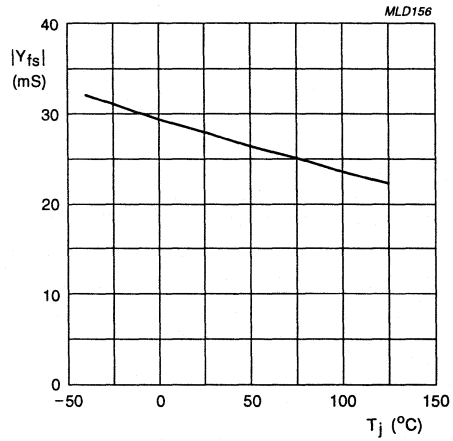


Fig.4 Forward transfer admittance as a function of junction temperature; typical values.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF1100		500	K/W
	BF1100R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF1100	T_s = 92 °C	290	K/W
	BF1100R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 1 mA	13.2	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 1 mA	13.2	20	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 µA	0.3	1	V
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 µA	0.3	1.2	V
		$V_{G1\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; R_{G1} = 180 kΩ; note 1	8	13	mA
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; R_{G1} = 250 kΩ; note 2	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 12 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 12 V	–	50	nA

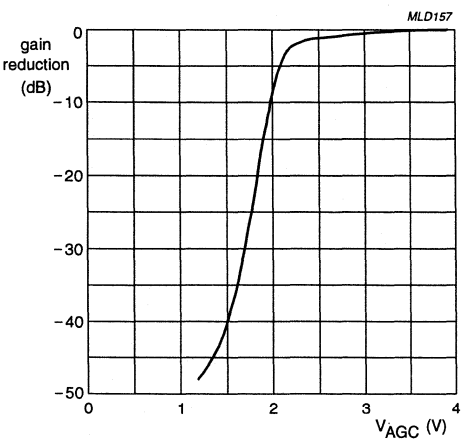
Notes

1. R_{G1} connects gate 1 to V_{GG} = 9 V; see Fig.27.
2. R_{G1} connects gate 1 to V_{GG} = 12 V; see Fig.27.

DYNAMIC CHARACTERISTICS

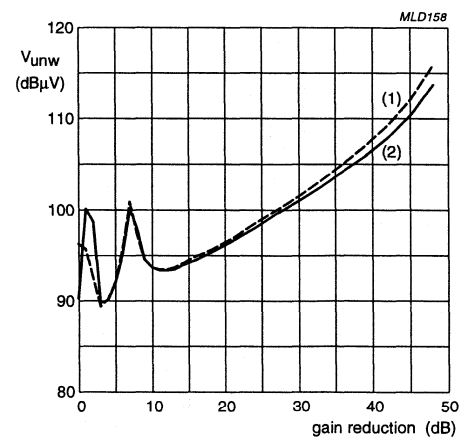
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C				
		V_{DS} = 9 V	24	28	33	mS
		V_{DS} = 12 V	24	28	33	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz				
		V_{DS} = 9 V	–	2.2	2.6	pF
		V_{DS} = 12 V	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz				
		V_{DS} = 9 V	–	1.6	–	pF
		V_{DS} = 12 V	–	1.4	–	pF
C_{os}	drain-source capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	1.4	1.8	pF
		V_{DS} = 12 V	–	1.1	1.5	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	25	35	fF
		V_{DS} = 12 V	–	25	35	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$				
		V_{DS} = 9 V	–	2	2.8	dB
		V_{DS} = 12 V	–	2	2.8	dB



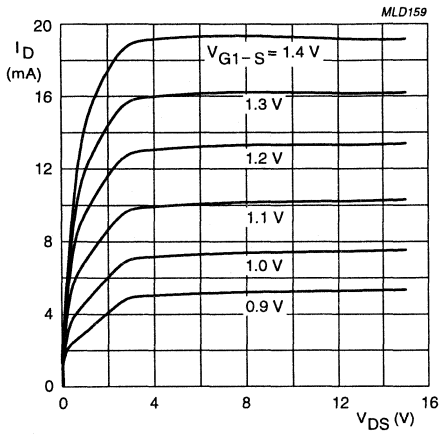
f = 50 MHz.
T_j = 25 °C.

Fig.5 Gain reduction as a function of the AGC voltage; typical values.



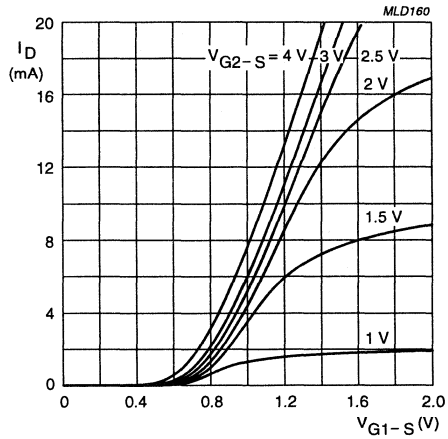
(1) R_G = 250 kΩ to V_{GG} = 12 V
(2) R_G = 180 kΩ to V_{GG} = 9 V
f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.27.



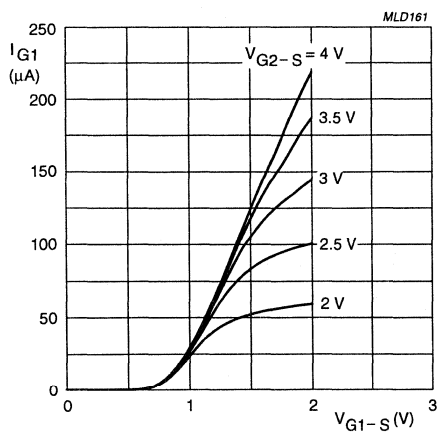
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.7 Output characteristics; typical values.



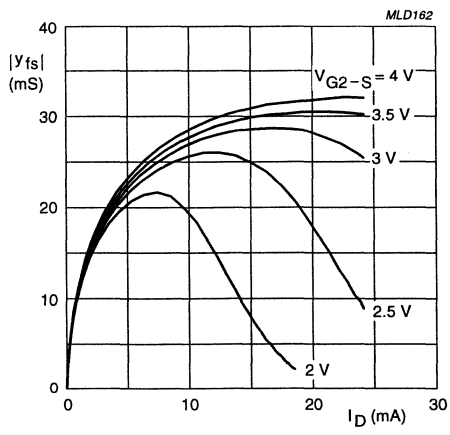
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.8 Transfer characteristics; typical values.



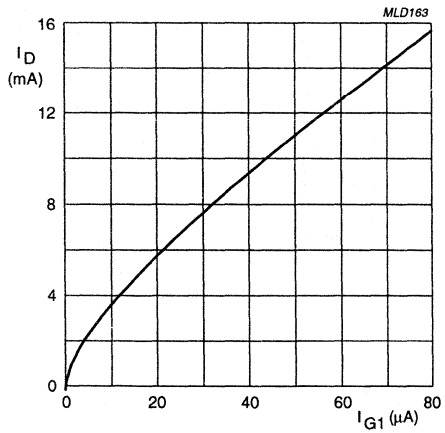
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



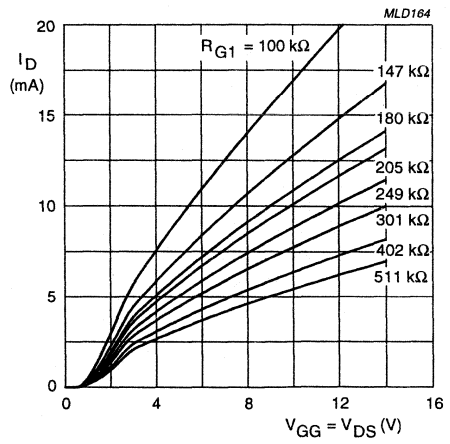
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.



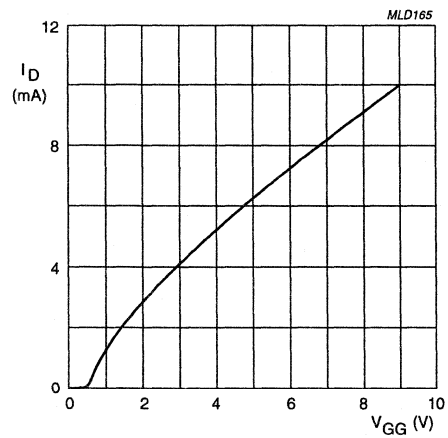
V_{DS} = 9 to 12 V.
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 current; typical values.



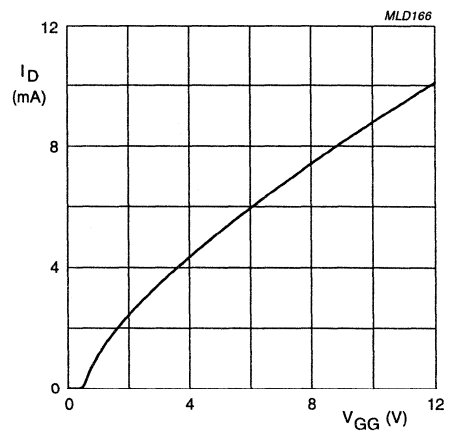
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}.
T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 supply voltage (= V_{GG}) and drain supply voltage; typical values; see Fig.27.



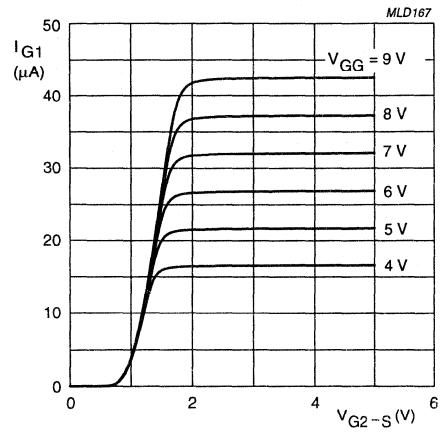
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.27.



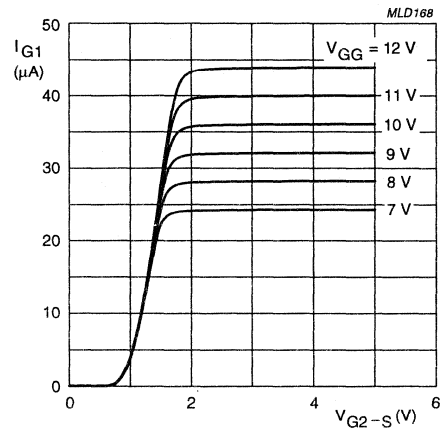
V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.14 Drain current as a function of gate 1 voltage; (= V_{GG}); typical values; see Fig.27.



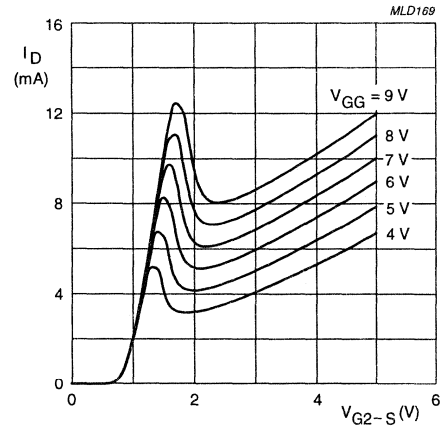
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



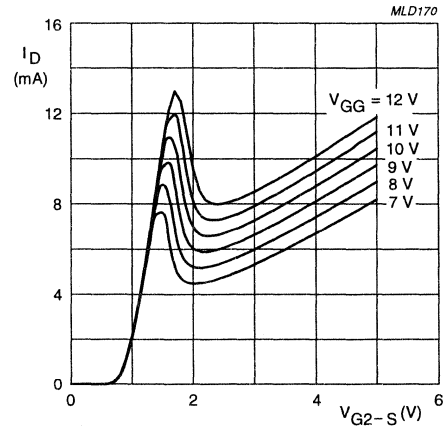
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.16 Gate 1 current as a function of gate 2 voltage; typical values.



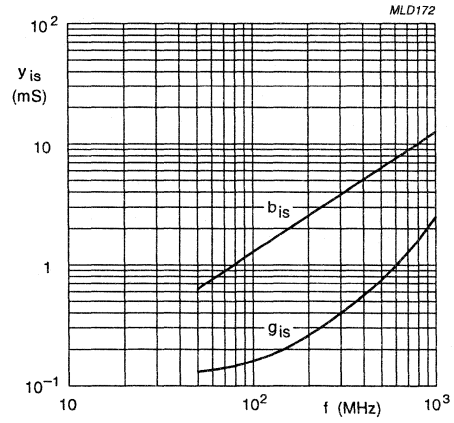
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.



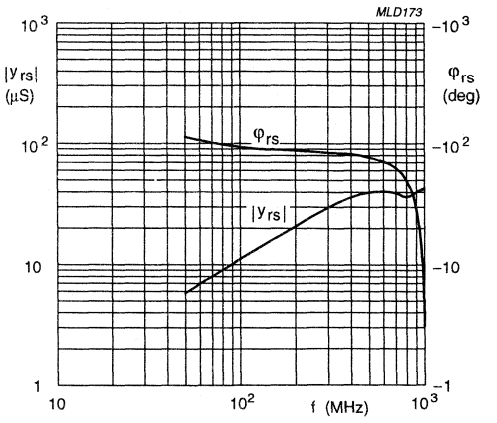
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}).
T_j = 25 °C.

Fig.18 Drain current as a function of the gate 2 voltage; typical values; see Fig.27.



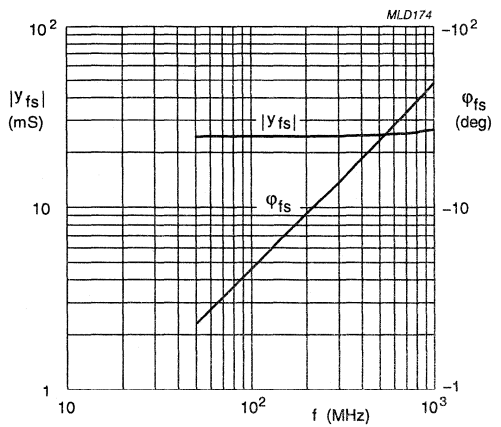
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Input admittance as a function of frequency; typical values.



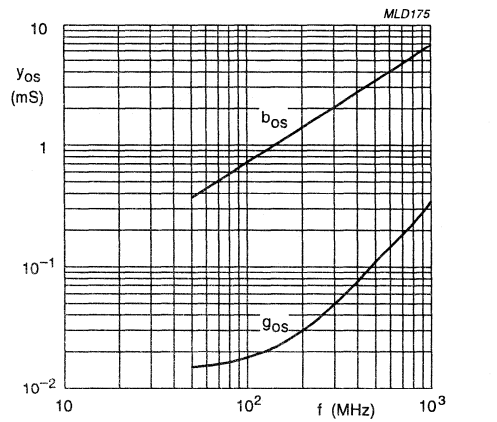
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse transfer admittance and phase as a function of frequency; typical values.



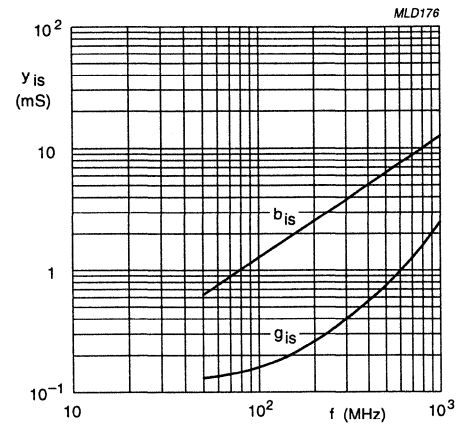
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Forward transfer admittance and phase as a function of frequency; typical values.



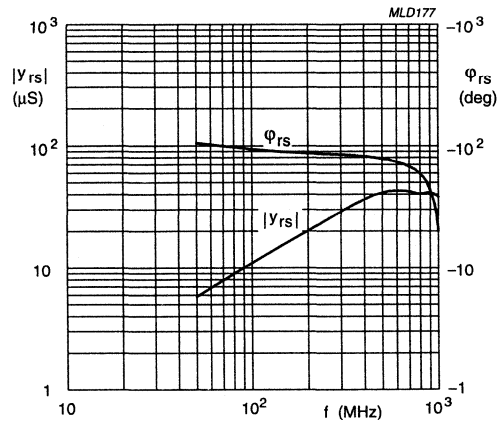
V_{DS} = 9 V; V_{G2} = 4 V.
I_D =10 mA; T_{amb} = 25 °C.

Fig.22 Output admittance as a function of frequency; typical values.



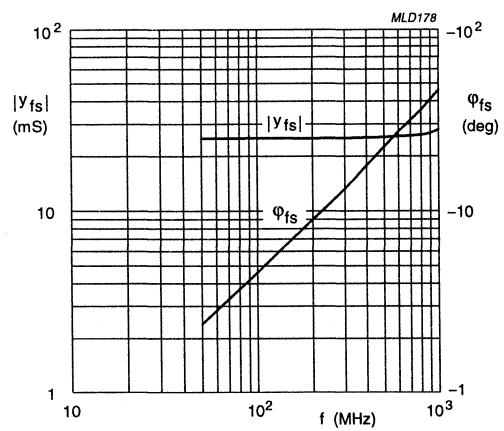
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.23 Input admittance as a function of frequency; typical values.



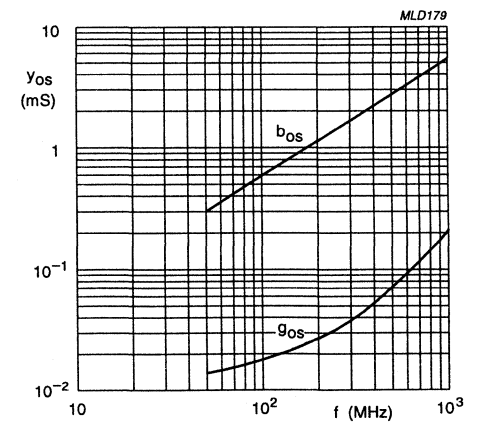
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.24 Reverse transfer admittance and phase as a function of frequency; typical values.



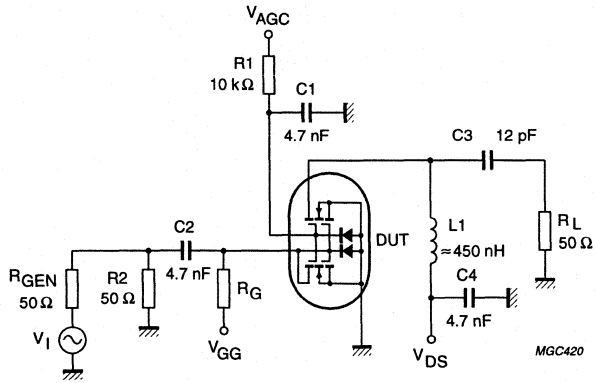
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.25 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.26 Output admittance as a function of frequency; typical values.



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ kΩ.
For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ kΩ.

Fig.27 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	−3.6	2.528	174.4	0.001	63.7	1.000	−2.0
100	0.983	−7.4	2.531	169.8	0.001	80.7	1.000	−4.2
200	0.974	−14.7	2.490	159.5	0.002	81.0	0.996	−8.1
300	0.960	−21.8	2.446	149.8	0.002	80.3	0.994	−11.9
400	0.953	−28.7	2.412	139.8	0.003	76.3	0.992	−15.7
500	0.933	−35.4	2.341	130.1	0.003	76.5	0.987	−19.4
600	0.915	−42.0	2.283	120.4	0.004	79.0	0.984	−23.0
700	0.895	−47.9	2.205	111.6	0.003	81.5	0.981	−26.7
800	0.880	−53.5	2.146	102.9	0.003	90.8	0.978	−30.3
900	0.864	−59.6	2.087	93.4	0.003	106.6	0.974	−33.9
1000	0.839	−65.0	1.998	84.4	0.003	135.4	0.971	−37.6

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	−3.7	2.478	174.7	0.001	72.2	1.000	−1.6
100	0.984	−7.4	2.480	170.3	0.001	80.9	1.000	−3.5
200	0.974	−14.6	2.440	160.6	0.002	82.7	0.997	−6.6
300	0.960	−21.8	2.400	151.4	0.002	79.9	0.996	−9.7
400	0.953	−28.7	2.371	141.9	0.003	77.7	0.994	−12.8
500	0.933	−35.3	2.306	132.7	0.003	77.1	0.991	−15.8
600	0.915	−41.9	2.255	123.6	0.004	77.1	0.989	−18.7
700	0.894	−47.8	2.183	115.3	0.004	79.3	0.986	−21.7
800	0.879	−53.5	2.131	107.2	0.003	83.9	0.984	−24.6
900	0.863	−59.5	2.080	98.2	0.003	95.1	0.982	−27.5
1000	0.838	−65.0	1.999	89.7	0.003	115.8	0.980	−30.4

Table 4 Noise data: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

Dual-gate MOS-FET BF1100WR

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

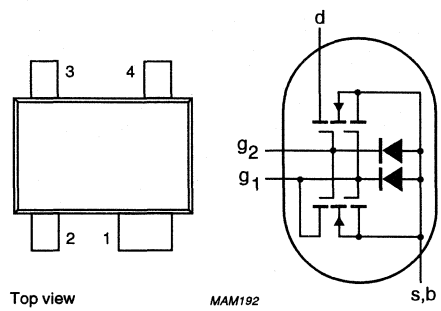
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MF.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	14	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		24	28	33	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	2.2	2.6	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.2; up to T_{amb} = 50 °C; note 1	–	280	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

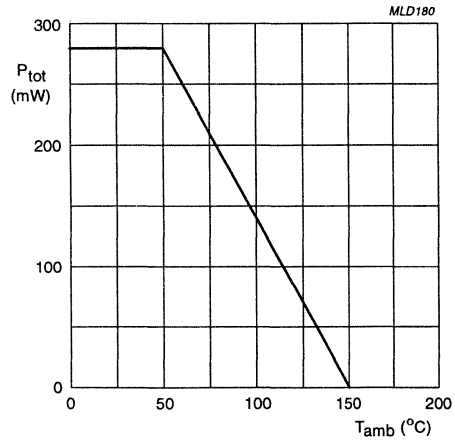


Fig.2 Power derating curve.

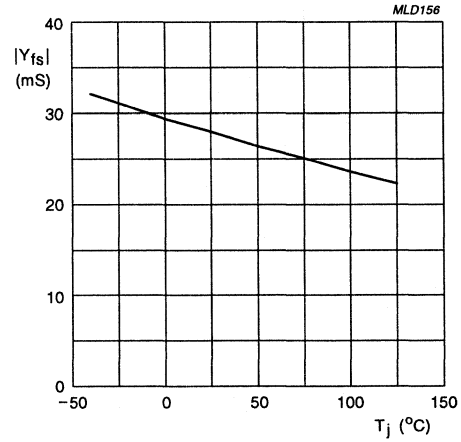


Fig.3 Forward transfer admittance as a function of junction temperature; typical values.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	T_s = 91 °C; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 1 mA	13.2	20	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 1 mA	13.2	20	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 µA	0.3	1	V
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 µA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = 4 V; V_{DS} = 9 V; I_D = 20 µA	0.3	1.2	V
		$V_{G1\text{-}S}$ = 4 V; V_{DS} = 12 V; I_D = 20 µA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; R_{G1} = 180 kΩ; note 1	8	13	mA
		$V_{G2\text{-}S}$ = 4 V; V_{DS} = 12 V; R_{G1} = 250 kΩ; note 2	8	13	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 12 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 12 V	–	50	nA

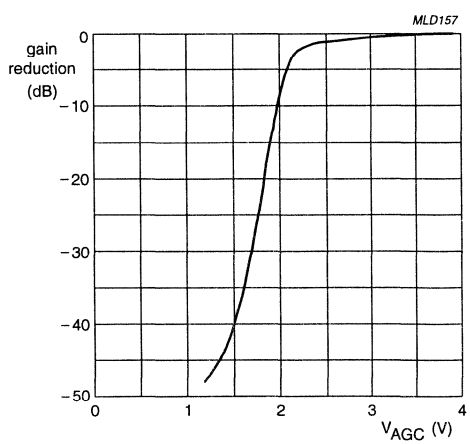
Notes

1. R_{G1} connects gate 1 to V_{GG} = 9 V; see Fig.26.
2. R_{G1} connects gate 1 to V_{GG} = 12 V; see Fig.26.

DYNAMIC CHARACTERISTICS

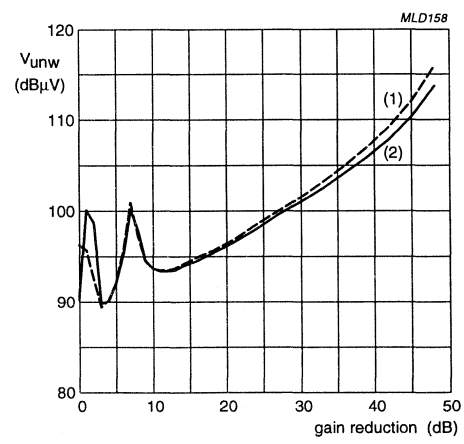
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; I_D = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C				
		V_{DS} = 9 V	24	28	33	mS
		V_{DS} = 12 V	24	28	33	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz				
		V_{DS} = 9 V	–	2.2	2.6	pF
		V_{DS} = 12 V	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz				
		V_{DS} = 9 V	–	1.6	–	pF
		V_{DS} = 12 V	–	1.4	–	pF
C_{os}	drain-source capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	1.4	1.8	pF
		V_{DS} = 12 V	–	1.1	1.5	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz				
		V_{DS} = 9 V	–	25	35	fF
		V_{DS} = 12 V	–	25	35	fF
F	noise figure	f = 800 MHz; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$				
		V_{DS} = 9 V	–	2	2.8	dB
		V_{DS} = 12 V	–	2	2.8	dB



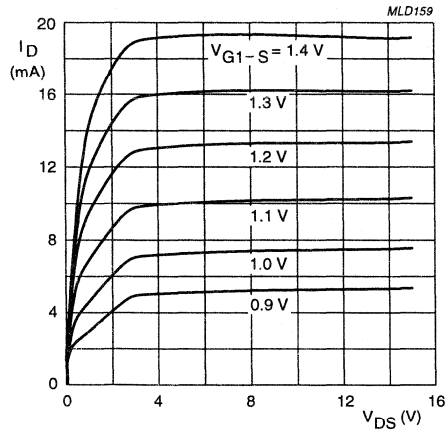
f = 50 MHz.
T_j = 25 °C.

Fig.4 Gain reduction as a function of the AGC voltage; typical values.



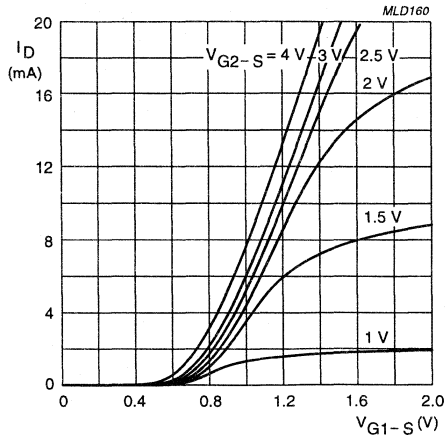
(1) R_G = 250 kΩ to V_{GG} = 12 V.
(2) R_G = 180 kΩ to V_{GG} = 9 V.
f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.5 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.26.



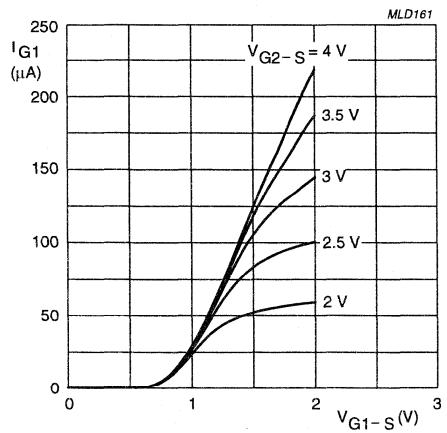
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



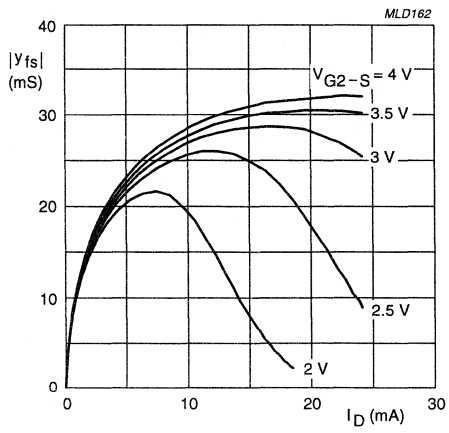
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



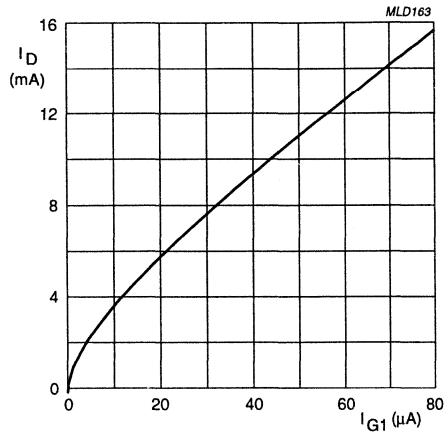
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.8 Gate 1 current as a function of gate 1 voltage; typical values.



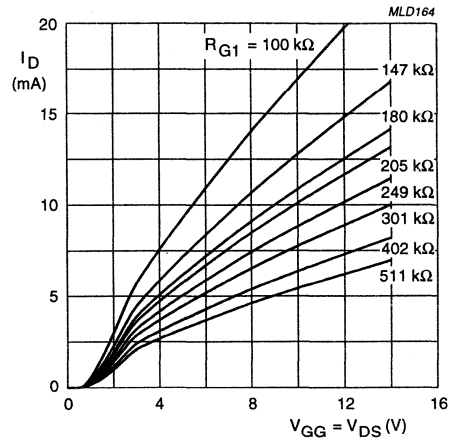
V_{DS} = 9 to 12 V.
T_j = 25 °C.

Fig.9 Forward transfer admittance as a function of drain current; typical values.



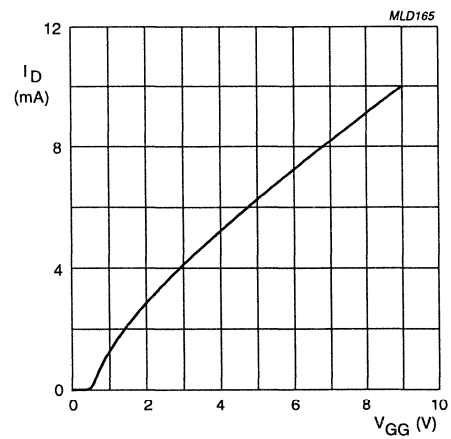
V_{DS} = 9 to 12 V.
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



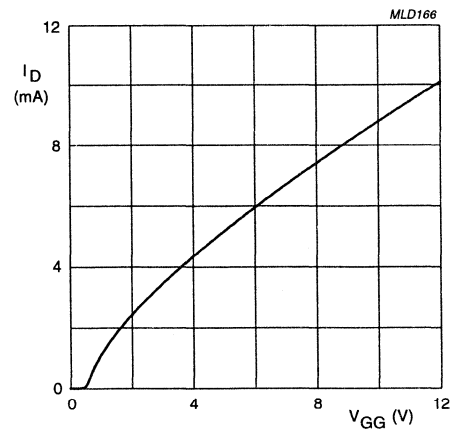
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}.
T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 supply voltage (= V_{GG}) and drain supply voltage; typical values; see Fig.26.



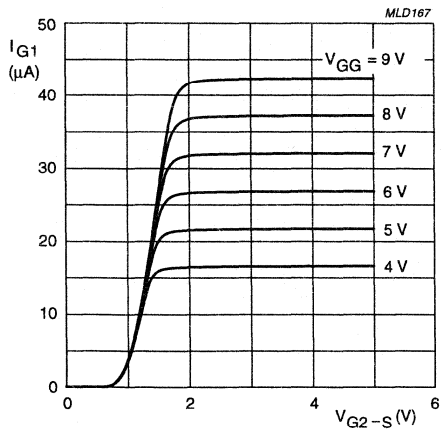
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.12 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.26.



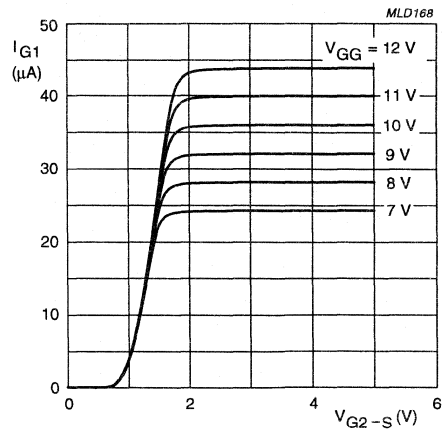
V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.13 Drain current as a function of gate 1 voltage (= V_{GG}); typical values; see Fig.26.



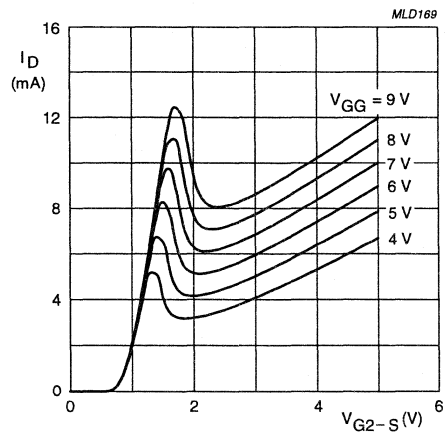
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.14 Gate 1 current as a function of gate 2 voltage; typical values.



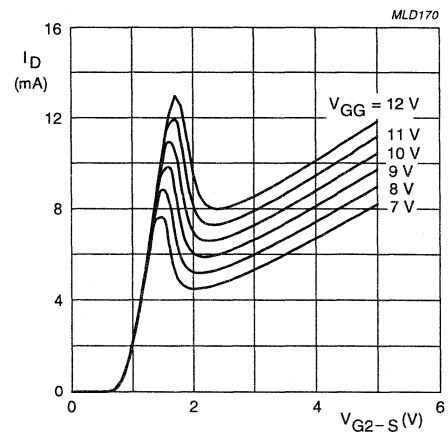
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.



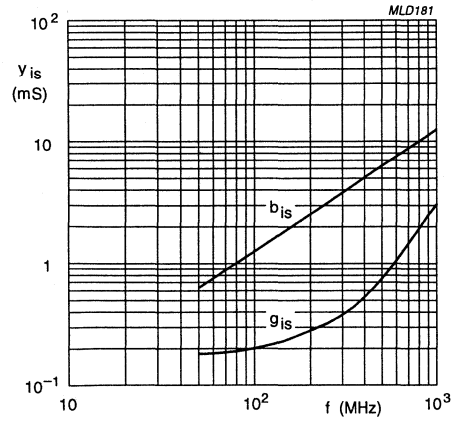
V_{DS} = 9 V.
R_{G1} = 180 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.16 Drain current as a function of the gate 2 voltage; typical values; see Fig.26.



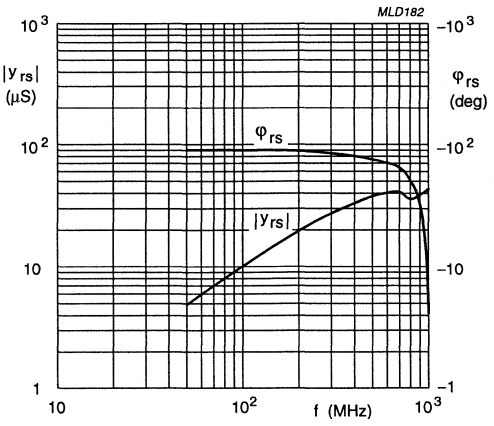
V_{DS} = 12 V.
R_{G1} = 250 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.17 Drain current as a function of the gate 2 voltage; typical values; see Fig.26.



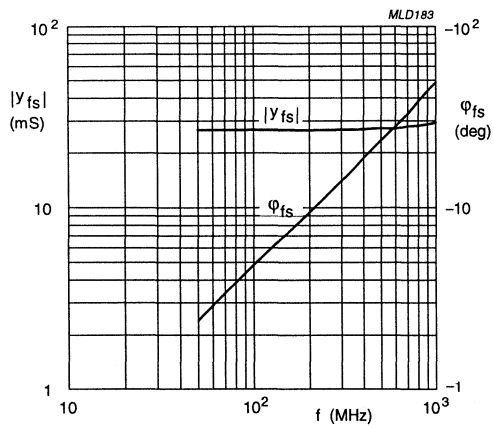
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.18 Input admittance as a function of frequency; typical values.



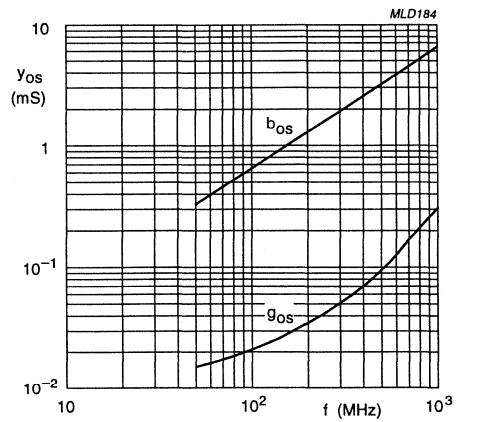
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.19 Reverse transfer admittance and phase as a function of frequency; typical values.



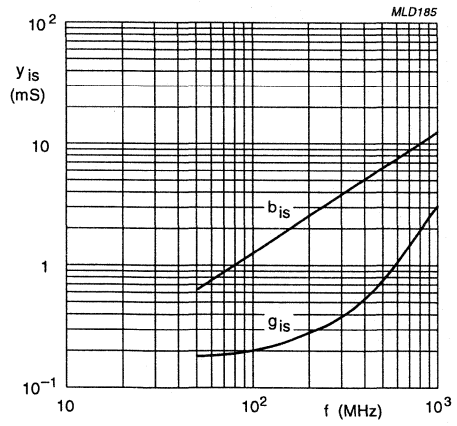
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Forward transfer admittance and phase as a function of frequency; typical values.



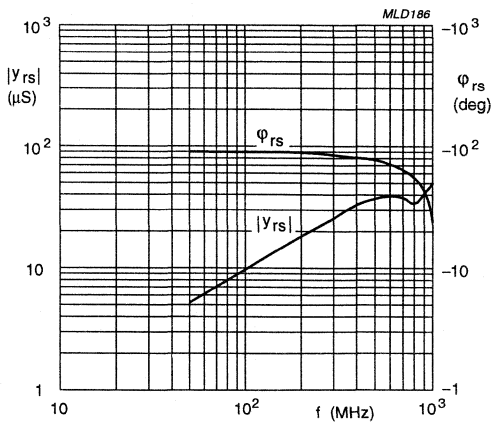
V_{DS} = 9 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance as a function of frequency; typical values.



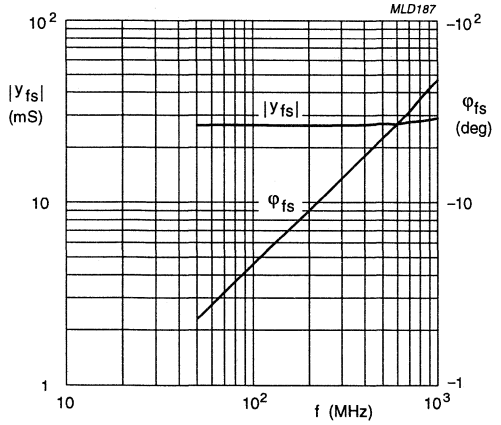
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.22 Input admittance as a function of frequency; typical values.



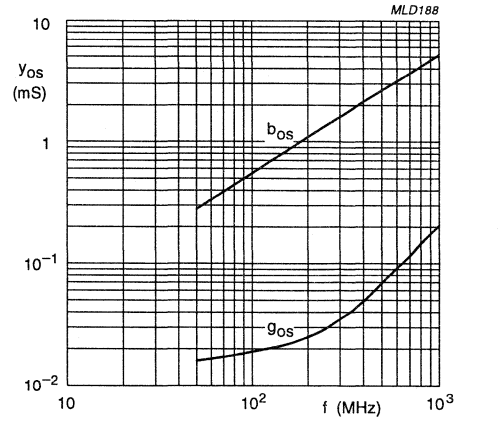
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.23 Reverse transfer admittance and phase as a function of frequency; typical values.



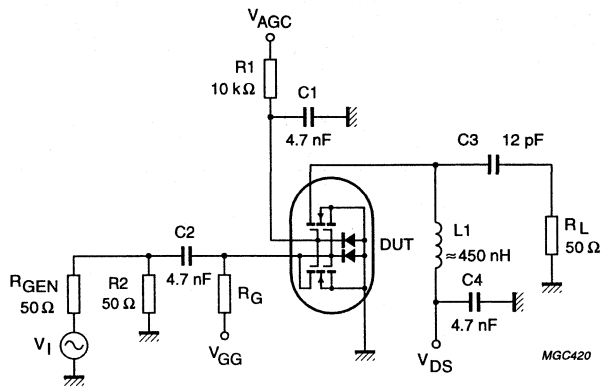
V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.24 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 12 V; V_{G2} = 4 V.
I_D = 10 mA; T_{amb} = 25 °C.

Fig.25 Output admittance as a function of frequency; typical values.



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ kΩ.
For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ kΩ.

Fig.26 Cross-modulation test circuit.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	–3.9	2.618	175.1	0.001	137.9	1.000	–1.9
100	0.981	–7.3	2.602	170.5	0.001	80.4	0.999	–4.0
200	0.975	–14.4	2.577	160.7	0.002	74.0	0.995	–7.6
300	0.965	–21.6	2.555	151.6	0.002	79.3	0.994	–11.3
400	0.947	–28.3	2.513	141.8	0.003	80.5	0.992	–15.0
500	0.927	–34.9	2.449	133.4	0.003	82.8	0.988	–18.5
600	0.913	–41.7	2.339	124.6	0.003	78.9	0.984	–22.0
700	0.890	–47.9	2.361	115.4	0.003	80.6	0.982	–25.3
800	0.869	–54.0	2.302	106.4	0.003	93.9	0.979	–28.8
900	0.845	–59.7	2.228	97.6	0.003	104.8	0.976	–32.1
1000	0.823	–65.4	2.167	89.6	0.003	129.3	0.974	–35.5

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	–3.7	2.576	175.3	0.000	125.0	1.000	–1.6
100	0.980	–7.4	2.563	170.9	0.001	111.2	1.000	–3.3
200	0.973	–14.6	2.541	161.6	0.002	83.0	0.997	–6.4
300	0.962	–21.5	2.519	152.9	0.002	85.2	0.996	–9.3
400	0.946	–28.5	2.479	143.5	0.003	79.4	0.995	–12.4
500	0.929	–35.0	2.419	135.5	0.003	78.2	0.991	–15.3
600	0.912	–41.6	2.373	127.2	0.003	80.0	0.989	–18.1
700	0.895	–47.8	2.336	118.7	0.003	83.4	0.987	–20.9
800	0.868	–53.8	2.284	110.0	0.003	91.3	0.985	–23.7
900	0.845	–59.8	2.213	101.6	0.003	95.9	0.983	–26.5
1000	0.823	–65.7	2.160	94.1	0.003	112.2	0.981	–29.3

Table 4 Noise data: V_{DS} = 12 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		10 to 40 mA
Transfer admittance I_D = 5 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert Y_{fs} \rvert$	>	6 mS
Feedback capacitance I_D = 5 mA; V_{DS} = 15 V; f = 1 MHz	C_{rs}	<	0,7 pF
Noise figure at f = 200 MHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C G_S = 1 mS; $B_S = B_{Sopt}$	F	<	5 dB
Equivalent noise voltage at f = 1 kHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C	$V_n\sqrt{B}$	typ.	100 $nV\sqrt{Hz}$

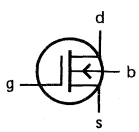
MECHANICAL DATA

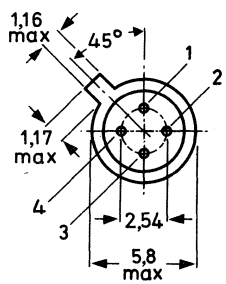
Dimensions in mm

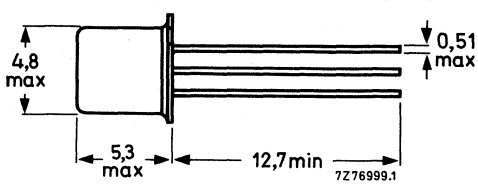
Fig. 1 TO-72.

Pinning

1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10	V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 −15	V V
Drain current (d.c.)	I_D	max.	20	mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0{,}1$	I_{DM}	max.	50	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to +	125	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Gate currents; $V_{BS} = 0$				
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	I_{GSS}	<	200	pA
Bulk currents; $V_{GB} = 0$				
$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	µA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	µA
Drain current				
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	10 to	40	mA
Gate-source voltage				
$I_D = 100$ nA; $V_{DS} = 15$ V	$-V_{GS}$	0.5 to	3.5	V

y parameters

$I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25\ ^oC$

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	6	mS
Output admittance at f = 1 kHz	$\|y_{os}\|$	<	0.4	mS
Input capacitance at f = 1 MHz	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	<	3	pF

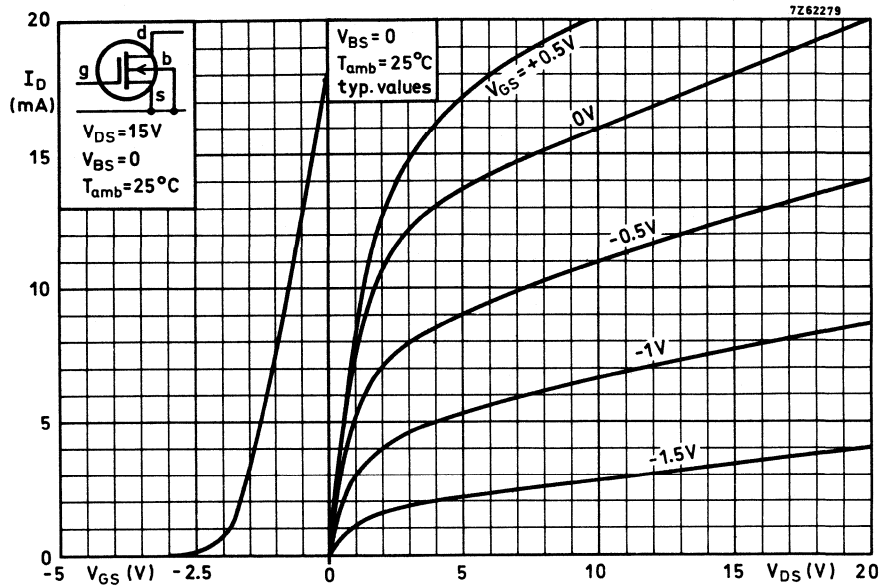
Noise figure at f = 200 MHz

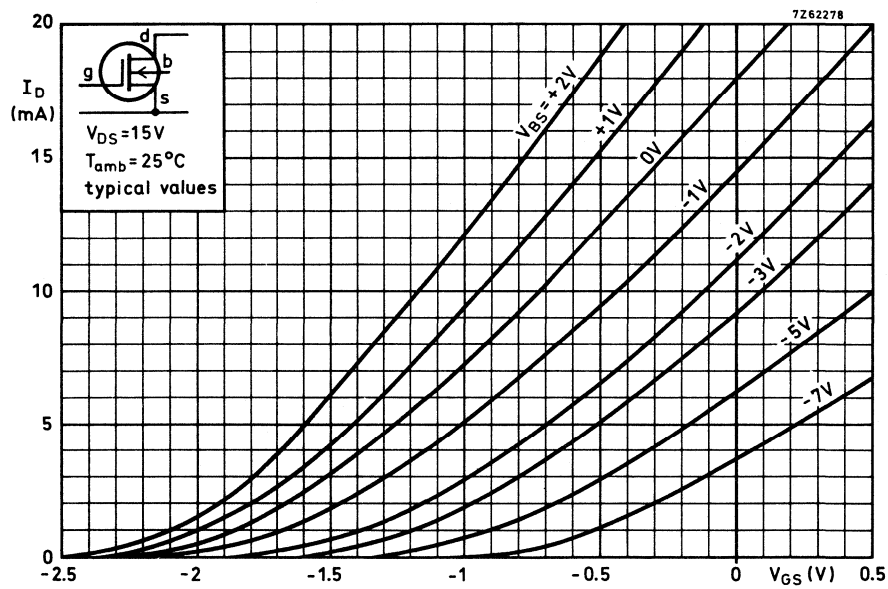
$I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25\ ^oC$

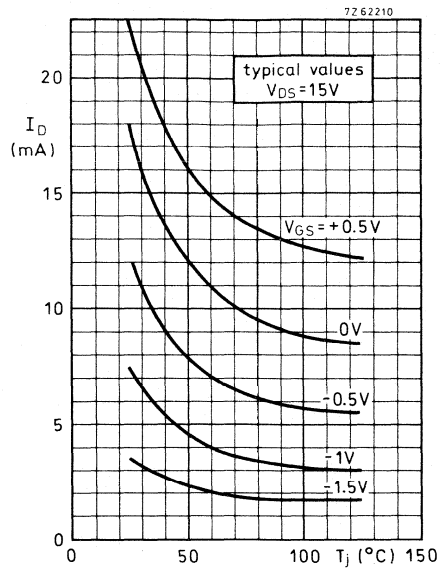
$G_S = 1$ mS; $B_S = B_{Sopt}$ F < 5 dB

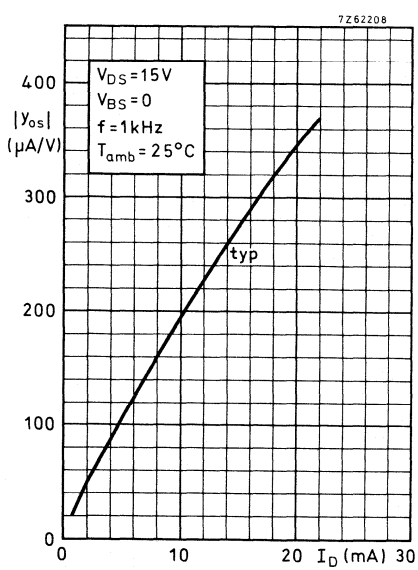
Equivalent noise voltage $T_{amb} = 25\ ^oC$

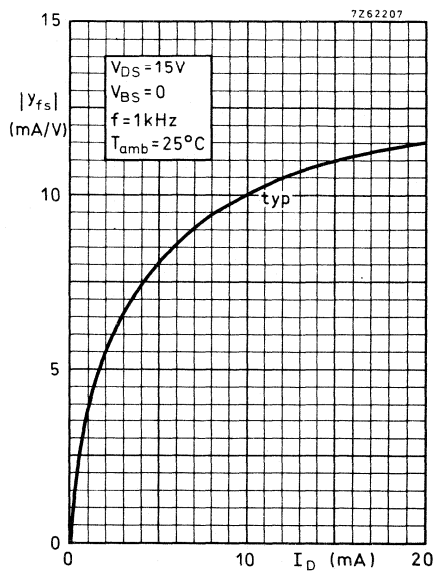
$I_D = 5$ mA; $V_{DS} = 15$ V; f = 120 Hz		$V_n/\sqrt{B}$	typ.	300	nV/$\sqrt{\text{Hz}}$
$T_{amb} = 25\ ^oC$	f = 1 kHz	$V_n/\sqrt{B}$	typ.	100	nV/$\sqrt{\text{Hz}}$
	f = 10 kHz	$V_n/\sqrt{B}$	typ.	35	nV/$\sqrt{\text{Hz}}$

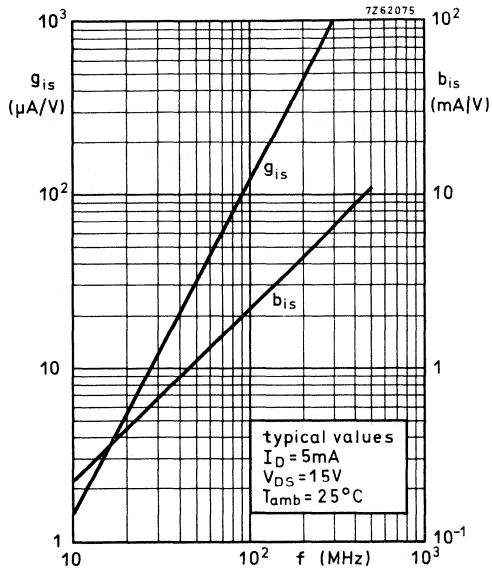

7Z62279
I_D (mA)
V_{DS}=15V
V_{BS}=0
T_{amb}=25°C
V_{BS}=0
T_{amb}=25°C
typ. values
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
V_{GS} (V)
V_{DS} (V)

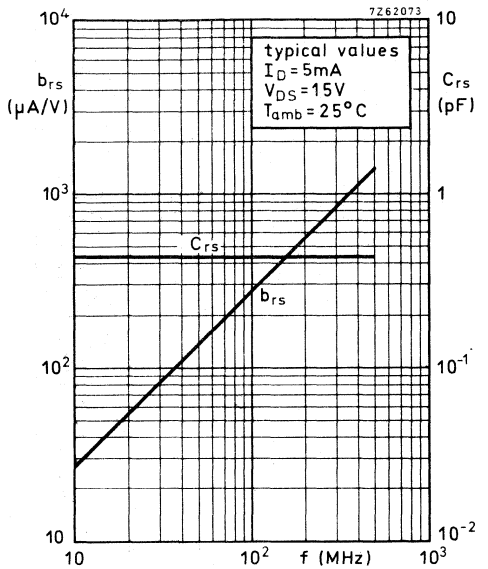

7Z62278
I_D (mA)
V_{DS}=15V
T_{amb}=25°C
typical values
V_{BS}=+2V
+1V
0V
-1V
-2V
-3V
-5V
-7V
V_{GS} (V)

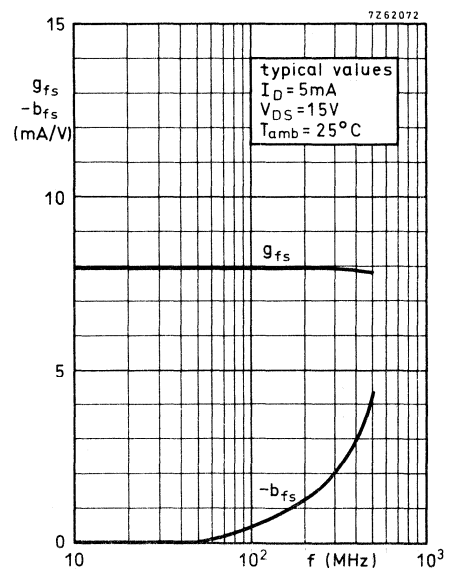

7Z62210
typical values
V_{DS}=15V
I_D (mA)
20
15
10
5
0
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
0
50
100
T_j (°C)
150

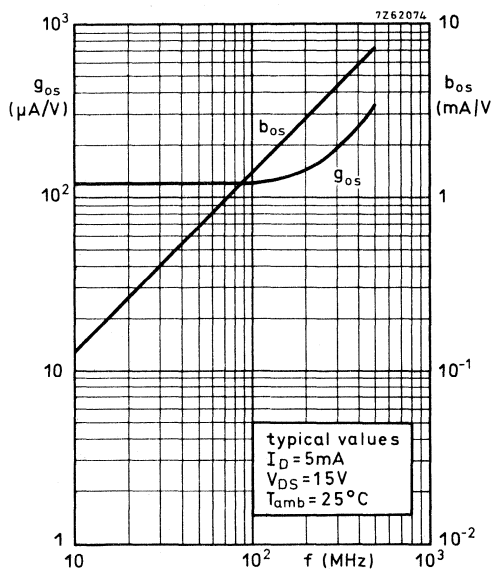

7Z62208
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{os}|$ (μA/V)
400
300
200
100
0
typ
0
10
20
I_D (mA)
30

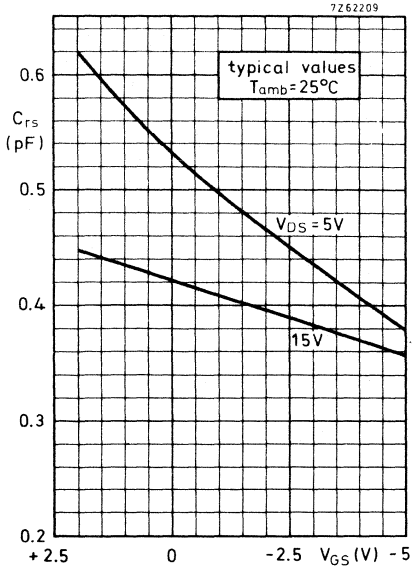

7Z62207
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{fs}|$ (mA/V)
15
10
5
0
typ
0
10
I_D (mA)
20

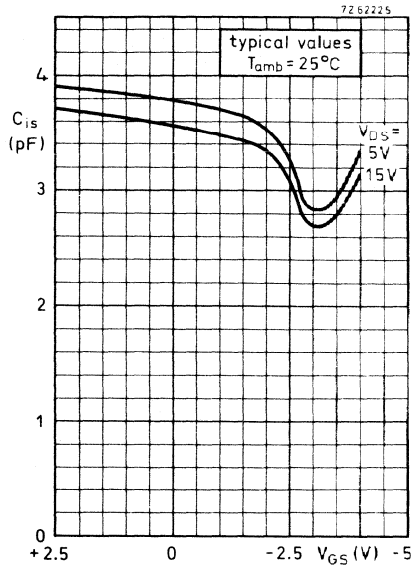

7Z62075
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


7Z62073
b_{rs} (μA/V)
C_{rs} (pF)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
C_{rs}
b_{rs}
f (MHz)


7Z62072
g_{fs} $-b_{fs}$ (mA/V)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
f (MHz)


7Z62074
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


7Z62209
typical values
T_{amb}=25°C
C_{rs} (pF)
0.6
0.5
0.4
0.3
0.2
V_{DS} = 5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5


7Z62225
typical values
T_{amb} = 25°C
C_{is} (pF)
4
3
2
1
0
V_{DS} =
5V
15V
+2.5
0
-2.5
V_{GS} (V)
-5

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial symmetrical junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

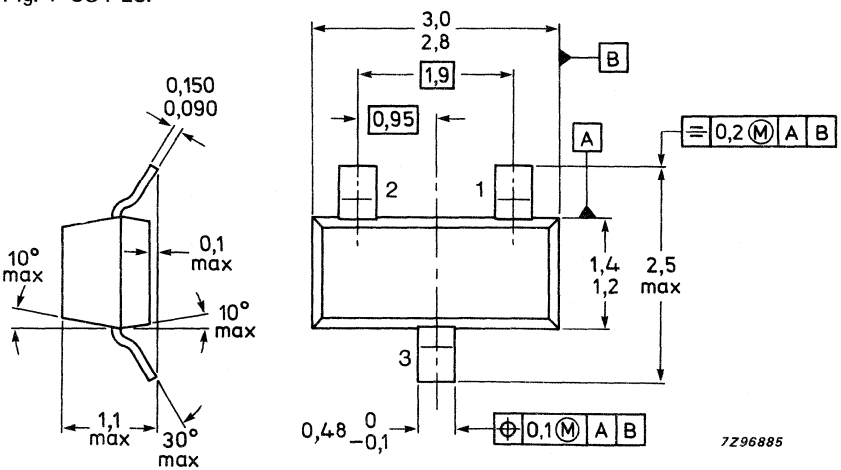
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25		V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250		mW
			BFR30	BFR31	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Transfer admittance (common source) I_D = 1 mA; V_{DS} = 10 V; f = 1 kHz	$\|Y_{fs}\|$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS

MECHANICAL DATA

Fig. 1 SOT-23.

Dimensions in mm



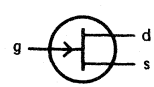
TOP VIEW

Marking code

BFR30 = M1p
BFR31 = M2p

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 40 °C*	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BFR30	BFR31	
Gate cut-off current					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	max.	0.2	0.2	nA
Drain current					
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Gate-source voltage					
I_D = 1 mA; V_{DS} = 10 V	$-V_{GS}$	min.	0.7	0	V
		max.	3.0	1.3	V
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	max.	4.0	2.0	V
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	max.	5	2.5	V
y parameters					
Transfer admittance at f = 1 kHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min.	0.5	0.75	mS
Output admittance at f = 1 kHz					
I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{os}\rvert$	max.	40	25	μS
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{os}\rvert$	max.	20	15	μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

y parameters (continued)

			BFR30	BFR31	
Input capacitance at f = 1 MHz					
I_D = 1 mA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
I_D = 200 μA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
Feedback capacitance at f = 1 MHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
I_D = 200 μA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 10 V B = 0.6 to 100 Hz	V_n	max.	0.5	0.5	μV

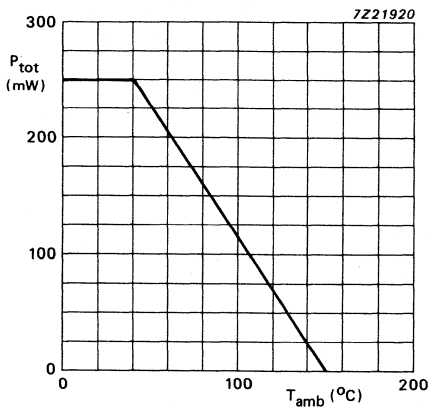


Fig.2 Power derating curve.

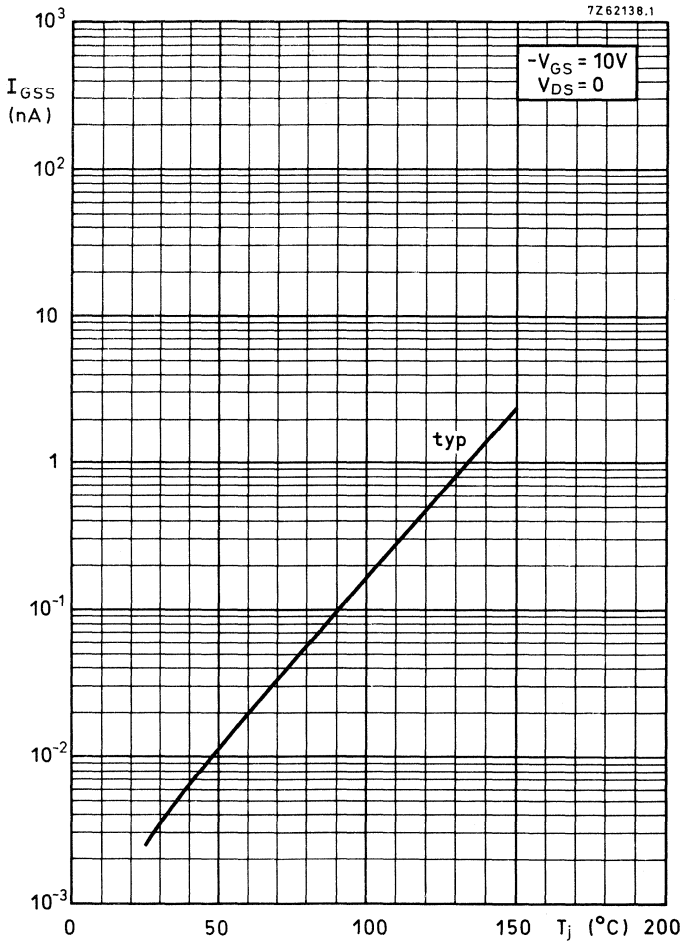

7Z62138.1
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

Fig.3.

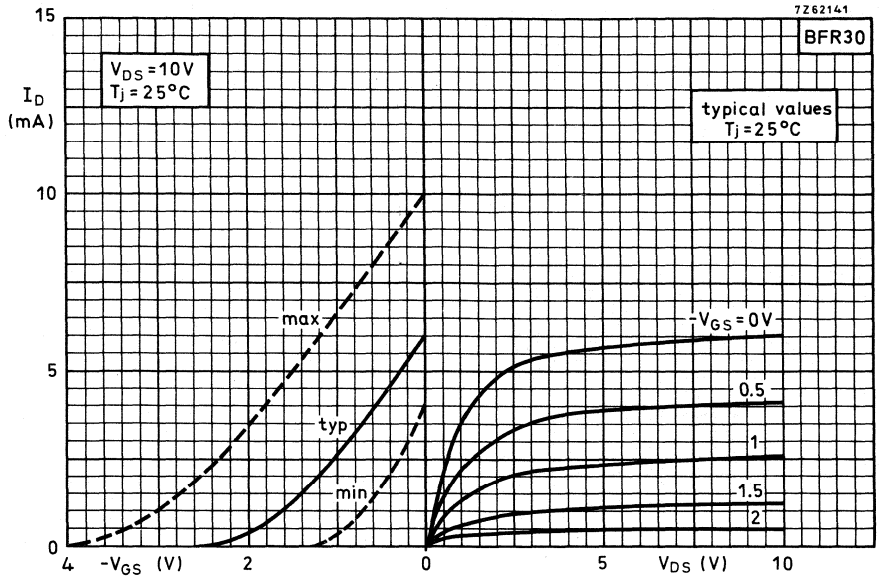

7Z62141
BFR30
V_{DS} = 10 V
T_j = 25 °C
typical values
T_j = 25 °C
I_D (mA)
15
10
5
0
max
typ
min
$-V_{GS}$ = 0 V
0.5
1
1.5
2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

Fig.4.

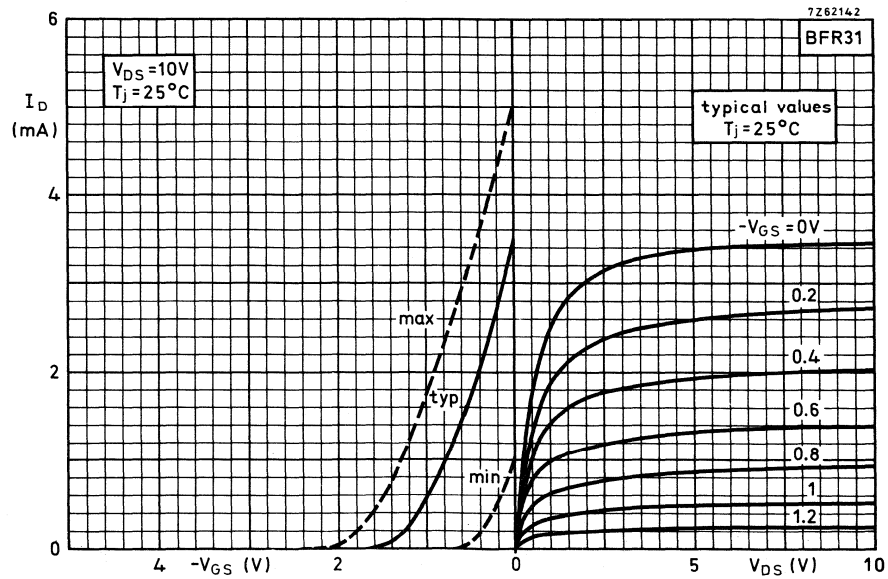

7Z62142
BFR31
V_{DS} = 10 V
T_j = 25 °C
typical values
T_j = 25 °C
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0 V
0.2
0.4
0.6
0.8
1
1.2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

Fig.5.

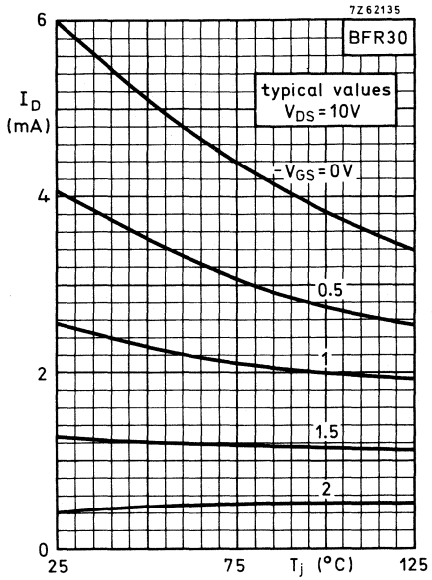


Fig.6.

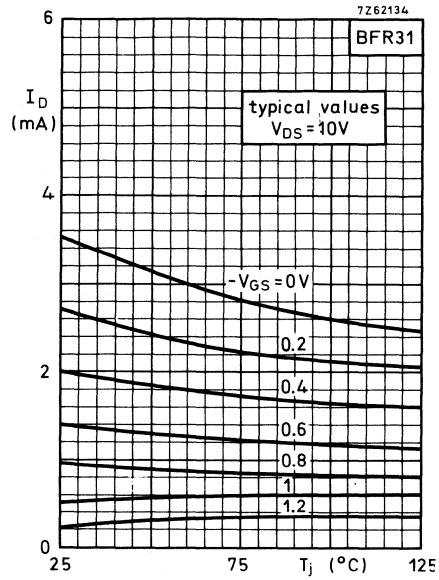


Fig.7.

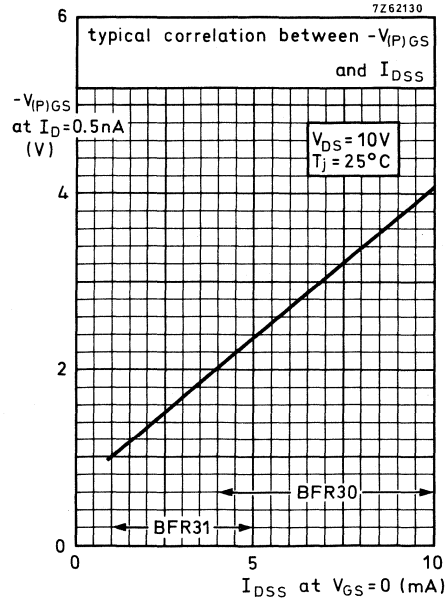


Fig.8.

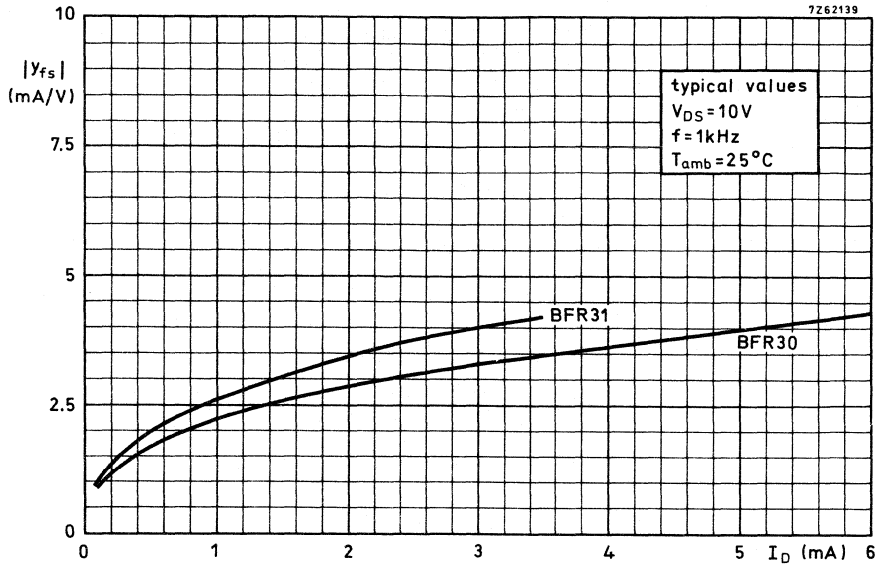

7Z62139
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS=10V
f=1kHz
Tamb=25°C
BFR31
BFR30
0
1
2
3
4
5
ID (mA)
6

Fig.9.

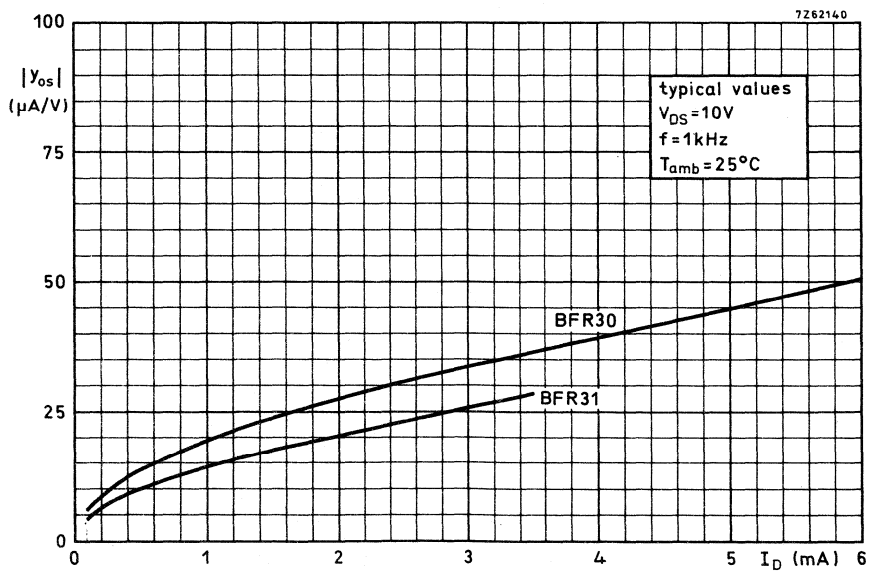

7Z62140
100
|yos|
(μA/V)
75
50
25
0
typical values
VDS=10V
f=1kHz
Tamb=25°C
BFR30
BFR31
0
1
2
3
4
5
ID (mA)
6

Fig.10.

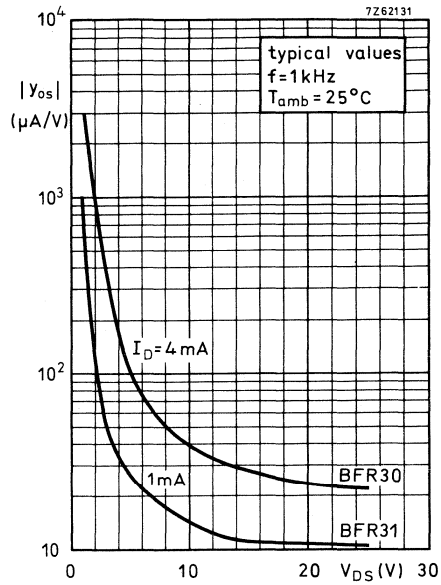


Fig.11.

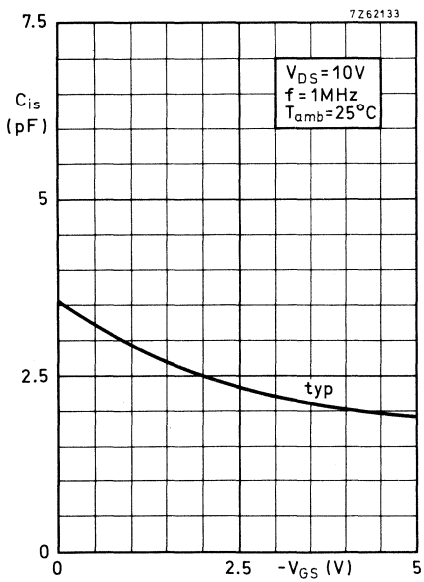


Fig.12.

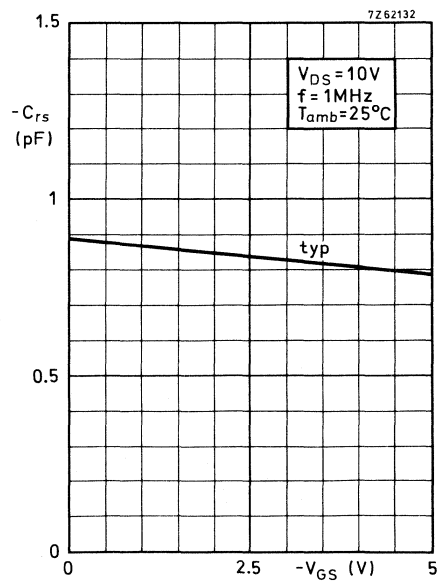


Fig.13.

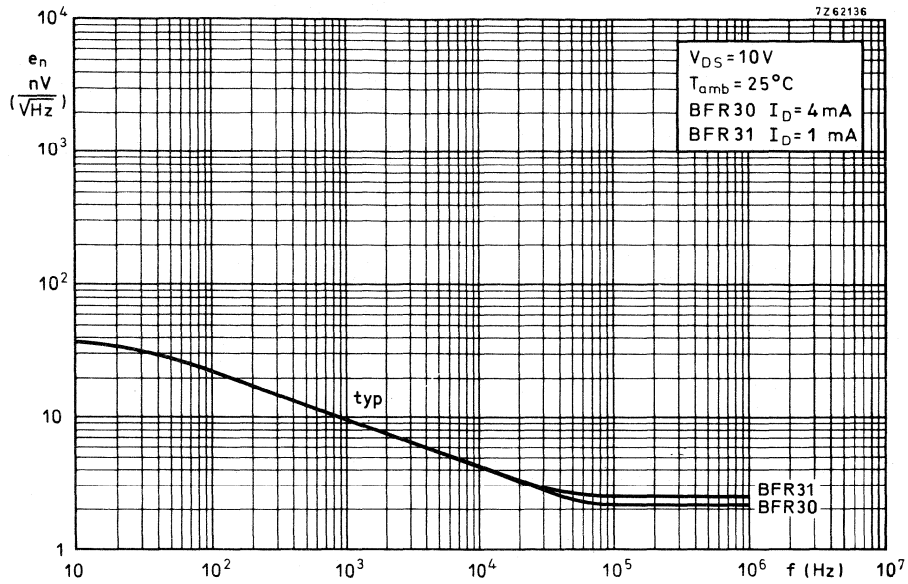

7Z62136
10^4
e_n
nV
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 10 V
T_{amb} = 25 °C
BFR30 I_D = 4 mA
BFR31 I_D = 1 mA
typ
BFR31
BFR30
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

Fig.14.

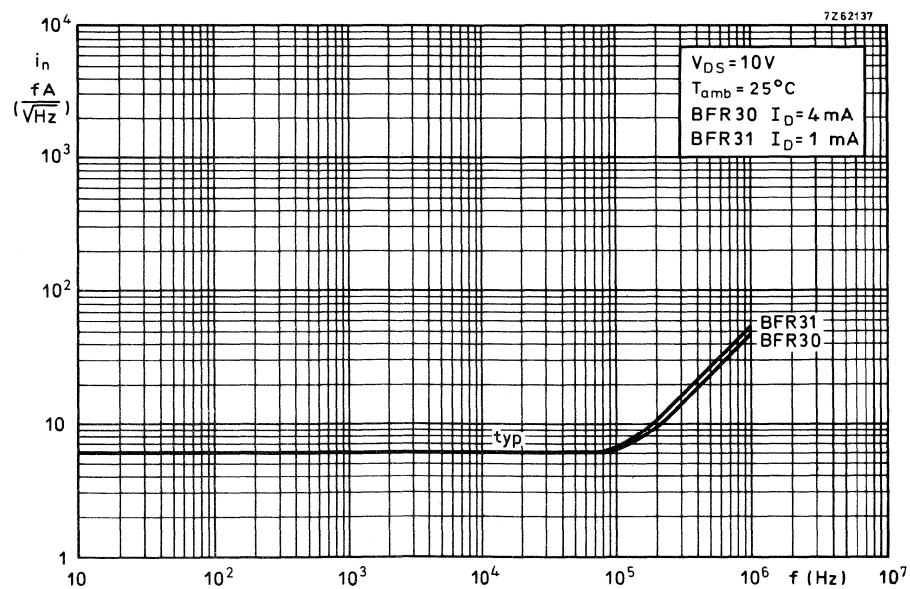

7Z62137
10^4
i_n
fA
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 10 V
T_{amb} = 25 °C
BFR30 I_D = 4 mA
BFR31 I_D = 1 mA
BFR31
BFR30
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

Fig.15.

N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

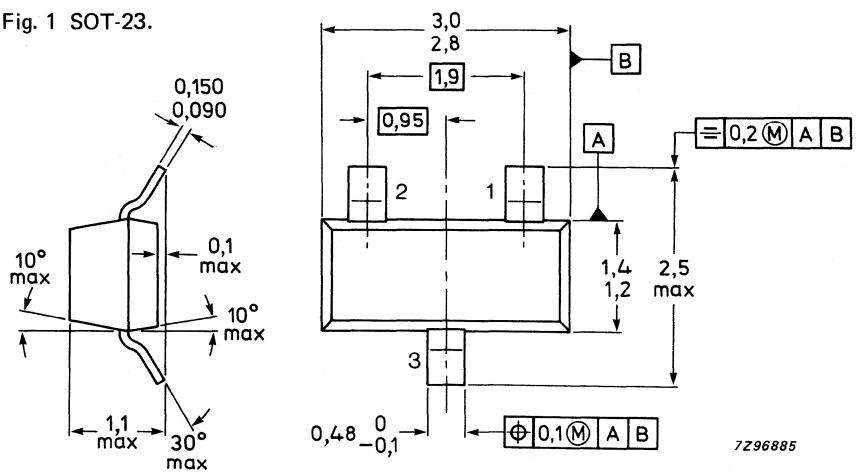
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250 mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	> <	0,2 mA 1,5 mA
Transfer admittance (common source) I_D = 0,2 mA; V_{DS} = 10 V; f = 1 kHz	$\|y_{fs}\|$	>	0,5 mS
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; B = 0,6 to 100 Hz	V_n	<	0,5 μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



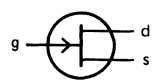
TOP VIEW

Marking code

BFT46 = M3

Pinning

1 = drain
2 = source
3 = gate



Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to	+150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2	nA
Drain current				
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2	mA
		<	1,5	mA
Gate-source voltage				
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	>	0,1	V
		<	1,0	V
Gate-source cut-off voltage				
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2	V
y-parameters at f = 1 kHz;				
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C				
Transfer admittance	$\lvert y_{fs}\rvert$	>	1,0	mS
Output admittance	$\lvert y_{os}\rvert$	<	10	μS
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C				
Transfer admittance	$\lvert y_{fs}\rvert$	>	0,5	mS
Output admittance	$\lvert y_{os}\rvert$	<	5	μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	<	1,5 pF
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C B = 0,6 to 100 Hz	V_n	<	0,5 μV

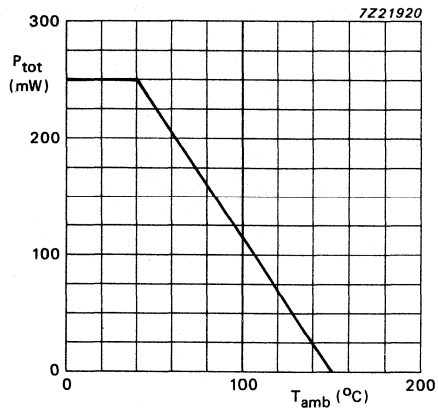


Fig.2 Power derating curve.

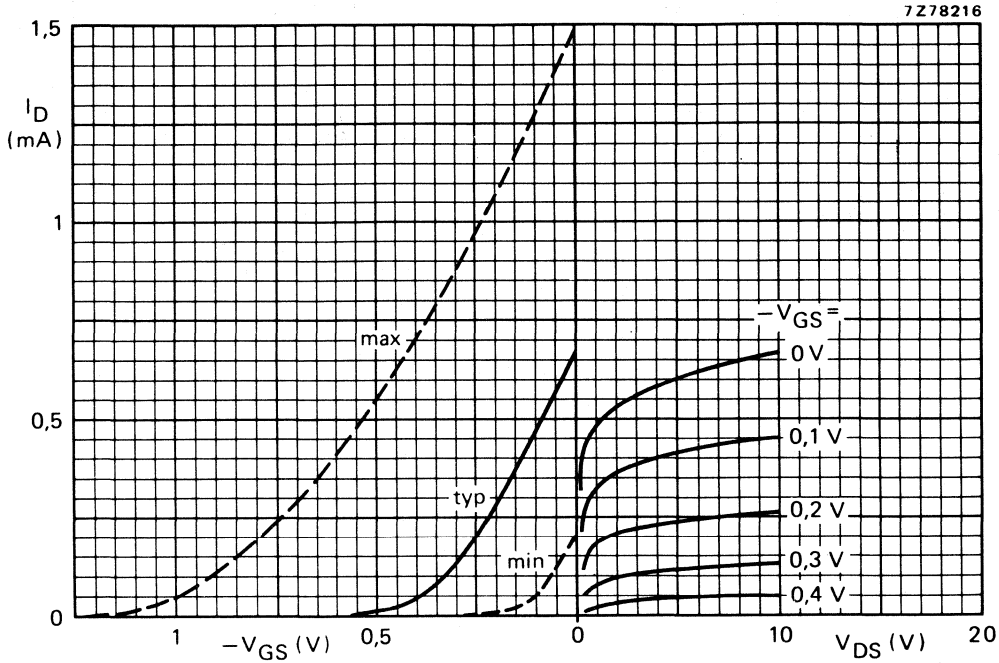


Fig. 3 Typical values. V_{DS} = 10 V; T_j = 25 °C.

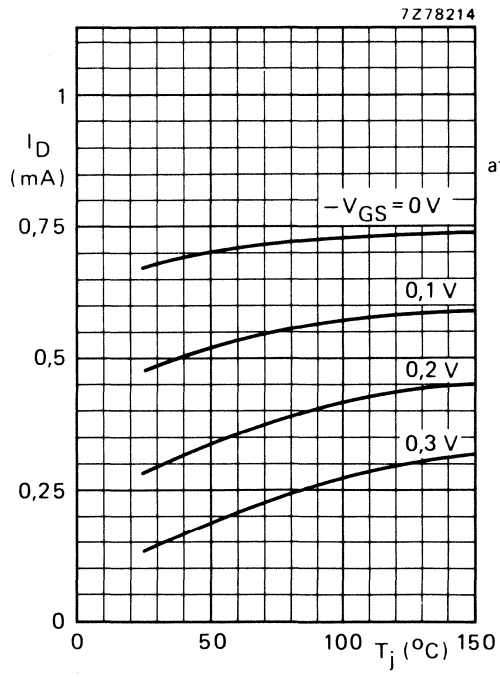


Fig. 4 Typical values. V_{DS} = 10 V.

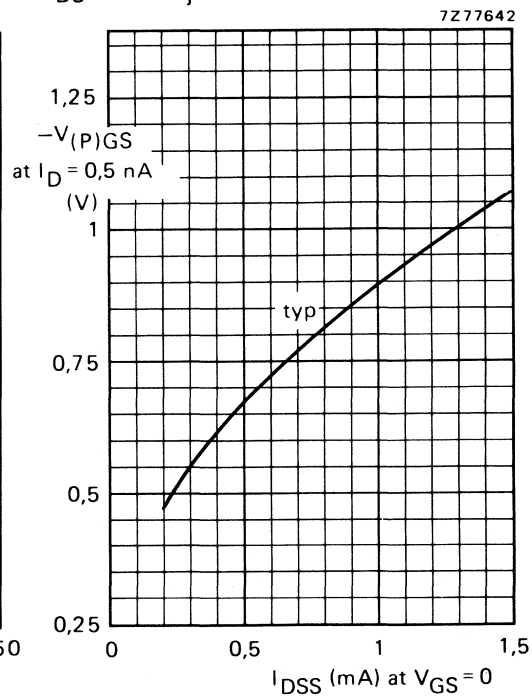


Fig. 5 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

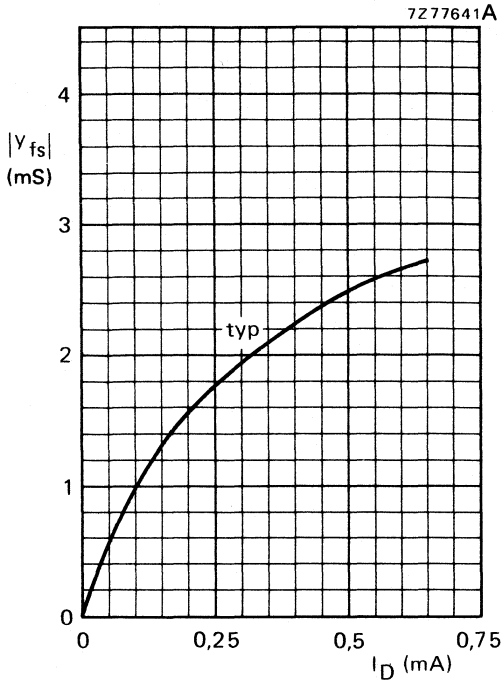


Fig. 6

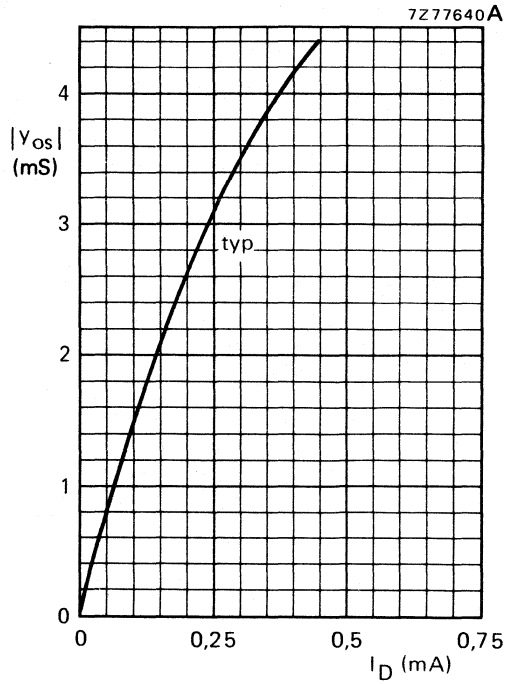


Fig. 7

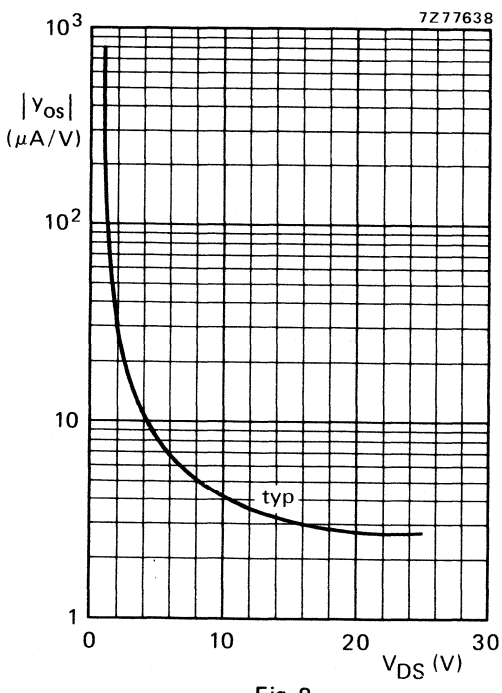


Fig. 8

Fig. 6 $|y_{fs}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 7 $|y_{os}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 8 $|y_{os}|$ versus V_{DS}.
I_D = 0,4 mA; f = 1 kHz; T_{amb} = 25 °C.

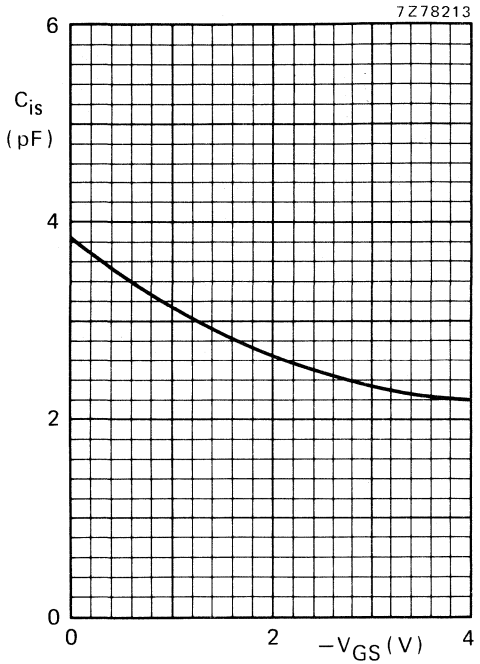


Fig. 9

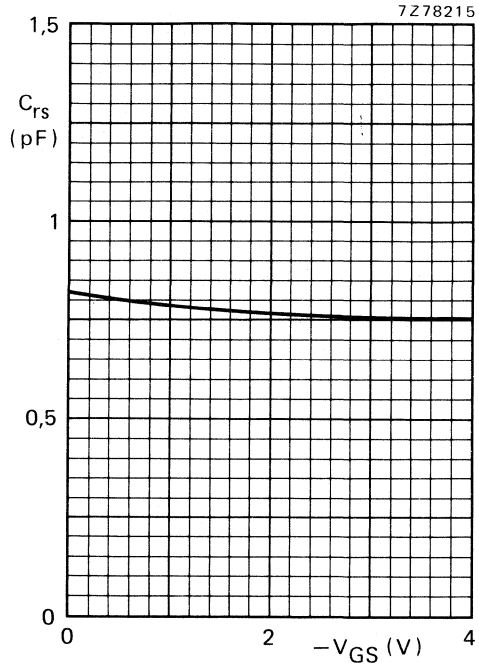


Fig. 10

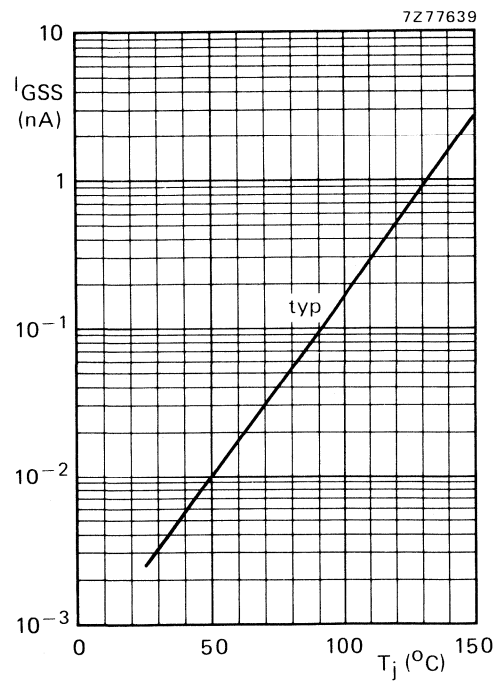


Fig. 11

Fig. 9 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 11 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

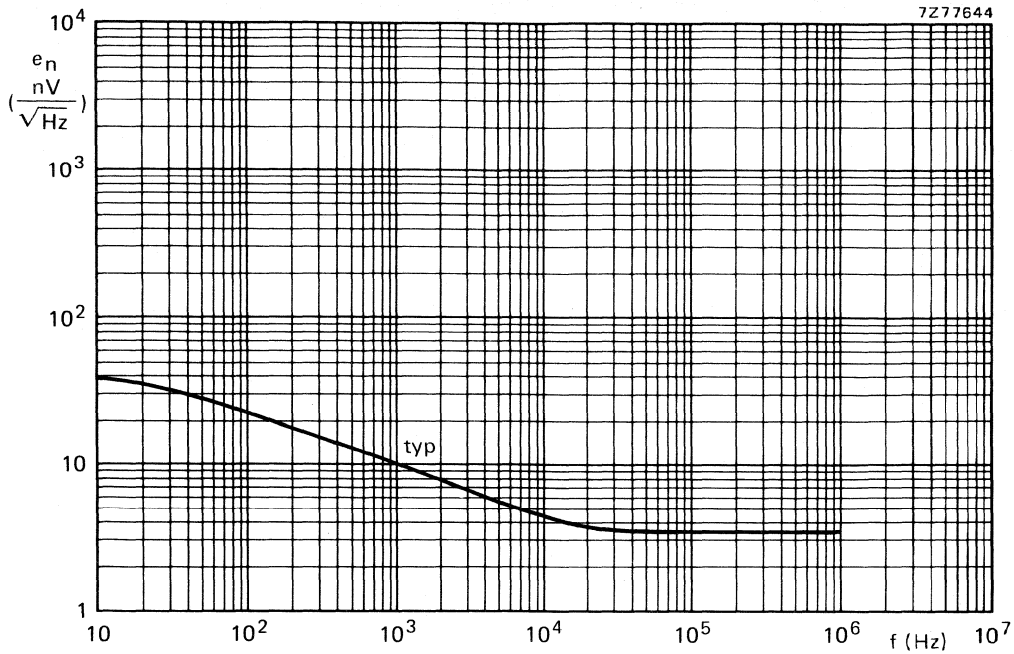


Fig. 12 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

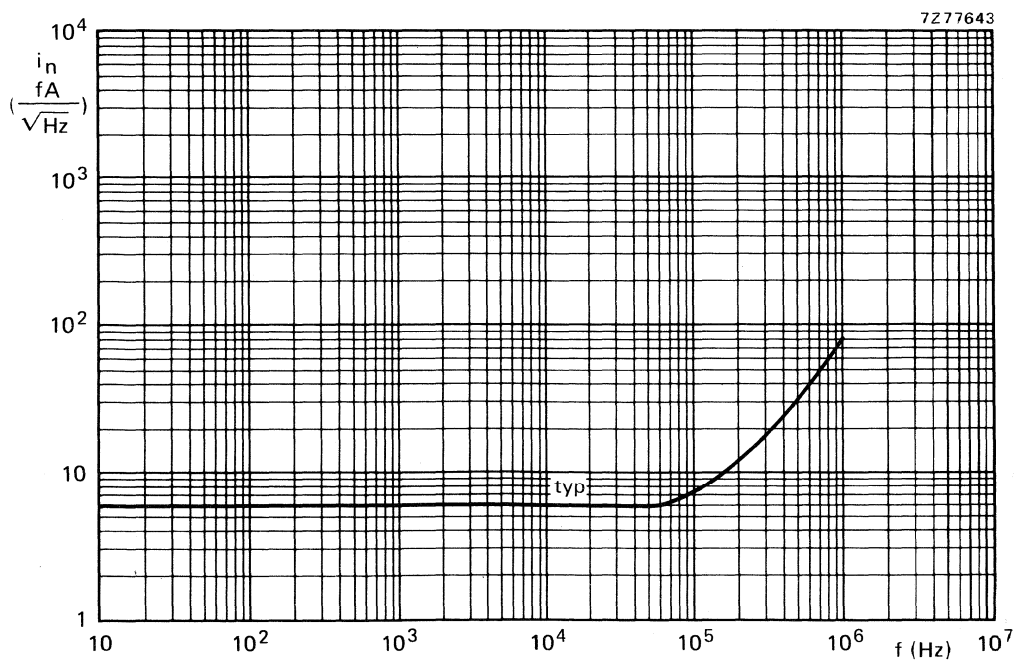


Fig. 13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

N-channel silicon field-effect transistors

BFU308/309/310

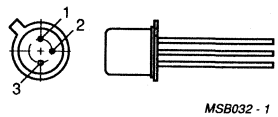
FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-18 envelope. They are intended for use in UHF/VHF amplifiers, oscillators and mixers.

PIN CONFIGURATION



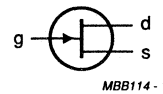


Fig.1 Simplified outline and symbol.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	BFU308		12	60	mA
	BFU309		12	30	mA
	BFU310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	275	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 µA			
	BFU308		1	6.5	V
	BFU309		1	4	V
	BFU310		2	6.5	V
Y_{fs}	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	275	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	360	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead minimum 10 x 10 mm.

STATIC CHARACTERISTICS

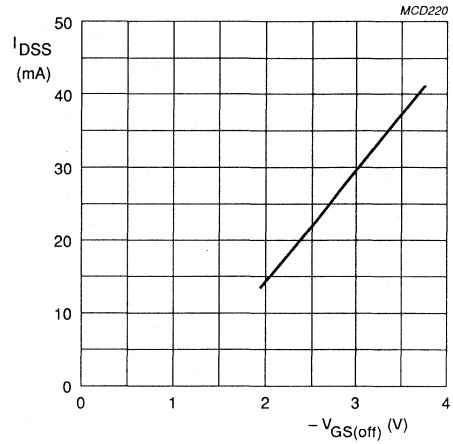
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	–	–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	BFU308		12	–	60	mA
	BFU309		12	–	30	mA
	BFU310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	BFU308		1	–	6.5	V
	BFU309		1	–	4	V
	BFU310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\lvert Y_{fs}\rvert$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\lvert Y_{os}\rvert$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

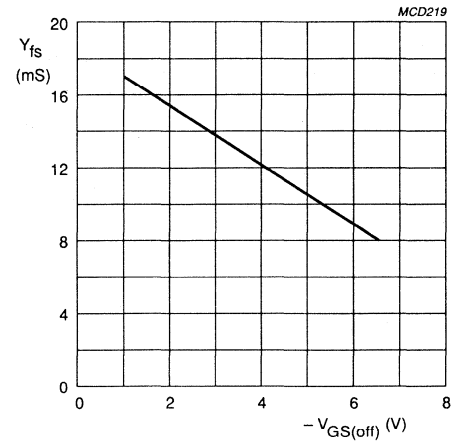
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\overline{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



BFU308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

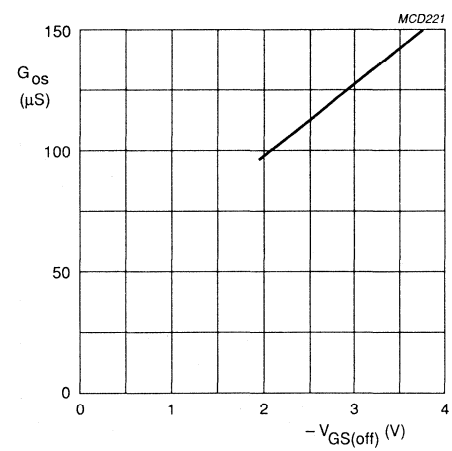
Fig.2 Drain current as a function of gate-source cut-off voltage.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

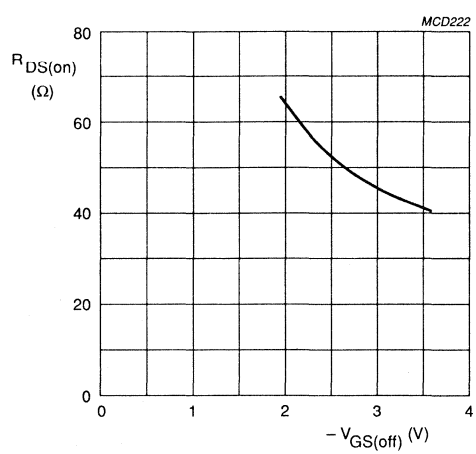
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

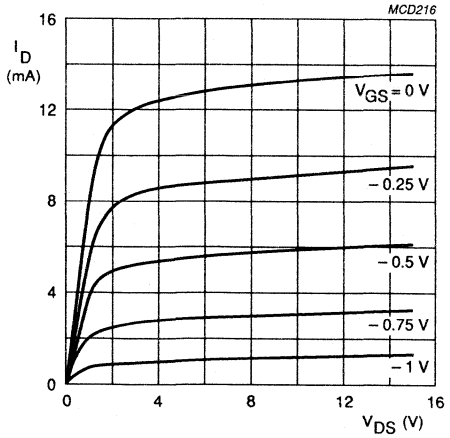
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



BFU308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

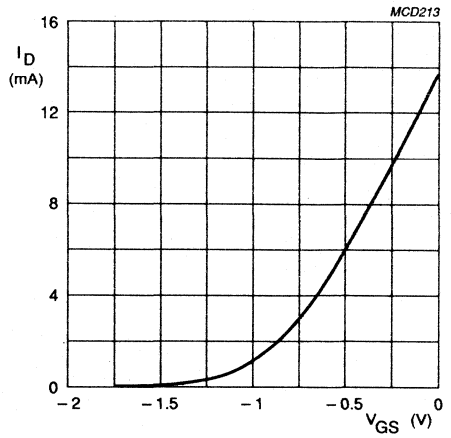
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



BFU308.

T_j = 25 °C.

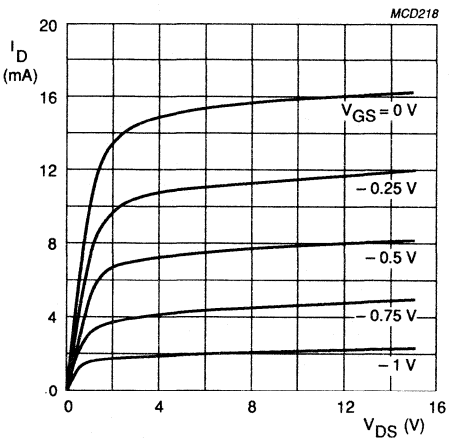
Fig.6 Output characteristics, typical values.



BFU308.

V_{DS} = 10 V; T_j = 25 °C.

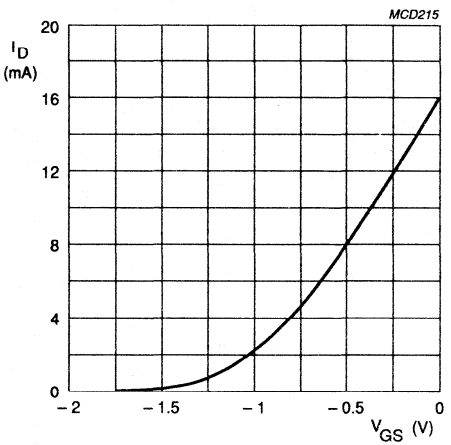
Fig.7 Input characteristics, typical values.



BFU309.

T_j = 25 °C.

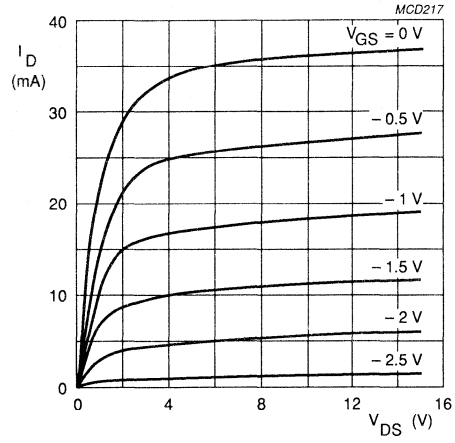
Fig.8 Output characteristics, typical values.



BFU309.

V_{DS} = 10 V; T_j = 25 °C.

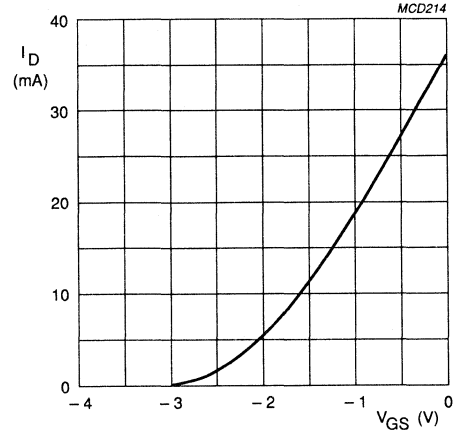
Fig.9 Input characteristics, typical values.



BFU310.

T_j = 25 °C.

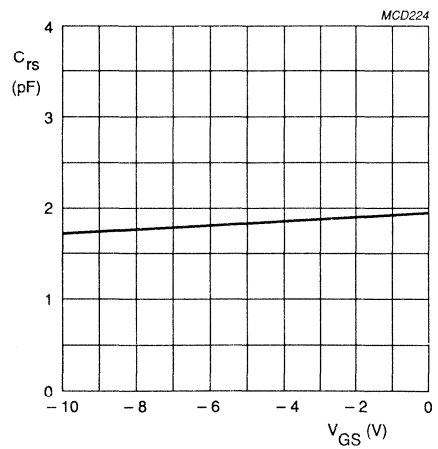
Fig.10 Output characteristics, typical values.



BFU310.

V_{DS} = 10 V; T_j = 25 °C.

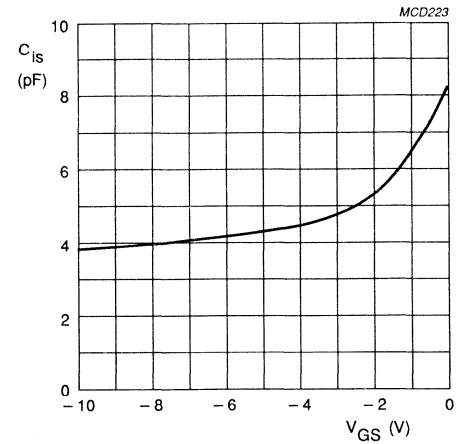
Fig.11 Input characteristics, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

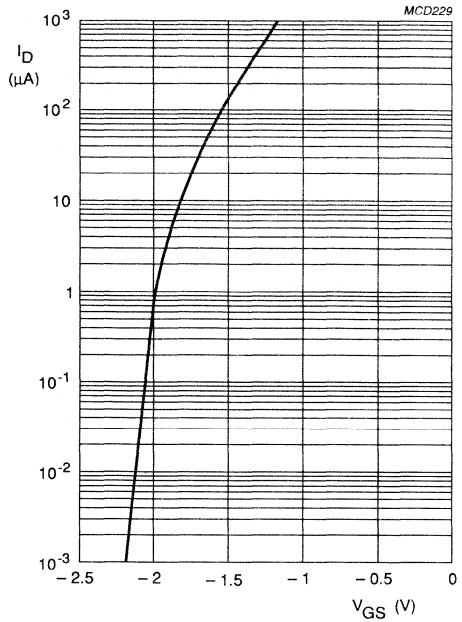
Fig.12 Feedback capacitance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

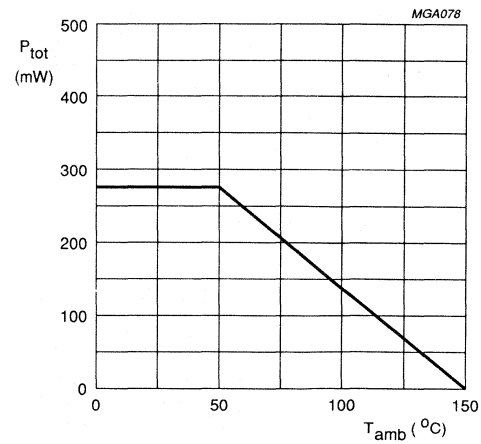
Fig.13 Input capacitance, typical values.



BFU308, 309 & 310.

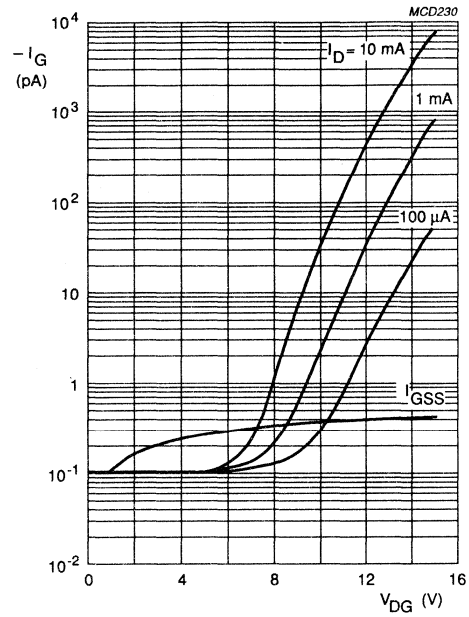
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



BFU308, 309 & 310.

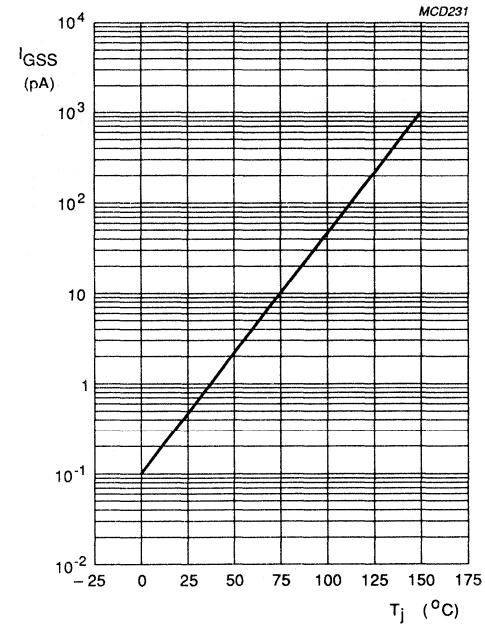
Fig.15 Power derating curve.



BFU308, 309 & 310.

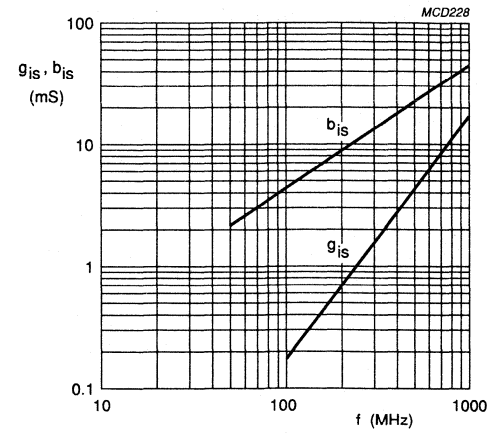
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



BFU308, 309 & 310.

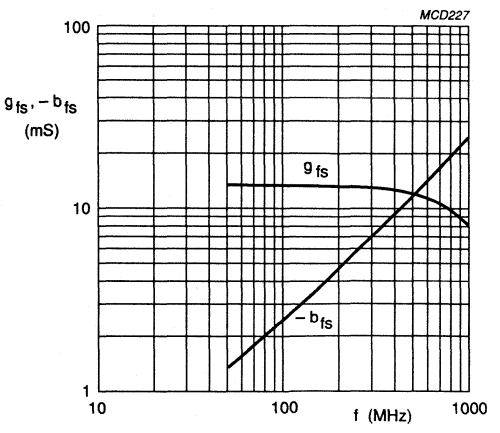
Fig.17 Gate current as a function of junction temperature, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

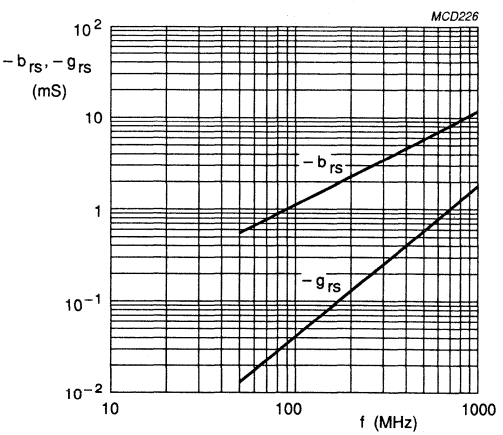
Fig.18 Input admittance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

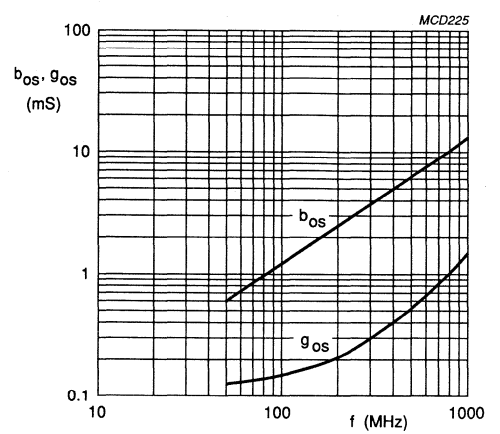
Fig.19 Forward admittance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



BFU308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250		mW
			BFW10	**BFW11**	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2	3,2	mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0					
f = 100 MHz; R_G = 1 kΩ	F	<	2,5	2,5	dB
Equivalent noise voltage					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

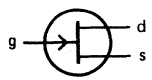
MECHANICAL DATA

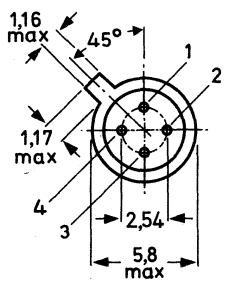
Dimensions in mm

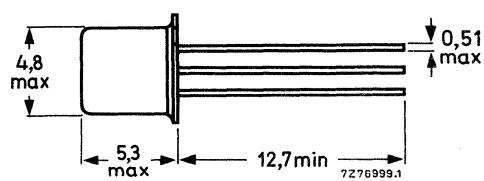
Fig.1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

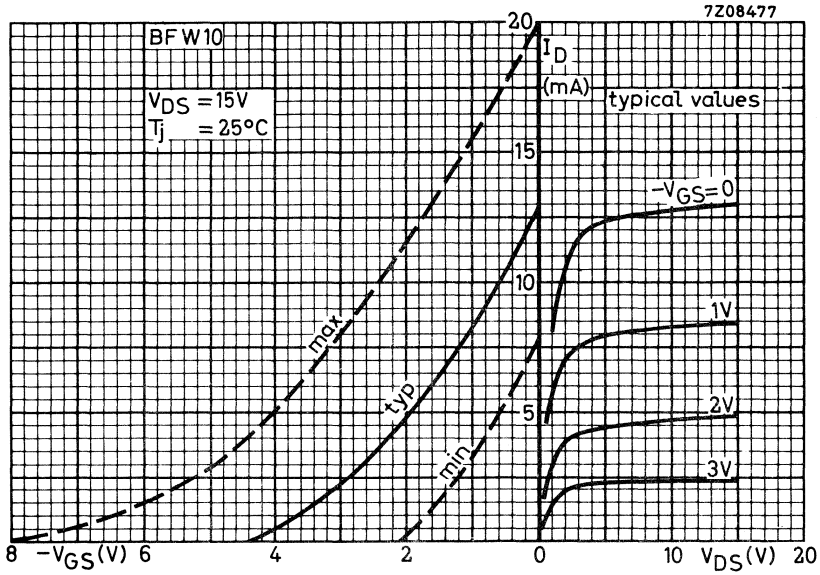
From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

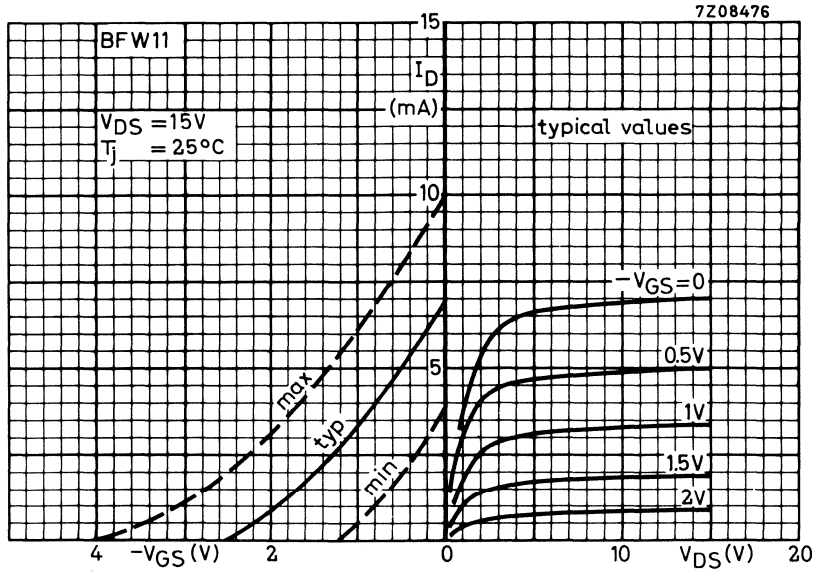
CHARACTERISTICS

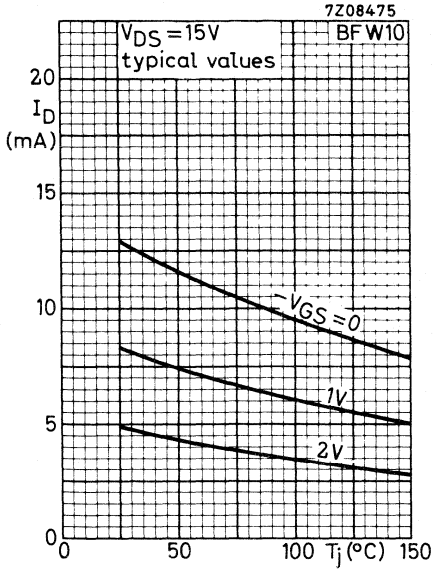
T_j = 25 °C unless otherwise specified

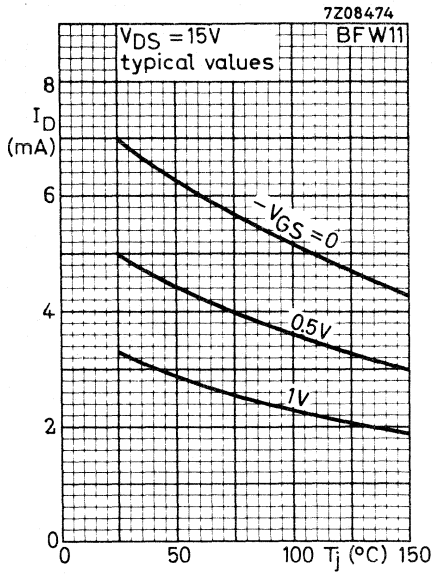
			BFW10	BFW11	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current*					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 1 kHz					
Transfer admittance	$\lvert y_{fs} \rvert$	>	3.5	3.0	mS
		<	6.5	6.5	mS
Output admittance	$\lvert y_{os} \rvert$	<	85	50	μS
f = 1 MHz; input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	C_{rs}	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz; transfer admittance	$\lvert y_{fs} \rvert$	>	3.2	3.2	mS
Input capacitance	g_{is}	<	800	800	μS
Output capacitance	g_{os}	<	200	100	μS
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

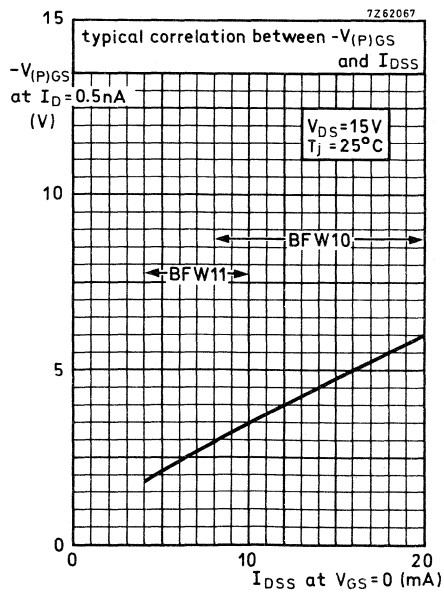
* Measured under pulsed conditions.

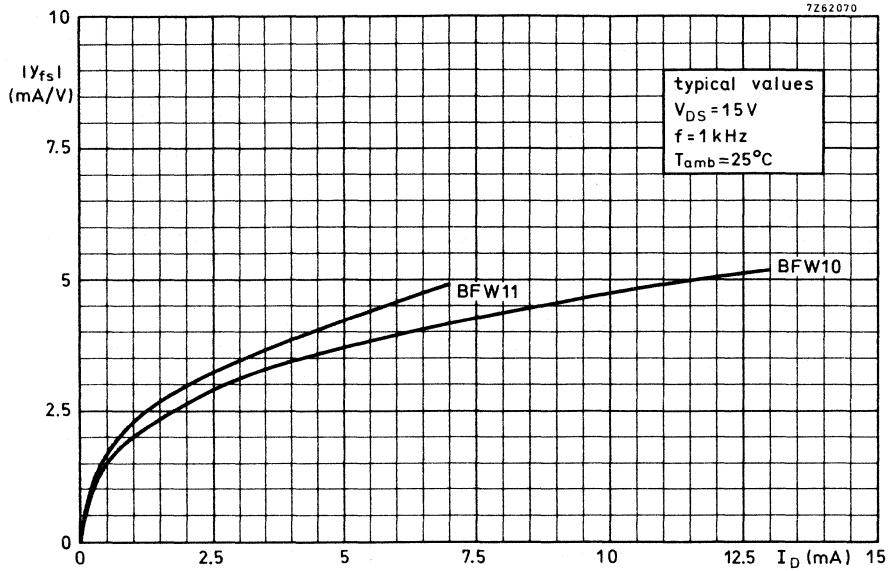

7Z08477
BFW10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
1V
2V
3V
max
typ
min
20
15
10
5
8
$-V_{GS}$(V)
6
4
2
0
10
V_{DS}(V)
20

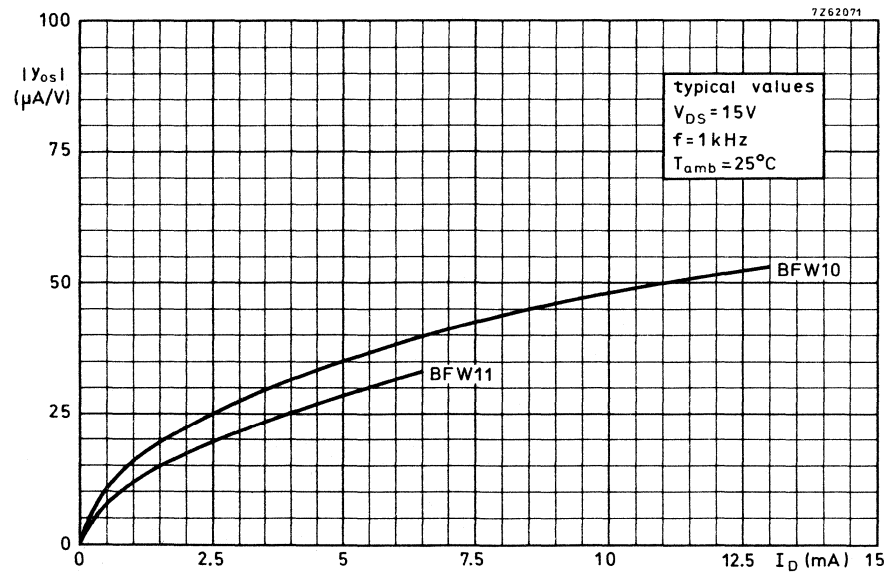

7Z08476
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
15
10
5
4
$-V_{GS}$(V)
2
0
10
V_{DS}(V)
20

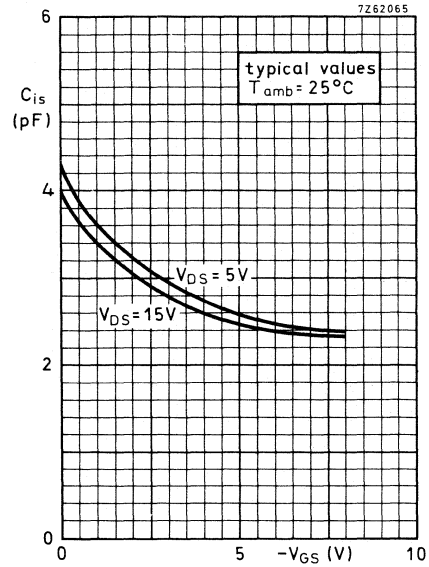

7Z08475
V_{DS} = 15V
typical values
BFW10
I_D (mA)
20
15
10
5
0
0
50
100
T_j (°C)
150
$-V_{GS}$ = 0
1V
2V

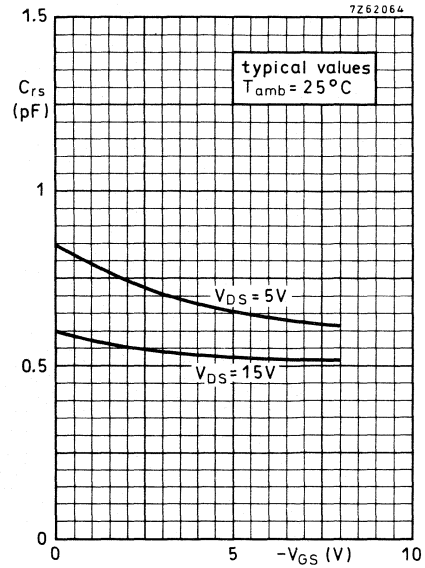

7Z08474
V_{DS} = 15V
typical values
BFW11
I_D (mA)
8
6
4
2
0
0
50
100
T_j (°C)
150
$-V_{GS}$ = 0
0.5V
1V

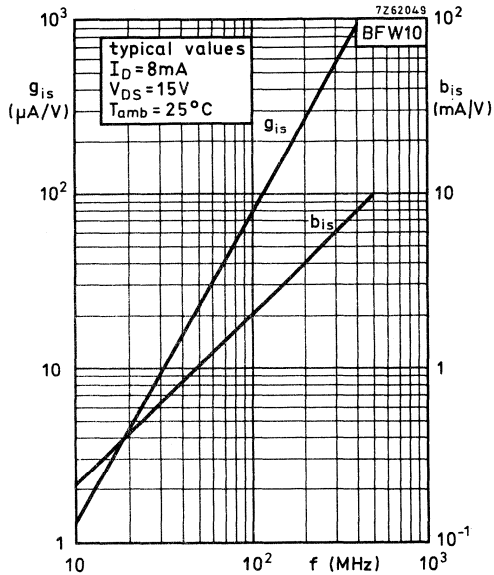

7Z62067
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15V
T_j = 25°C
BFW10
BFW11
15
10
5
0
0
10
20
I_{DSS} at V_{GS} = 0 (mA)

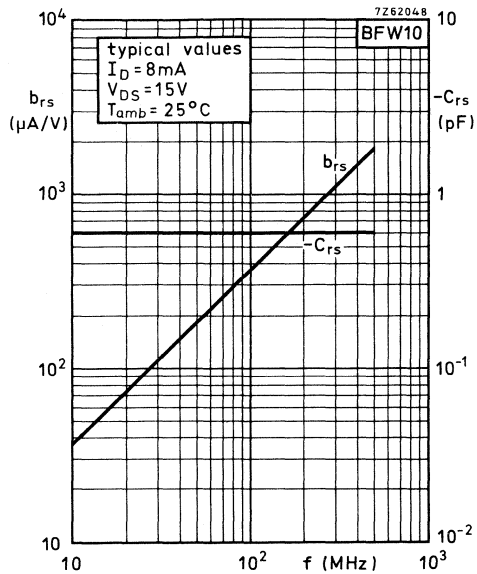

7Z62070
10
$|y_{fs}|$ (mA/V)
7.5
5
2.5
0
typical values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
I_D (mA)
15

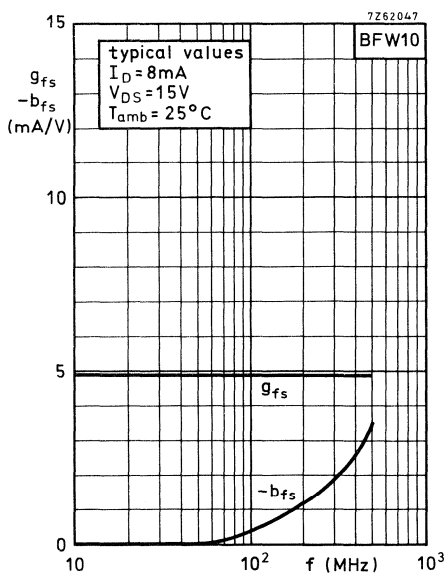

7Z62071
100
$|y_{os}|$ (μA/V)
75
50
25
0
typical values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
I_D (mA)
15

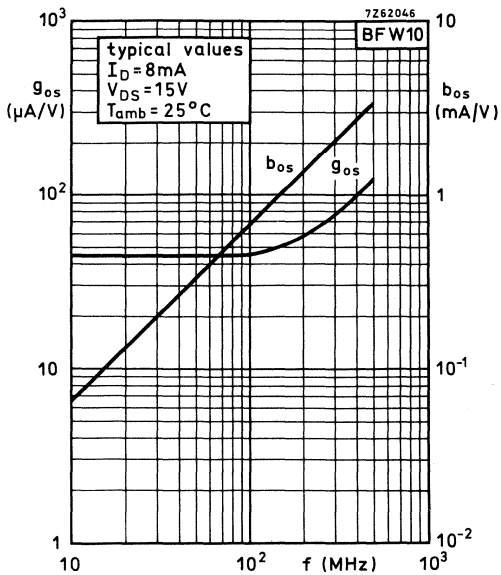

7Z62065
typical values
T_{amb} = 25 °C
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

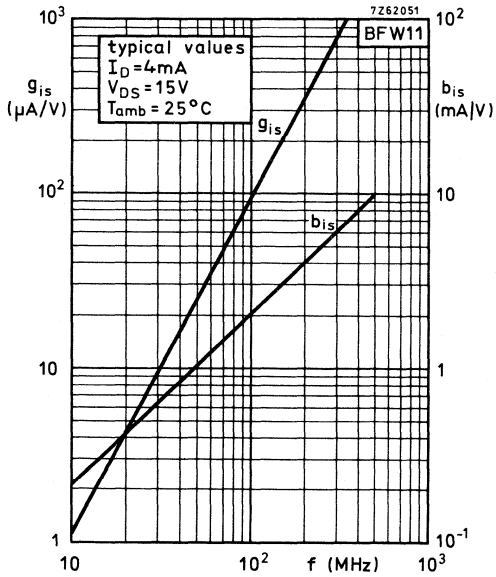

7Z62064
typical values
T_{amb} = 25 °C
C_{rs} (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

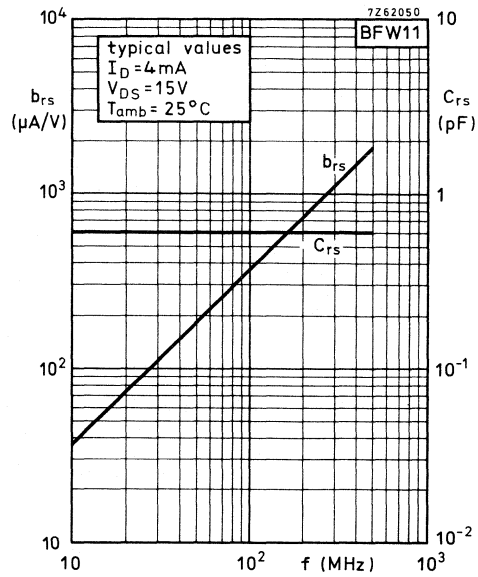

7Z62049
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

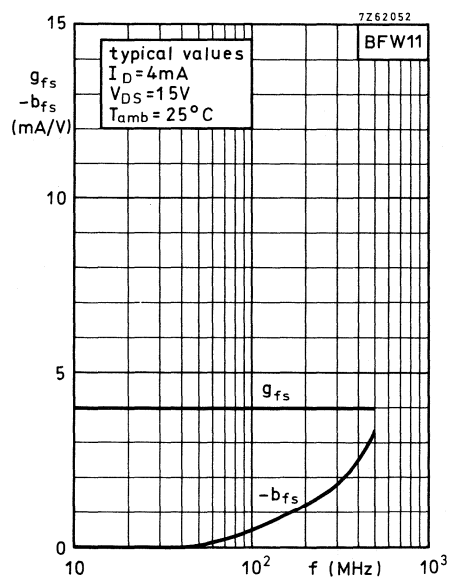

7Z62048
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
$-C_{rs}$ (pF)
b_{rs}
$-C_{rs}$
f (MHz)

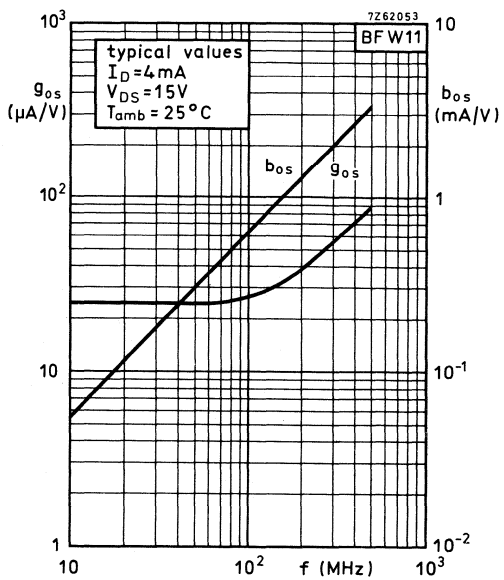

7Z62047
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)

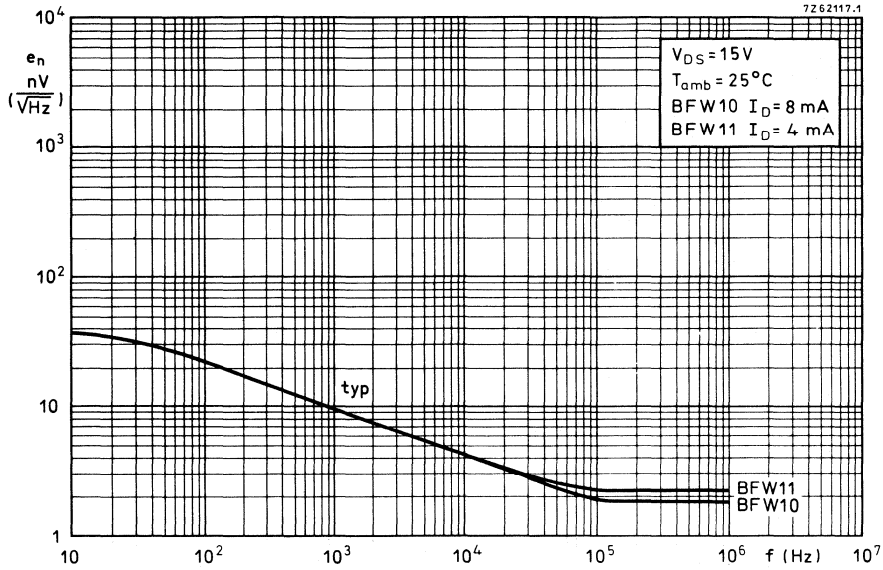

7Z62046
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)

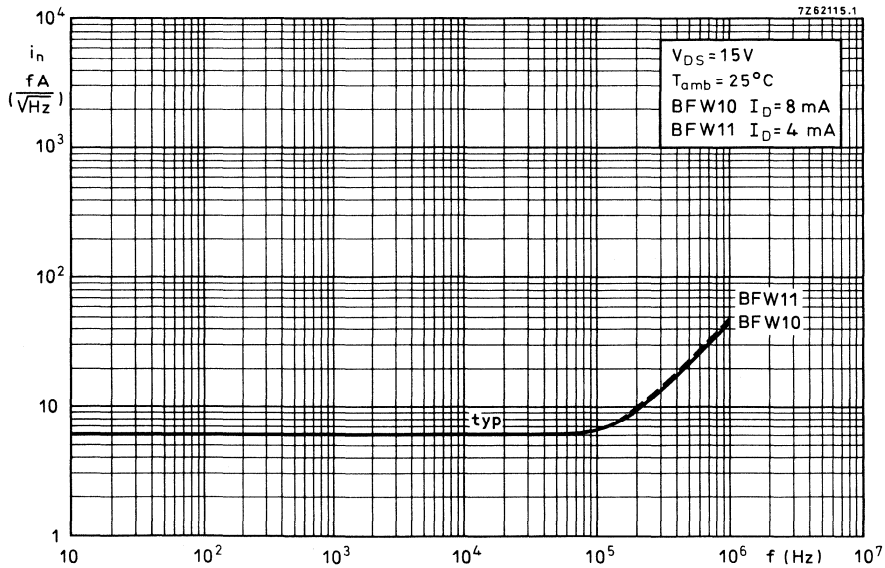

7Z62051
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

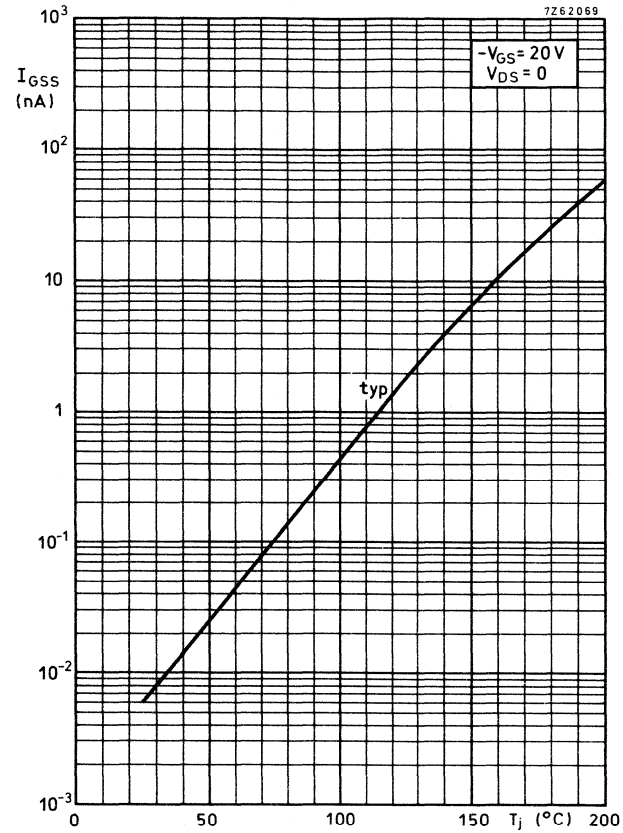

7Z62050
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
f (MHz)


7Z62052
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)


7Z62053
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)


7Z62117.1
10^4
e_n
$\frac{nV}{\sqrt{Hz}}$
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62115.1
10^4
i_n
$\frac{fA}{\sqrt{Hz}}$
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
BFW11
BFW10
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62069
$-V_{GS}$ = 20 V
V_{DS} = 0
typ
I_{GSS} (nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150		mW
			BFW12	**BFW13**	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0,2	mA
		<	5	1,5	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2,5	1,2	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	0,5	mS
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA					
B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

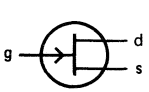
MECHANICAL DATA

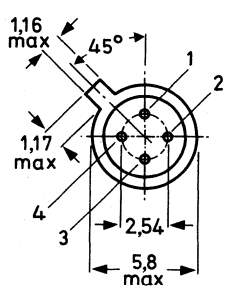
Dimensions in mm

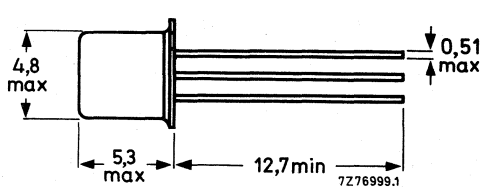
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 85 °C	P_{tot}	max.	150	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

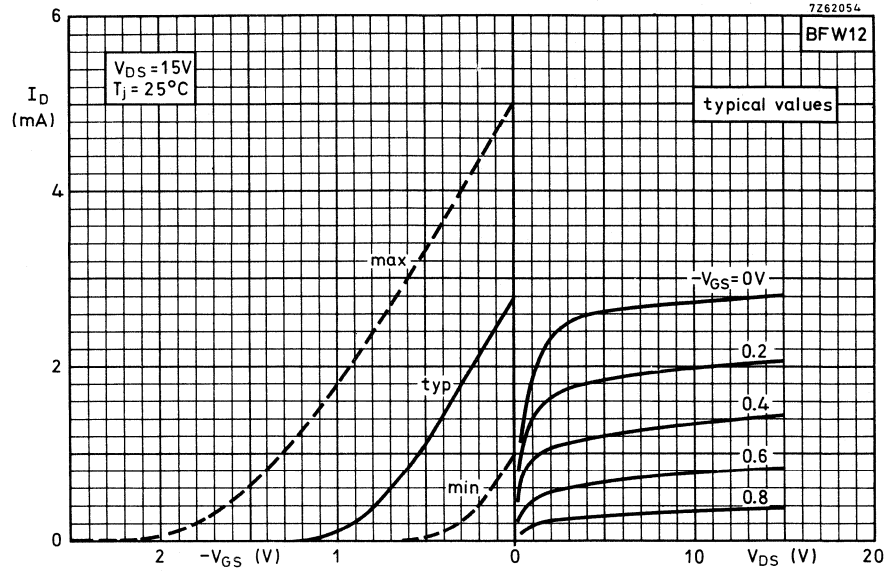
From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

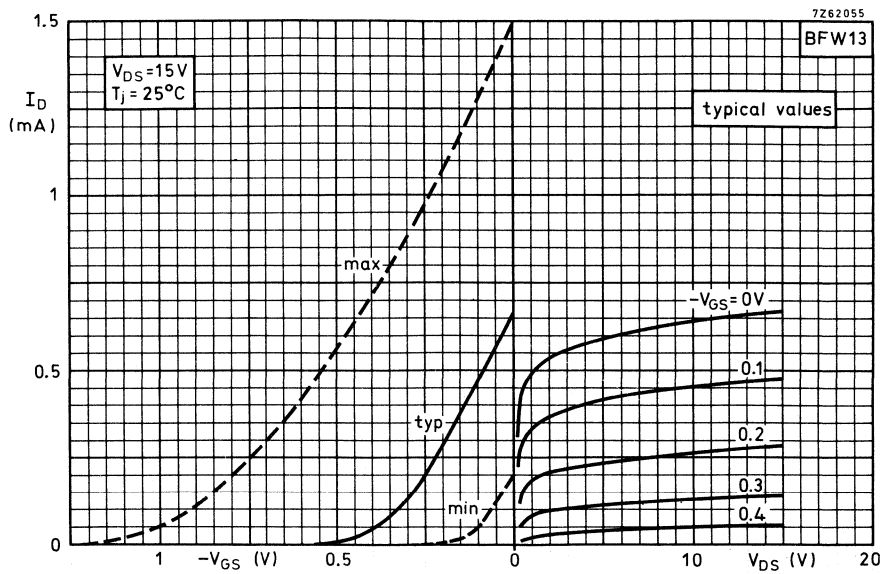
CHARACTERISTICS

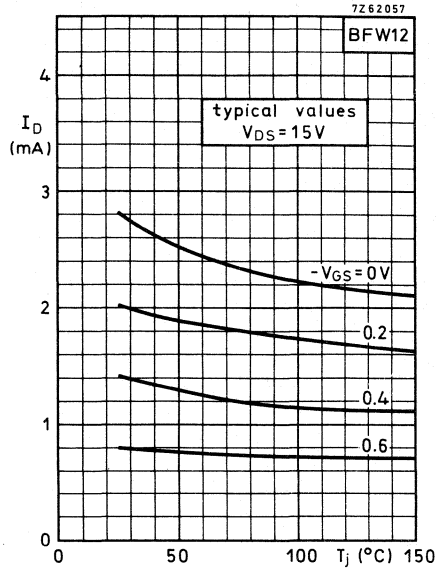
T_j = 25 °C unless otherwise specified

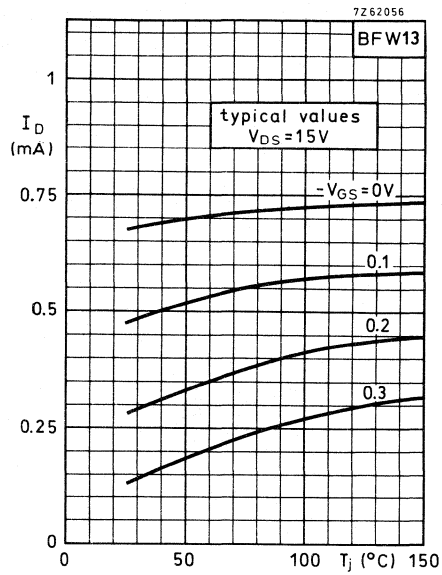
			BFW12	BFW13	
Gate cut-off currents					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.1	0.1	μA
Drain current [1])					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mS
Output admittance	$\|y_{os}\|$	<	30	10	μS
V_{DS} = 15 V; I_D = 500 μA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	–	mS
Output admittance	$\|y_{os}\|$	<	10	–	μS
V_{DS} = 15 V; I_D = 200 μA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mS
Output admittance	$\|y_{os}\|$	<	5	5	μS
f = 1 MHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA; T_{amb} = 25 °C B = 0.6 to 100 Hz	V_n	<	0.5	0.5	μV

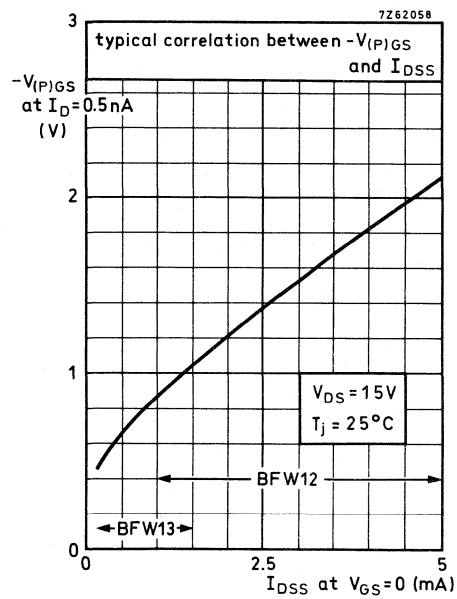
[1]) Measured under pulsed conditions.

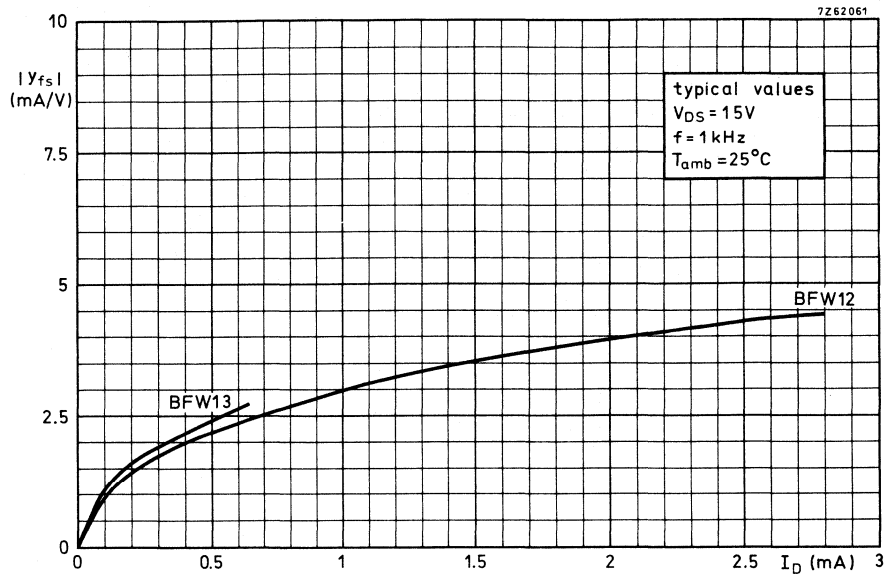

7Z62054
BFW12
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$= 0V
0.2
0.4
0.6
0.8
2
$-V_{GS}$ (V)
1
0
10
V_{DS} (V)
20

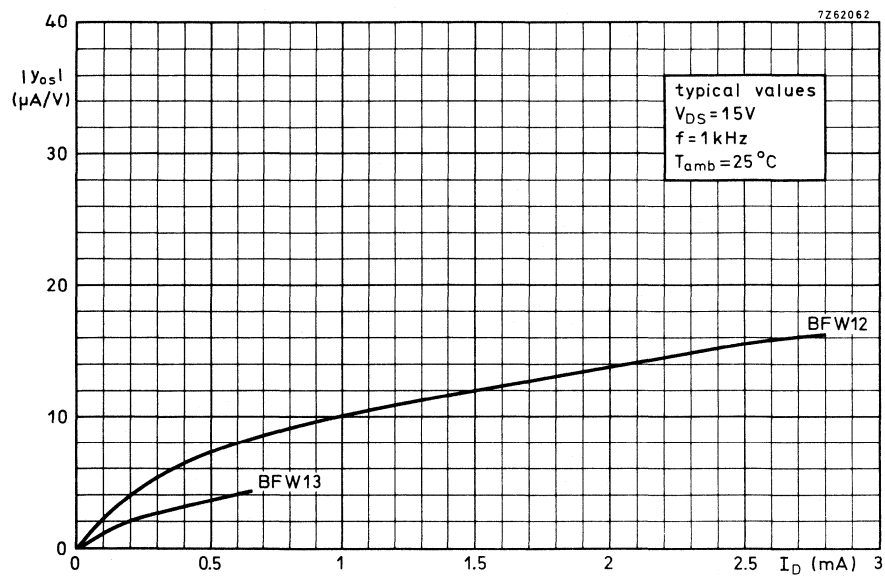

7Z62055
BFW13
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
1.5
1
0.5
0
max
typ
min
$-V_{GS}$= 0V
0.1
0.2
0.3
0.4
1
$-V_{GS}$ (V)
0.5
0
10
V_{DS} (V)
20

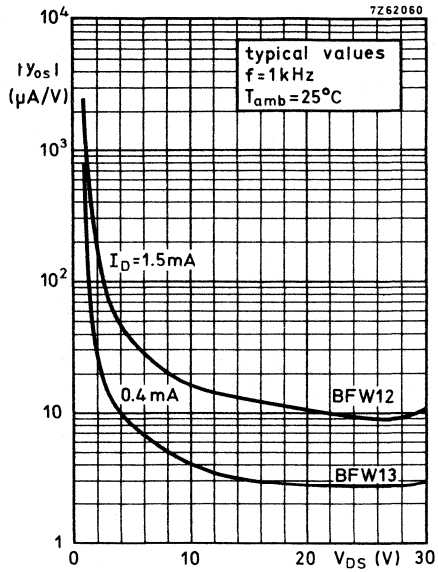

7Z62057
BFW12
typical values
V_{DS} = 15V
I_D (mA)
-V_{GS} = 0V
0.2
0.4
0.6
0
1
2
3
4
0
50
100
150
T_j (°C)

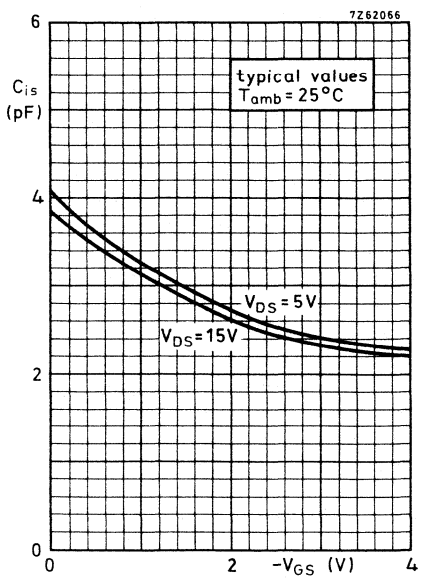

7Z62056
BFW13
typical values
V_{DS} = 15V
I_D (mA)
-V_{GS} = 0V
0.1
0.2
0.3
0
0.25
0.5
0.75
1
0
50
100
150
T_j (°C)

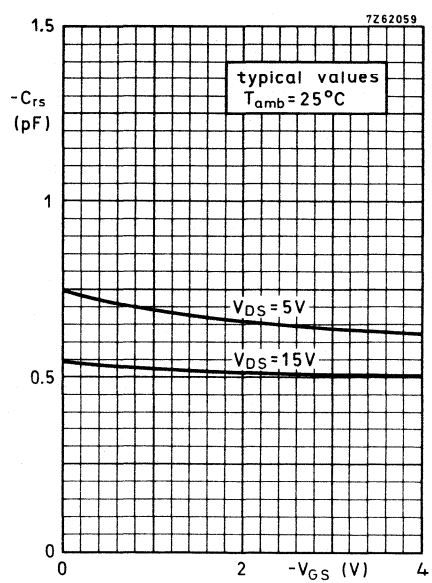

7Z62058
typical correlation between -$V_{(P)GS}$ and I_{DSS}
-$V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15V
T_j = 25°C
BFW12
BFW13
0
1
2
3
0
2.5
5
I_{DSS} at V_{GS} = 0 (mA)

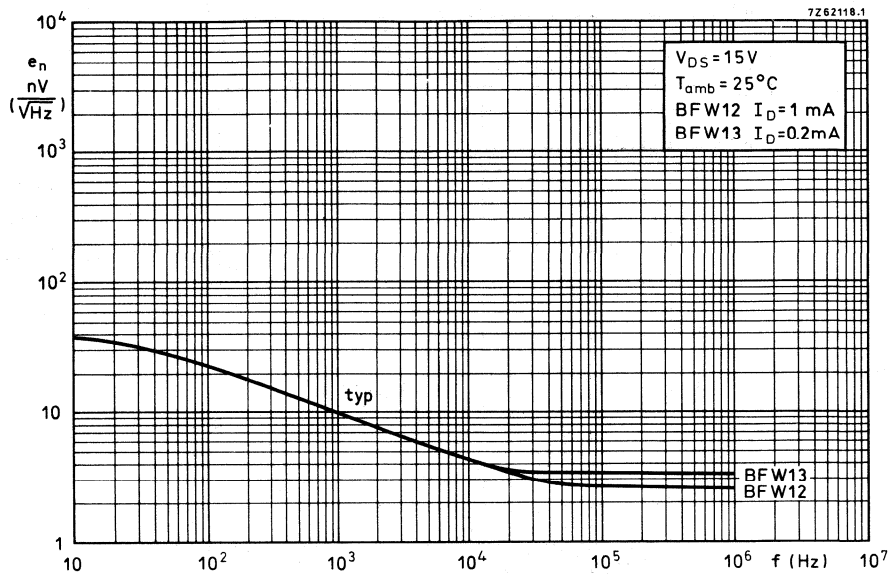

7Z62061
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

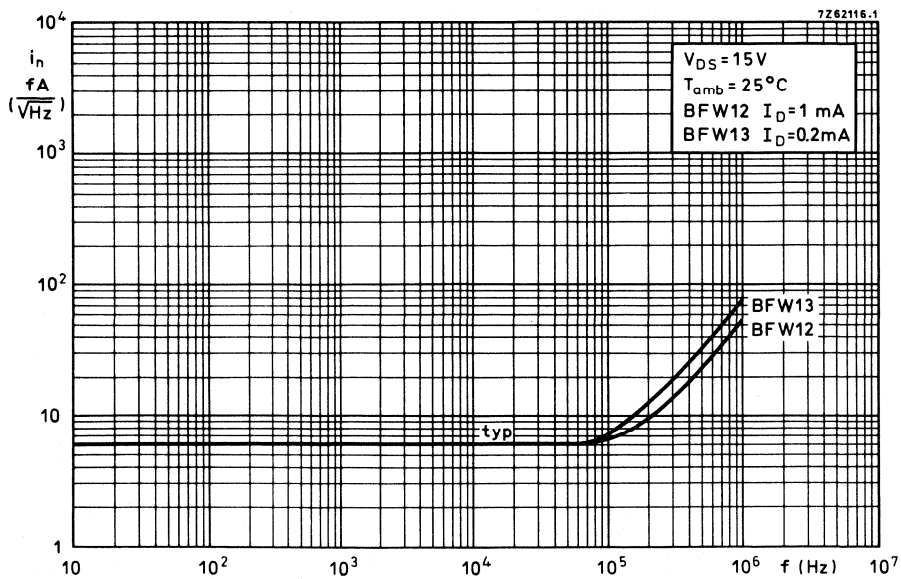

7Z62062
40
|yos|
(μA/V)
30
20
10
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

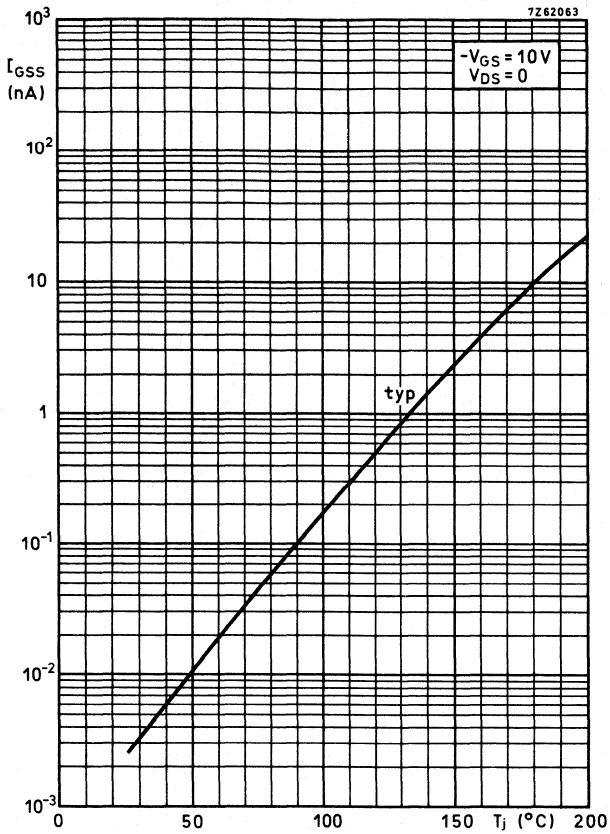

7Z62060
typical values
f = 1kHz
T_{amb} = 25°C
$|Y_{os}|$
(μA/V)
10^4
10^3
10^2
10
1
I_D = 1.5mA
0.4mA
BFW12
BFW13
0
10
20
V_{DS} (V)
30


7Z62066
typical values
T_{amb} = 25°C
C_{is}
(pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
2
$-V_{GS}$ (V)
4


7Z62059
typical values
T_{amb} = 25°C
$-C_{rs}$
(pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
2
$-V_{GS}$ (V)
4


7Z62118.1
10^4
e_n
nV
($\frac{}{\sqrt{Hz}}$)
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2 mA
typ
BFW13
BFW12
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62116.1
10^4
i_n
fA
($\frac{}{\sqrt{Hz}}$)
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2 mA
BFW13
BFW12
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62063
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10 V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

N-channel enhancement mode vertical D-MOS transistor

BS107

FEATURES

- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
V_{GSth}	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	150	mA
R_{DSon}	drain-source on-state resistance	28	Ω

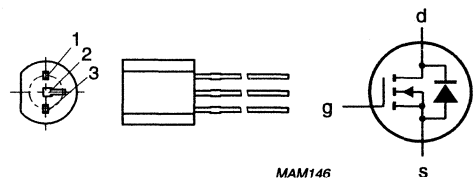


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BS107

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	150	mA
I_{DM}	drain current	peak	-	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

N-channel enhancement mode vertical D-MOS transistor

BS107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	4	20	ns

N-channel enhancement mode vertical D-MOS transistor

BS107

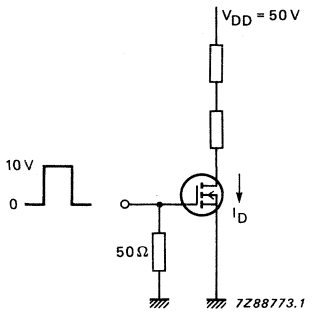


Fig.2 Switching time test circuit.

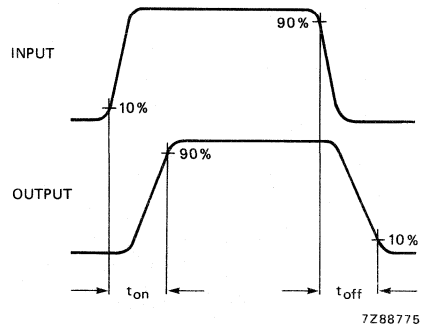


Fig.3 Input and output waveforms.

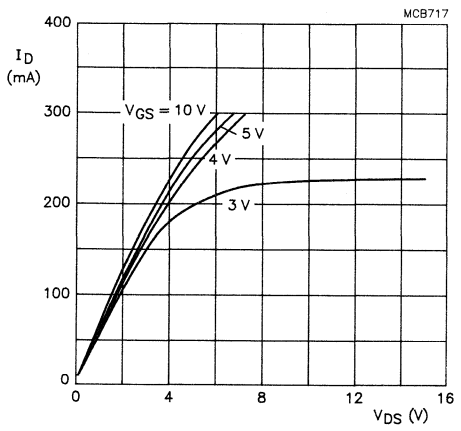


Fig.4 Typical output characteristics; T_j = 25 °C.

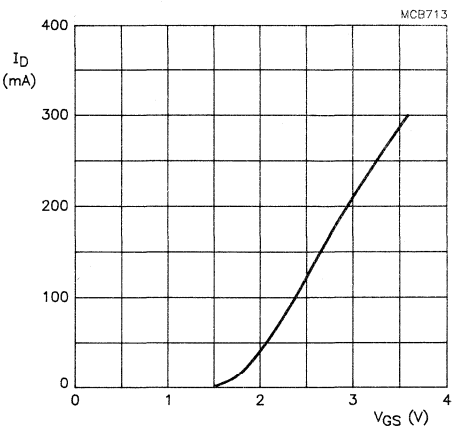


Fig.5 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

BS107

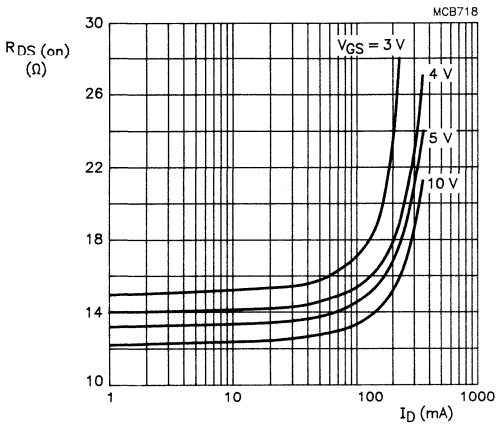


Fig.6 Typical on-resistance as a function of drain current; T_j = 25 °C.

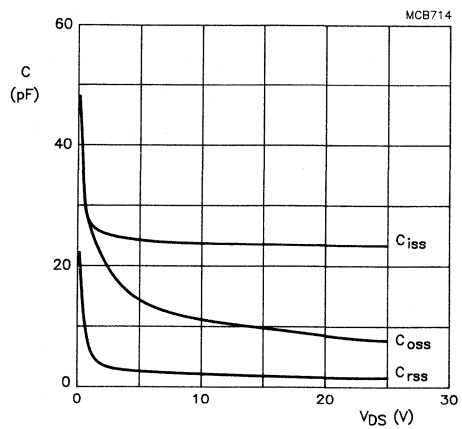


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

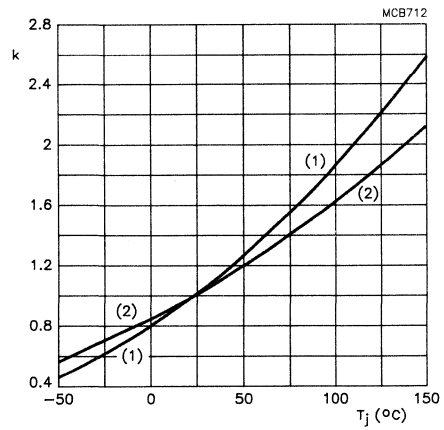


Fig.8 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}; \text{ typical } R_{DS(on)}$$

at 150 mA/10 V;
(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V;

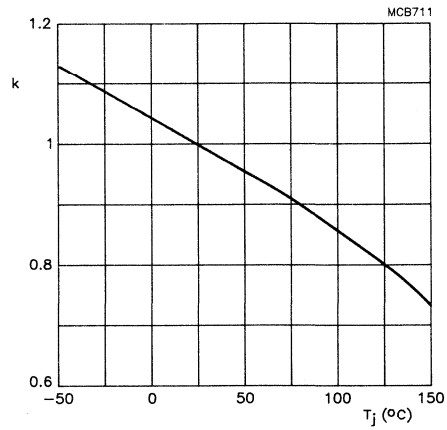


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}; \text{ typical } V_{GS(th)}$$

at 1 mA.

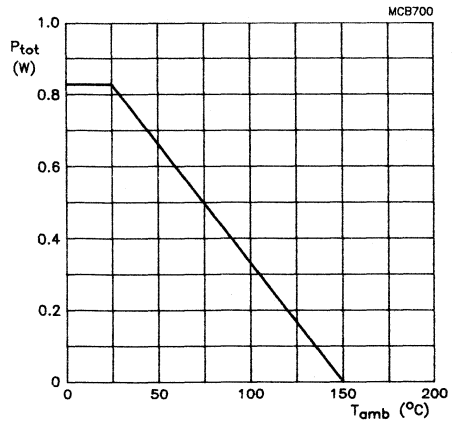


Fig.10 Power derating curve.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6	W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 6.4	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	200 350	mS mS

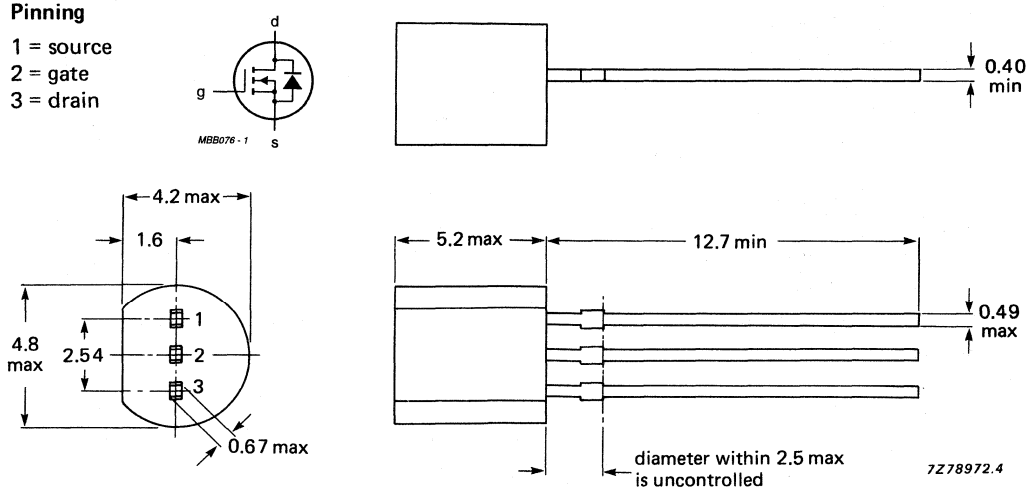
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinnings are available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Storage temperature	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 130 V; V_{GS} = 0	I_{DSS}	max.	30 nA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.0 V 3.0 V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.4 Ω
I_D = 100 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.2 Ω 6.0 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

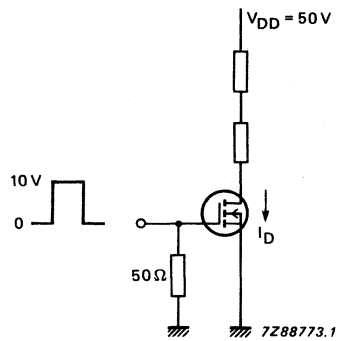


Fig.2 Switching times test circuit.

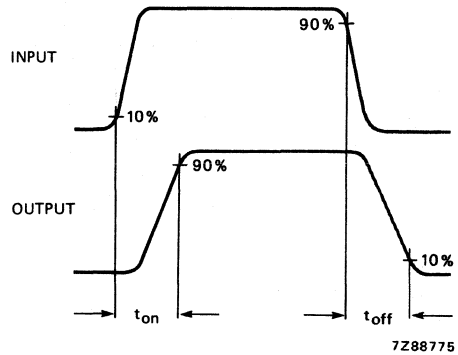


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BS108

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

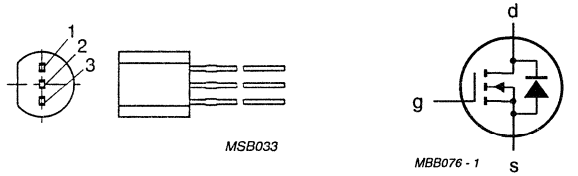


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 x 10 mm

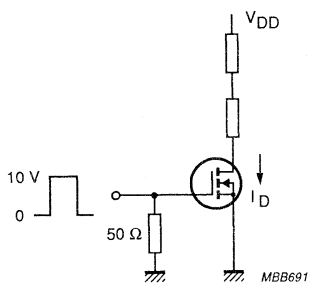
N-channel enhancement mode vertical D-MOS transistor

BS108

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V

Fig.2 Switching times test circuit.

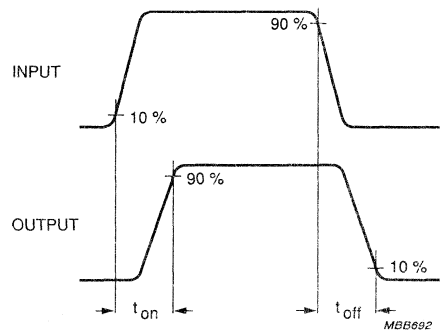


Fig.3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Junction temperature	T_j	max.	150 °C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5 Ω

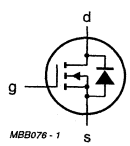
MECHANICAL DATA

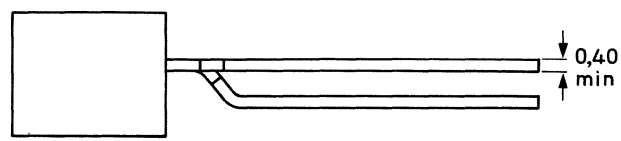
Dimensions in mm

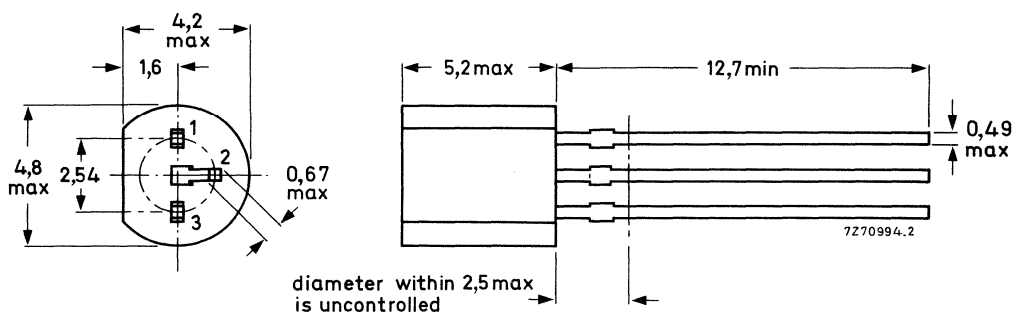
Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain







Note: Various pin configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Drain-gate voltage	V_{DG}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (DC) at T_c = 25 °C	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage V_{GS} = 0; I_D = 100 μA	$V_{(BR)DS}$	min. typ.	60 V 90 V
Gate threshold voltage V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min. max.	0.8 V 3.0 V
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10 nA
Drain cut-off current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5 μA
Drain-source ON-resistance (note 1) V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	typ. max.	2.5 Ω 5.0 Ω
Forward transconductance (note 1) V_{DS} = 10 V; I_D = 200 mA; f = 1 kHz	g_{fs}	typ.	200 mS
Capacitances at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	25 pF 40 pF
	C_{os}	typ. max.	22 pF 30 pF
	C_{rs}	typ. max.	6 pF 10 pF
Switching times at I_D = 200 mA I_D = 200 mA; V_{DS} = 50 V;	t_{on}	typ. max.	4 ns 10 ns
V_{GS} = 0 to 10 V	t_{off}	typ. max.	4 ns 10 ns

Note

1. t_p = 80 μs; δ = 0,01.

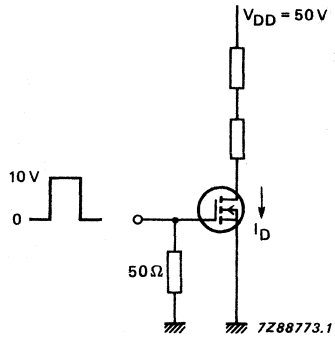


Fig. 2 Switching times test circuit.

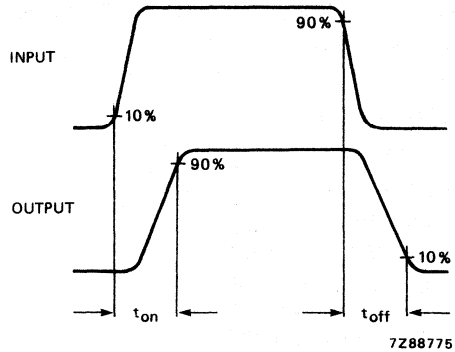


Fig. 3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BS208

FEATURES

- Direct interface to C-MOS
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope. Intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92

PIN	DESCRIPTION
1	source
2	gate
3	drain

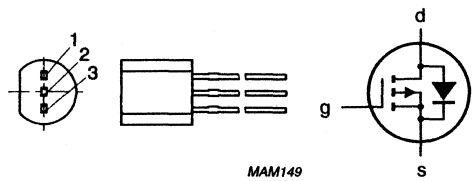


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	–200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
$\lvert y_{fs} \rvert$	forward transfer admittance	ID = –200 mA; V_{DS} = –25 V	100	200	–	mS
I_D	drain current (DC)		–	–	–0.2	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	14	Ω
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	–	0.83	W

P-channel enhancement mode vertical D-MOS transistor

BS208

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
$-I_D$	drain current	DC	-	0.2	A
$-I_{DM}$	drain current	peak value	-	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	0.83	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
R_{thj-a}	from junction to ambient	150	K/W

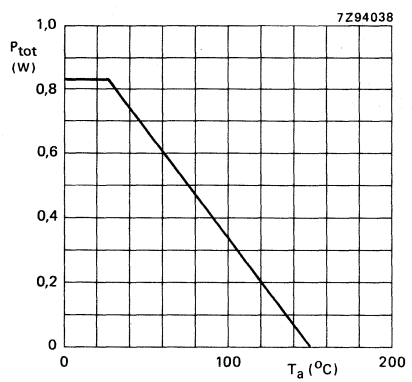


Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

BS208

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	200	-	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 130 V V_{GS} = 0	-	-	1	μA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 70 V $-V_{GS}$ = 0.2 V	-	-	25	μA
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	V_{GS} = V_{DS} $-I_D$ = 1 mA	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	-	14	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	-	mS
C_{iss}	input capacitances	note 1	-	55	90	pF
C_{oss}	output capacitance	note 1	-	20	30	pF
C_{rss}	feedback capacitance	note 1	-	5	15	pF
t_{on}	turn-on time	note 2	-	5	10	ns
t_{off}	turn-off time	note 2	-	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

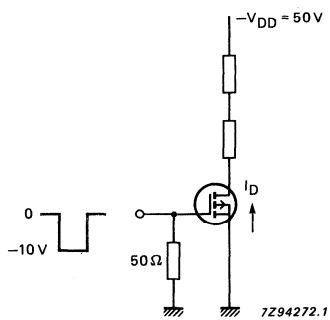


Fig.3 Switching times test circuit.

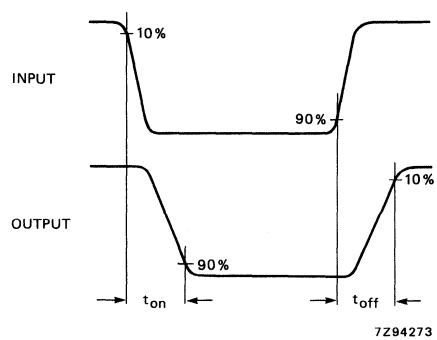


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BS208

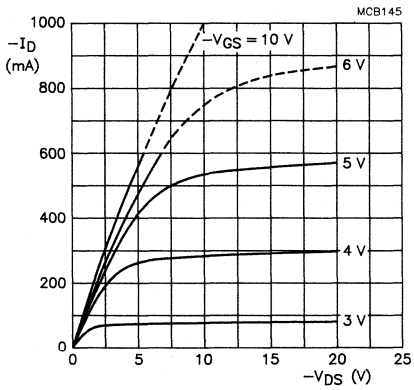


Fig.5 Typical output characteristics; T_j = 25 °C.

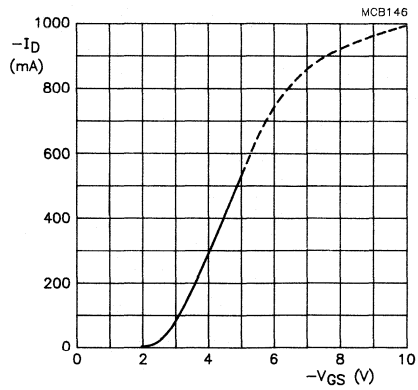


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

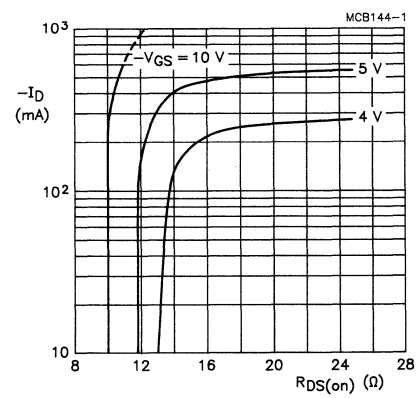


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

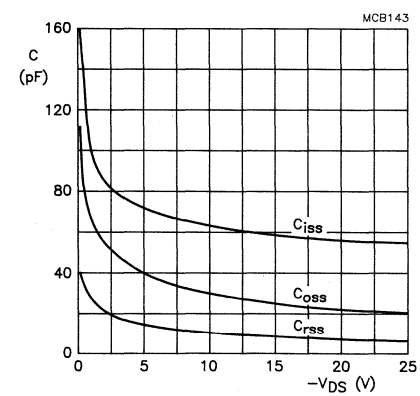


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BS208

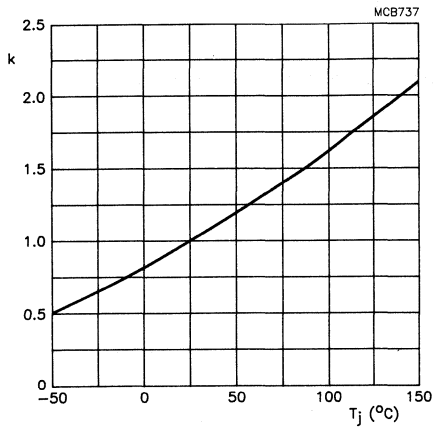


Fig.9 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C}$; typical $R_{DS\,(on)}$ at 200 mA/10 V;

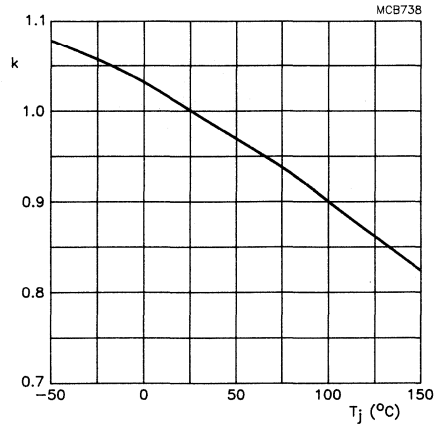


Fig.10 Temperature coefficient of gate-source threshold voltage;

$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C}$; typical $V_{GS\,(th)}$ at 1 mA.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|y_{fs}\|$	typ.	125 mS

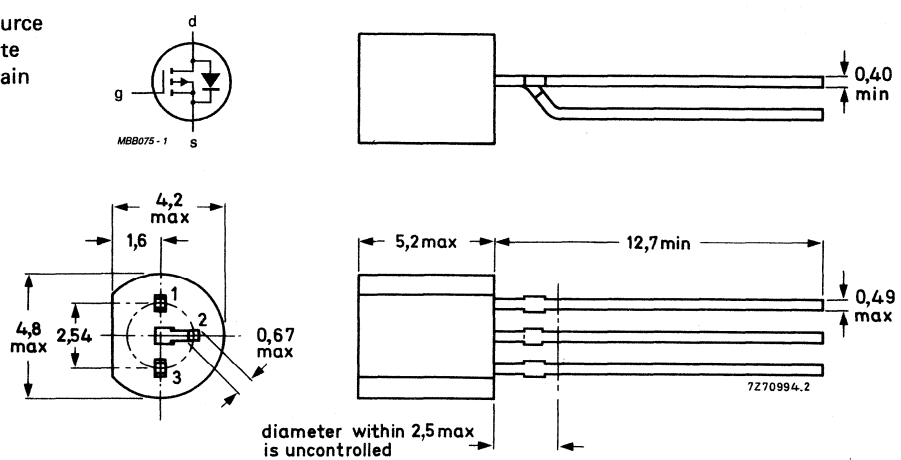
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak value)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	45 V
Drain-source leakage current $-V_{DS}$ = 25 V; V_{GS} = 0	$-I_{DSS}$	max.	0.5 μA
Gate-source leakage current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.0 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

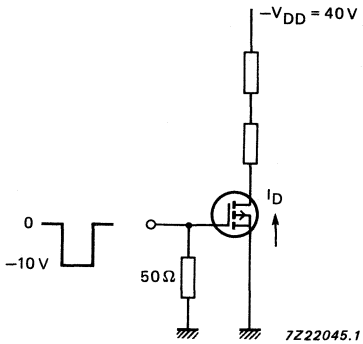


Fig. 2 Switching times test circuit.

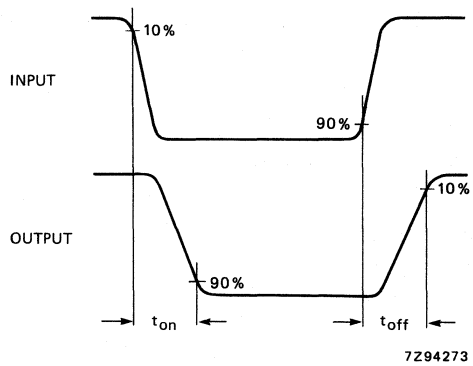


Fig. 3 Input and output waveforms.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feedback capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

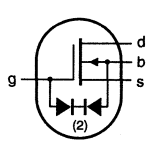
MECHANICAL DATA

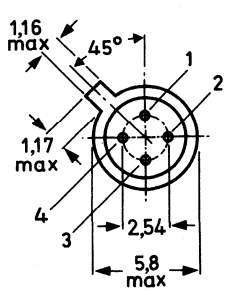
Dimensions in mm

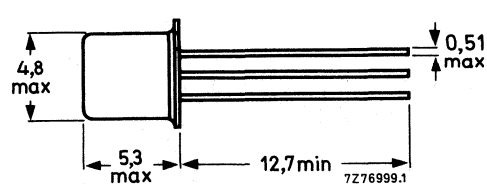
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = substrate (b) connected to case







Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	+ 15 −15	V V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C in free air	P_{tot}	max.	275	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	max.	10	nA
Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_S = 20 mA	g_{fs}	min. typ.	10 15	mS mS

Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I_D = 10 μA	$-V_{(P)GS}$	max.	2.0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0 V_{GS} = 5 V	r_{DSon}	typ. max.	25 Ω 50 Ω
V_{GS} = 10 V	r_{DSon}	typ. max.	15 Ω 30 Ω
Capacitances at f = 1 MHz (see Fig. 2) V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0.6 pF
Input capacitance	C_{iss}	typ.	2.3 pF
Output capacitance	C_{oss}	typ.	1.9 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 to + 5 V	t_{on}	typ.	1.0 ns
	t_{off}	typ.	5.0 ns

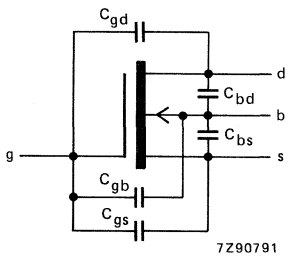
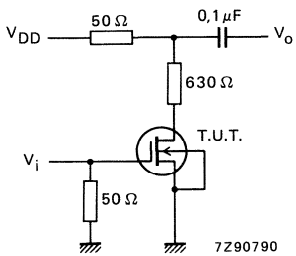


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$



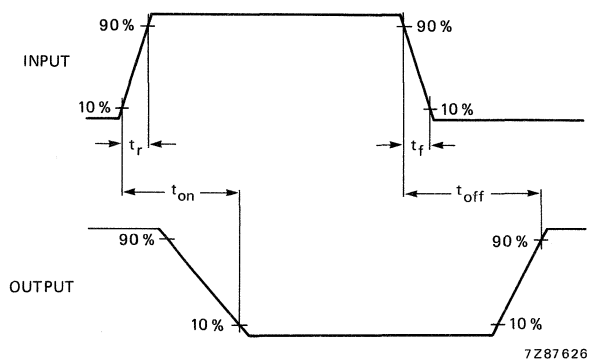


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; $t_r < 0.5$ ns; $t_f < 1.0$ ns; t_p = 20 ns; $\delta < 0.01$.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feed-back capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

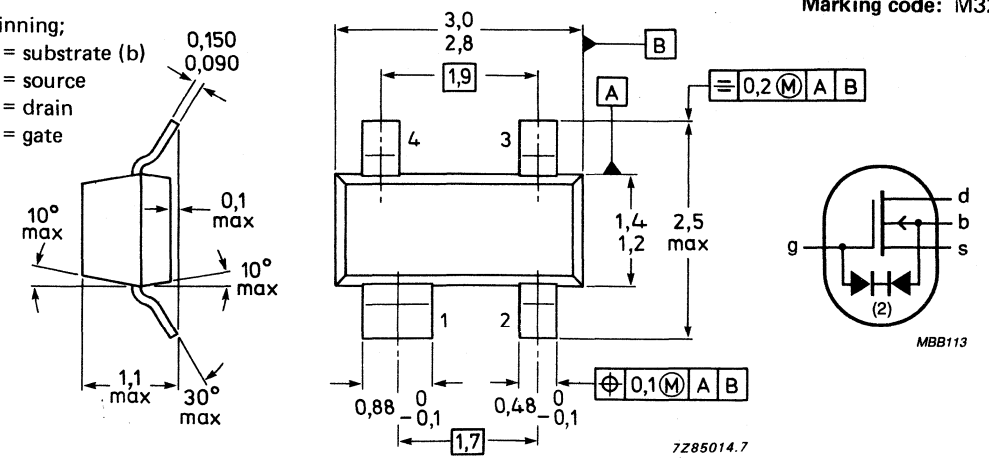
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Marking code: M32

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate



TOP VIEW

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	± 25	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current $V_{GD} = V_{BD}$ = 5 V; V_{SD} = 10V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	max.	10	nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	min. typ.	10 mS 15 mS
Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I I_D = 10 μA	$-V_{(P)GS}$	max.	2.0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 5 V	R_{DSon}	typ. max.	25 Ω 50 Ω
V_{GS} = 10 V	R_{DSon}	typ. max.	15 Ω 30 Ω
Capacitances at f = 1 MHz V_{GS} = V_{BS} = −5V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0.6 pF
Input capacitance	C_{iss}	typ.	1.5 pF
Output capacitance	C_{oss}	typ.	1.0 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on} t_{off}	typ. typ.	1.0 ns 5.0 ns

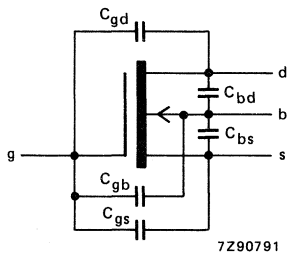
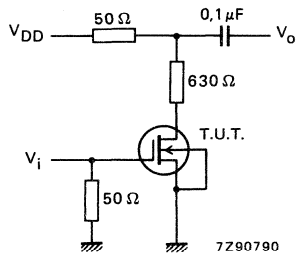


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$



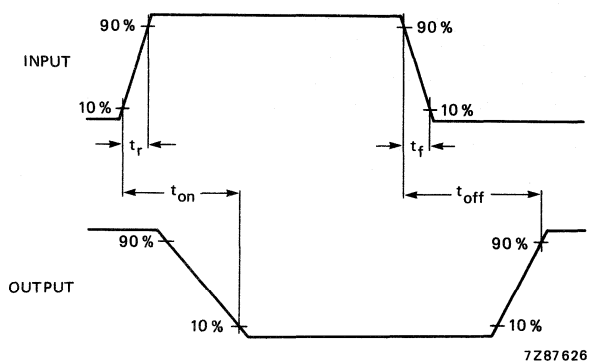


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; $t_r < 0.5$ ns; $t_f < 1.0$ ns; t_p = 20 ns; $\delta < 0.01$.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:
- analogue and/or digital switch
- switch driver
- converters
- choppers

QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275			mW
Drain-source resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 15 V	$R_{DS(on)}$	typ.		25			Ω
Feedback capacitance $V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.		0,6			pF
Junction temperature	T_j	max.		125			°C

MECHANICAL DATA

See next page.

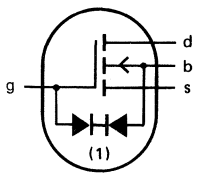
MECHANICAL DATA

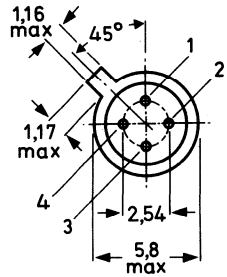
Dimensions in mm

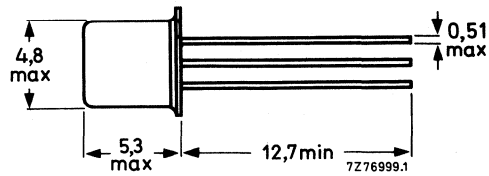
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = substrate (b)
connected to case







(1) Diode protection on types BSD213 and BSD215 only.
BSD212 and BSD214 have no protection diode.
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Gate-drain voltage	V_{GD}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275			mW
Storage temperature range	T_{stg}			−65 to + 175			°C
Junction temperature	T_j	max.		125			°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage							
$V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	>	10	10	20	20	V
Source-drain breakdown voltage							
$V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10	10	20	20	V
Drain-substrate breakdown voltage							
V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15	15	25	25	V
Source-substrate breakdown voltage							
V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	>	15	15	25	25	V
Drain-source leakage current							
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1,0	1,0	–	–	nA
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 20 V	I_{DSoff}	typ.	–	–	1,0	1,0	nA
Source-drain leakage current							
$V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1,0	1,0	–	–	nA
$V_{GD} = V_{BD} = -5$ V; V_{SD} = 20 V	I_{SDoff}	typ.	–	–	1,0	1,0	nA
Gate-substrate leakage current							
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 40 V	I_{GBS}	<	0,1	–	0,1	–	nA
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	<	–	10	–	10	nA
Threshold voltage							
$V_{DS} = V_{GS} = V_{GS(th)}$; V_{SB} = 0; I_S = 1 μA	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance							
I_D = 1,0 mA; V_{SB} = 0;							
V_{GS} = 5 V	$R_{DS(on)}$	typ.	50	50	50	50	Ω
		<	70	70	70	70	Ω
V_{GS} = 10 V	$R_{DS(on)}$	typ.	30	30	30	30	Ω
		<	45	45	45	45	
V_{GS} = 15 V	$R_{DS(on)}$	typ.	25	25	25	25	Ω
V_{GS} = 25 V	$R_{DS(on)}$	typ.	15		15		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at f = 1 kHz				
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	typ.	15	mS
		>	10	
Capacitance at f = 1 MHz (see Fig. 2)				
$V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

DYNAMIC CHARACTERISTICS (continued)

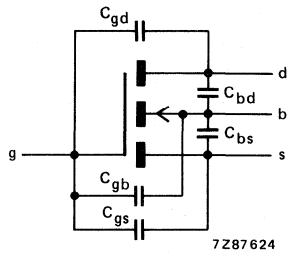


Fig. 2 Capacitances model.

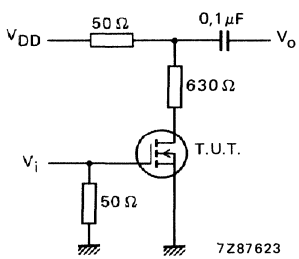
$C_{iss} = C_{GS} + C_{GD} + C_{GB}$

$C_{oss} = C_{GD} + C_{BD}$

$C_{rss} = C_{GD}$

Switching times (see Fig. 3)

V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on}	typ.	1,0	ns
	t_{off}	typ.	5,0	ns



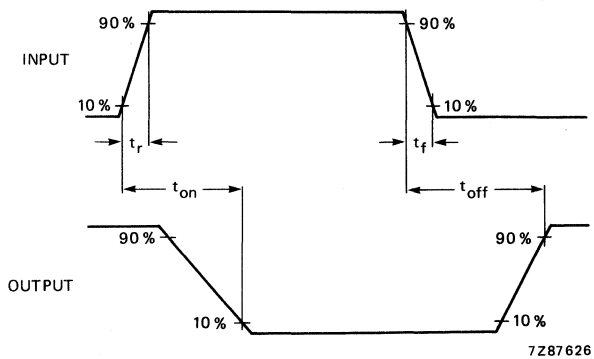


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

R_i = 50 Ω

t_r < 0,5 ns

t_f < 1,0 ns

t_p = 20 ns

δ < 0,01

N-channel depletion mode vertical D-MOS transistors

BSD254; BSD254A; BSD254AR

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	200	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	0.85	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	–1.65	–0.75	V

PINNING - TO-92 variant

PIN	DESCRIPTION
BSD254	
1	gate
2	drain
3	source
BSD254A	
1	source
2	gate
3	drain
BSD254AR	
1	drain
2	gate
3	source

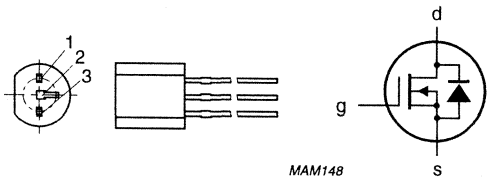
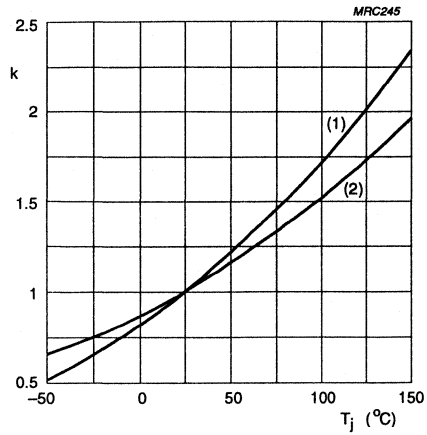


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	200	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	0.85	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C



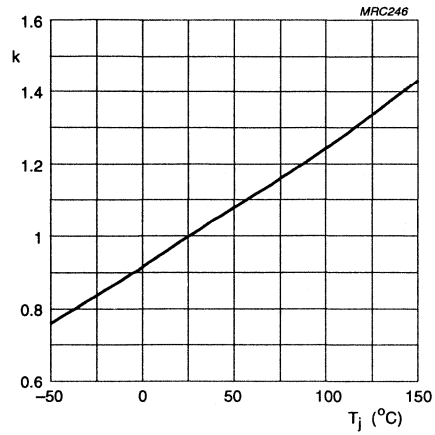
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$:

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig.13 Temperature coefficient of gate-source threshold voltage.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	145 K/W

Note

1. Device mounted on an epoxy printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = –3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = –3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	–1.65	–0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	–1.4	–0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain saturation current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = –3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to –3 V	–	30	ns

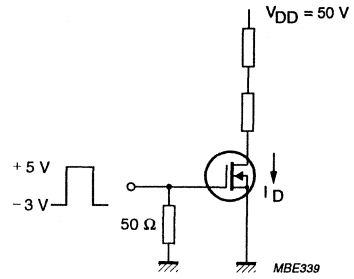


Fig.2 Switching times test circuit.

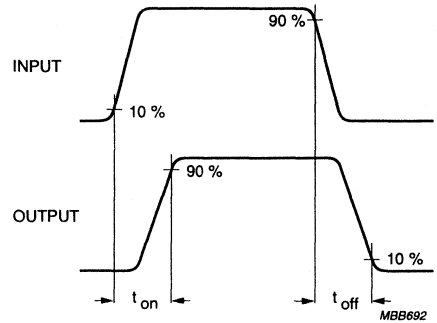


Fig.3 Input and output waveforms.

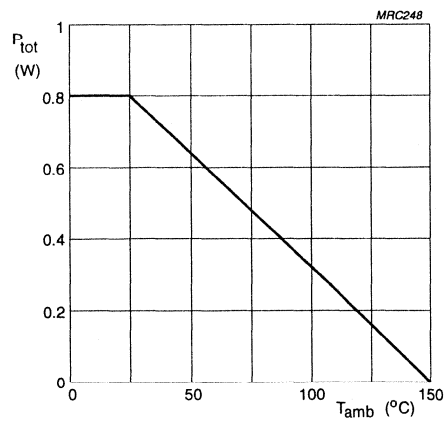
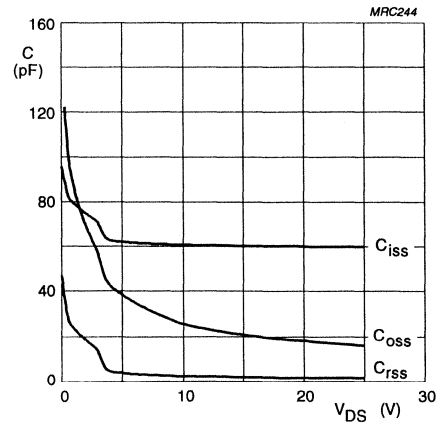
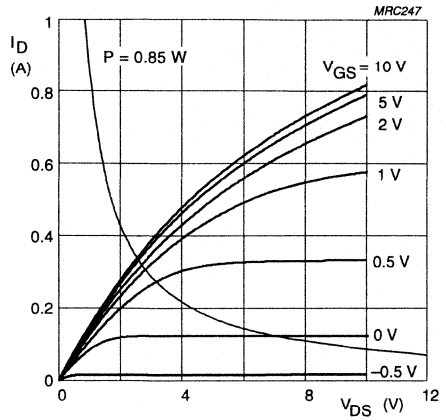


Fig.4 Power derating curve.



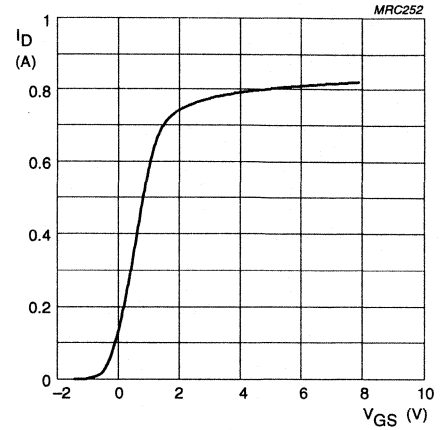
V_{GS} = –3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



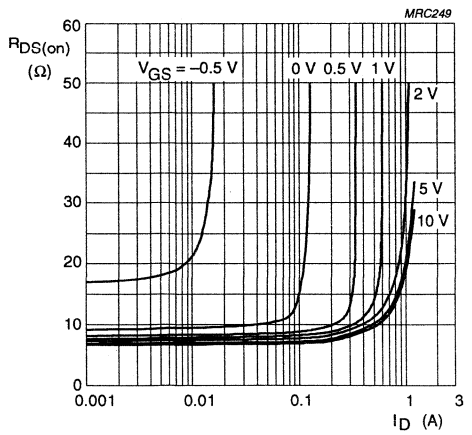
T_j = 25 °C.

Fig.6 Typical output characteristics.



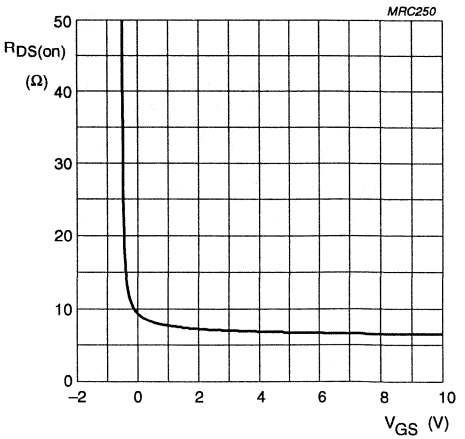
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

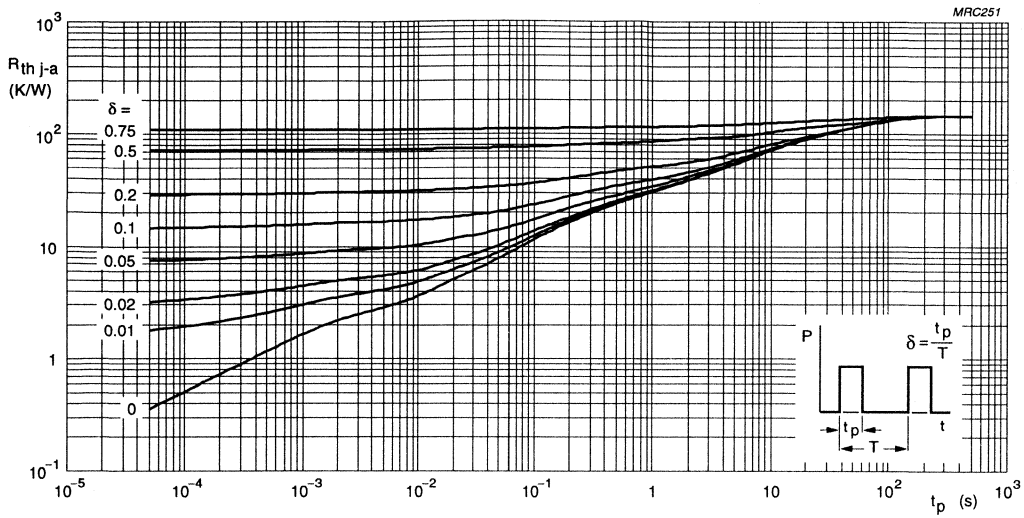
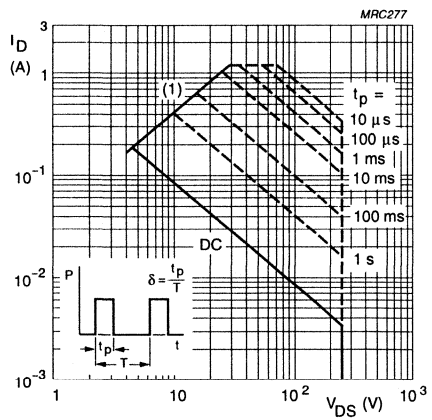


Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.

N-channel enhancement mode vertical D-MOS transistors

BSN10; BSN10A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use in general purpose fast switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	175	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

PINNING

PIN	DESCRIPTION
BSN10	
1	gate
2	drain
3	source
BSN10A	
1	source
2	gate
3	drain

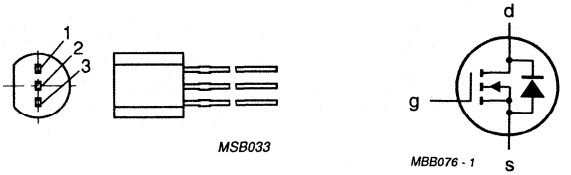


Fig.1 Simplified outline (TO-92) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	175	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	8	15	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	12	20	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	18	30	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	40	80	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	7	15	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns

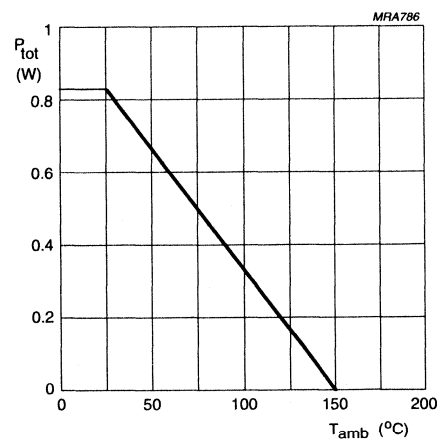
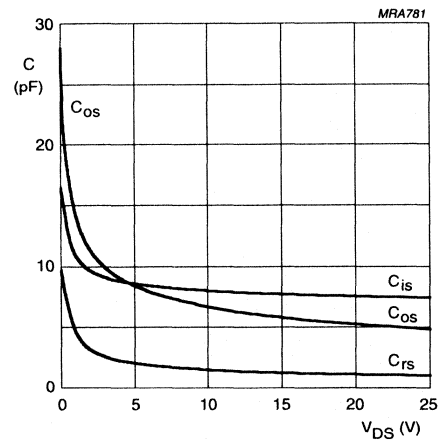
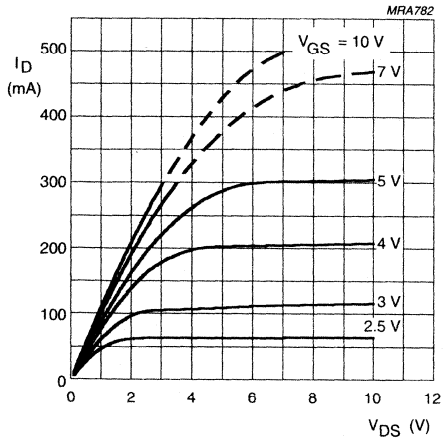


Fig.2 Power derating curve.



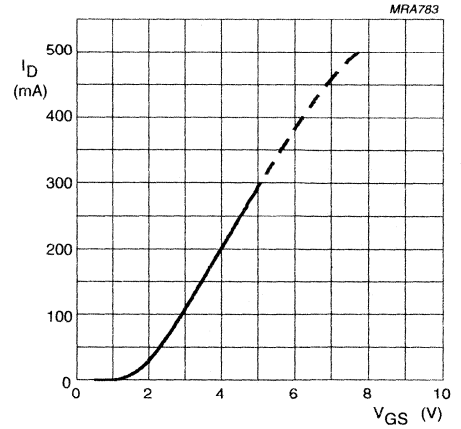
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.3 Capacitance as a function of drain-source voltage, typical values.



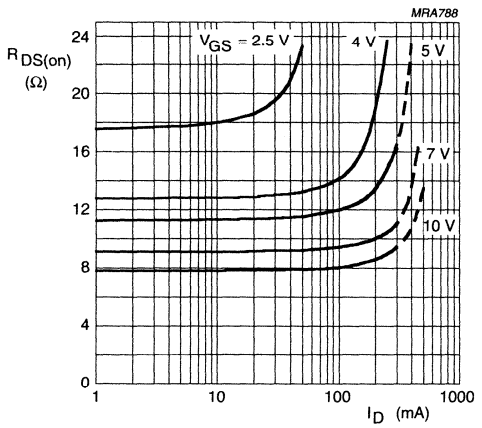
T_j = 25 °C.

Fig.4 Typical output characteristics.



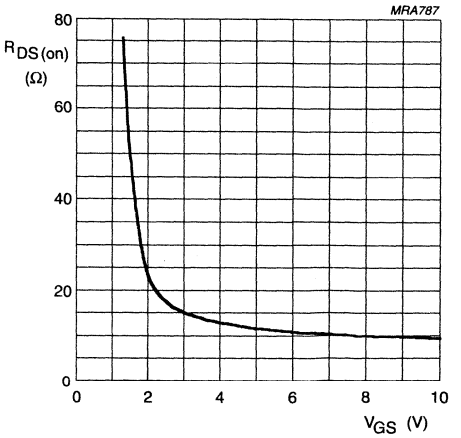
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



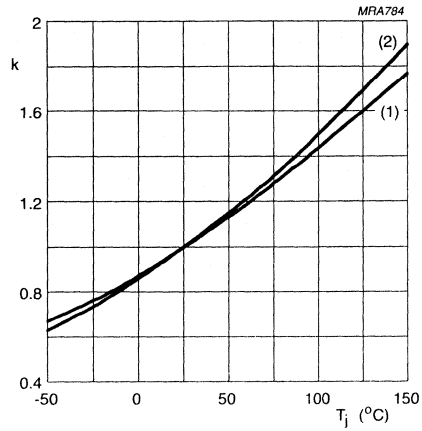
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



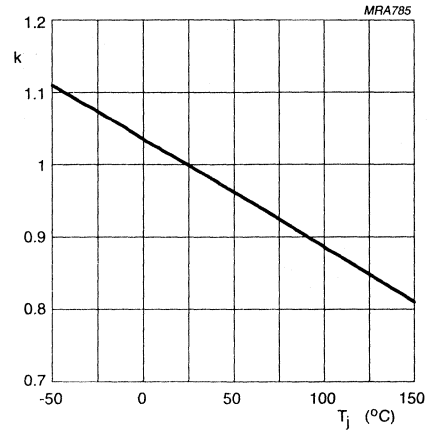
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$ at 100 mA/10 V.

(1) I_D = 10 mA; V_{GS} = 2.5 V.

(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSN20

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	100	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a surface-mounted device in thin and thick film circuits and in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
1	gate
2	source
3	drain

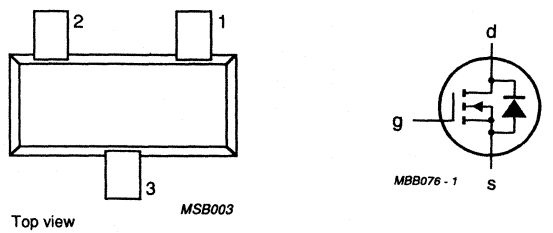


Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	300	mW
		up to T_{amb} = 25 °C (note 2)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430 K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500 K/W

Notes

1. Transistor mounted on a ceramic substrate, 10 x 8 x 0.7 mm.
2. Transistor mounted on a printed circuit board.

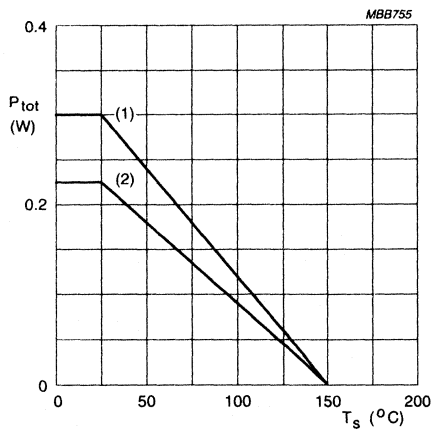
N-channel enhancement mode vertical D-MOS transistor

BSN20

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

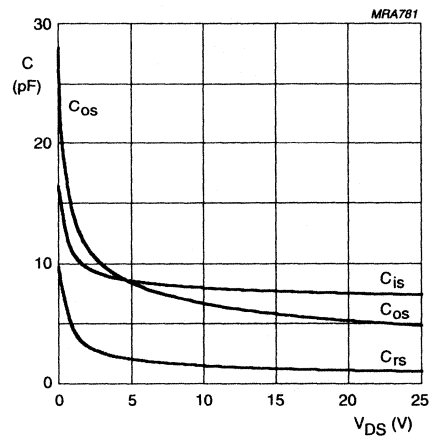
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	8	15	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	14	20	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	18	30	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	40	80	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	7	15	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	5	10	ns



(1) Mounted on a ceramic substrate.

(2) Mounted on a printed circuit board.

Fig.2 Power derating curve.

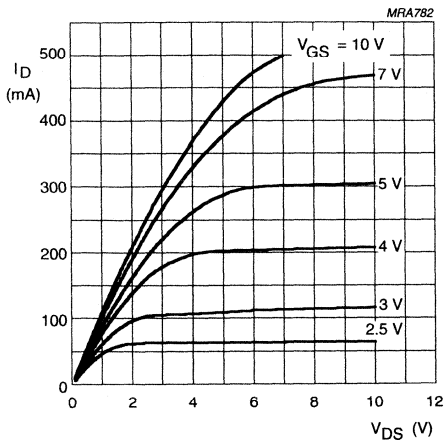


V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.3 Capacitance as a function of drain-source voltage, typical values.

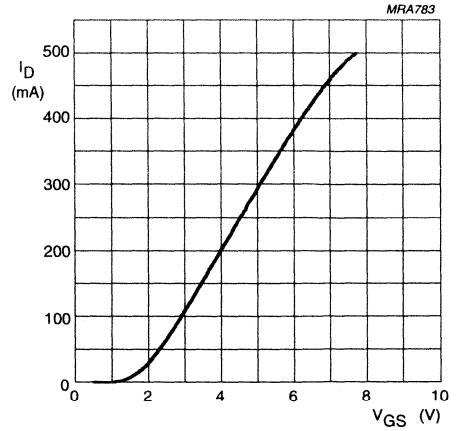
N-channel enhancement mode vertical D-MOS transistor

BSN20



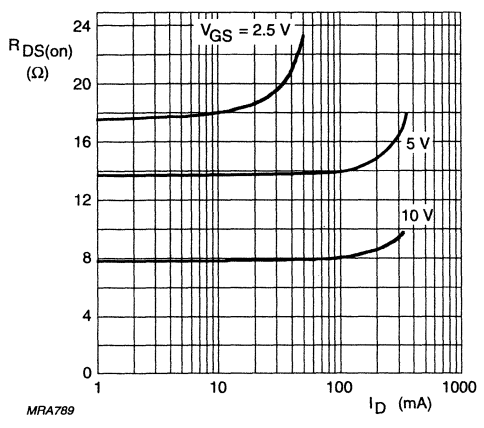
T_j = 25 °C.

Fig.4 Typical output characteristics.



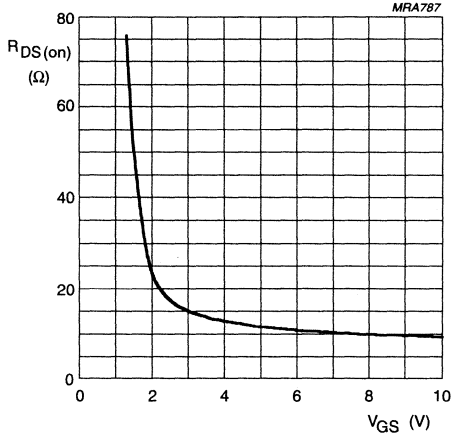
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



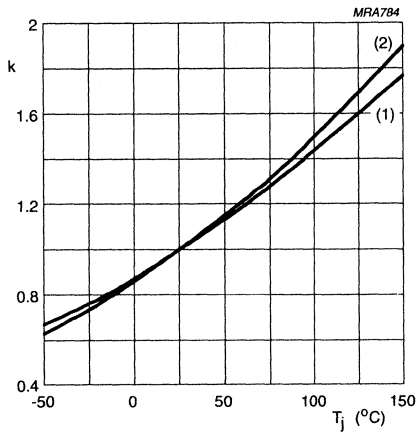
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



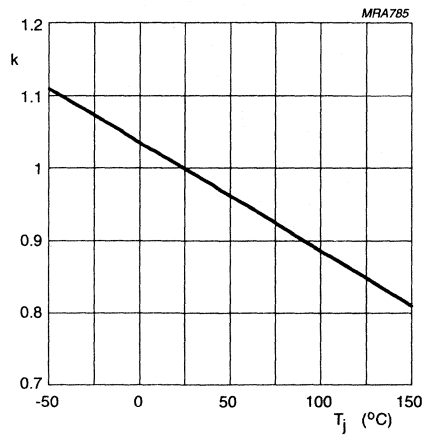
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$ at 100 mA/10 V.

(1) I_D = 10 mA; V_{GS} = 2.5 V.

(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage.

Data sheet	
status	Product specification
date of issue	April 1995

BSN204/BSN204A

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 (BSN204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 (BSN204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.8 V	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	1.8	V

PIN CONFIGURATION

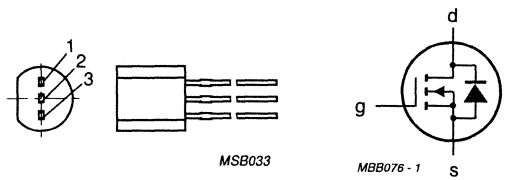


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	250	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.4	1	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

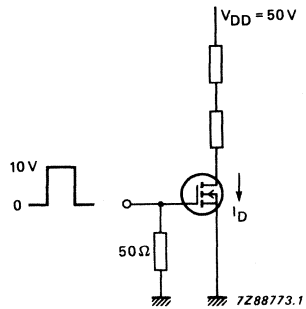


Fig.2 Switching time test circuit.

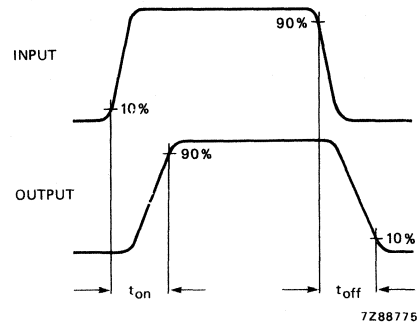


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5	Ω
		max.	6	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	200	mS
		typ.	350	mS

MECHANICAL DATA

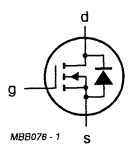
Dimensions in mm

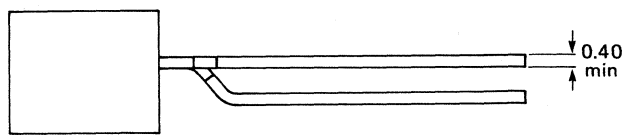
Fig.1 TO-92 variant.

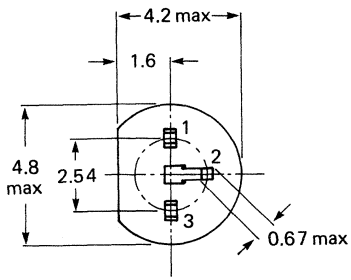
Pinning

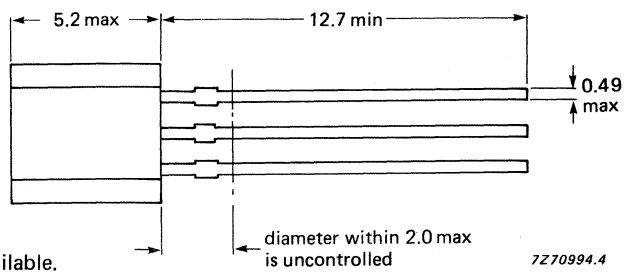
BSN205
1 = gate
2 = drain
3 = source

BSN205A
1 = source
2 = gate
3 = drain









Note: various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	15 ns 20 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

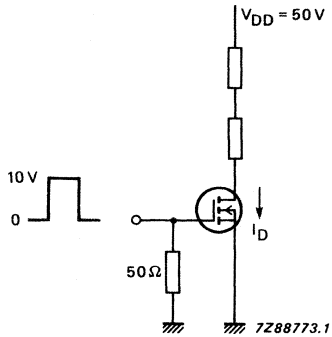


Fig.2 Switching time test circuit.

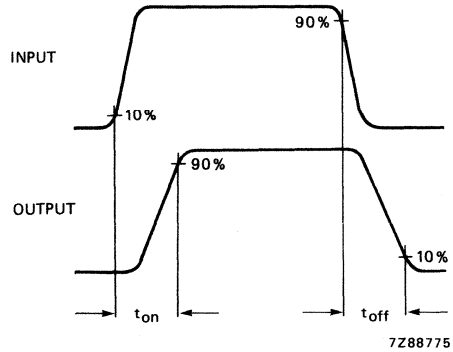


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

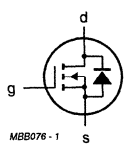
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92 variant.

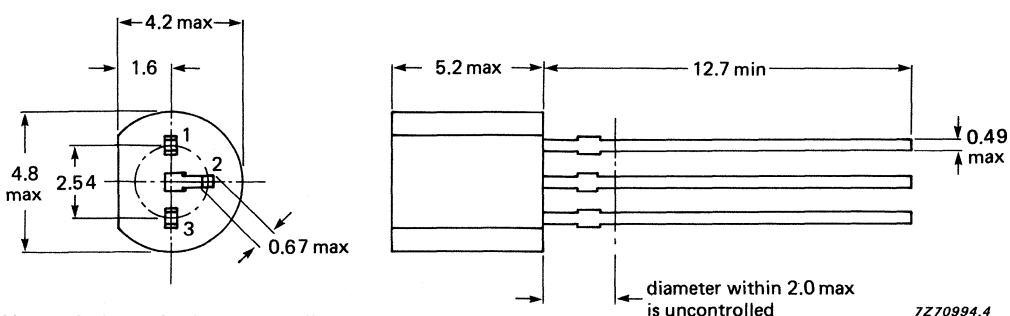
Pinning (BSN254)

1 = gate
2 = drain
3 = source



Pinning (BSN254A)

1 = source
2 = gate
3 = drain



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250 V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.0 V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
I_D = 20mA; V_{GS} = 2.4V	$R_{DS(on)}$	max.	10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 400 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 15 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	20 ns 30 ns

Note

1. Device mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

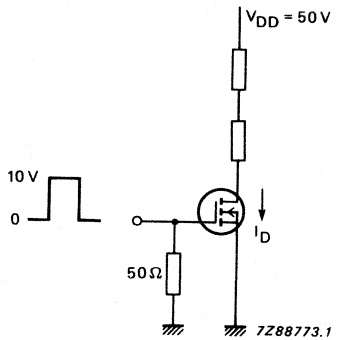


Fig.2 Switching times test circuit.

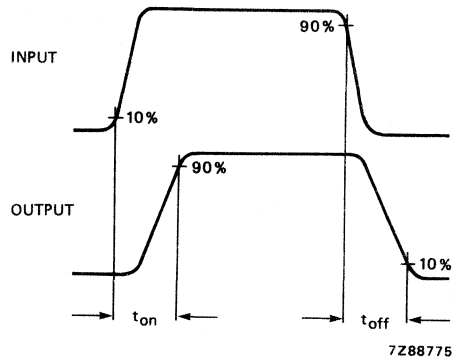


Fig.3 Input and output waveforms.

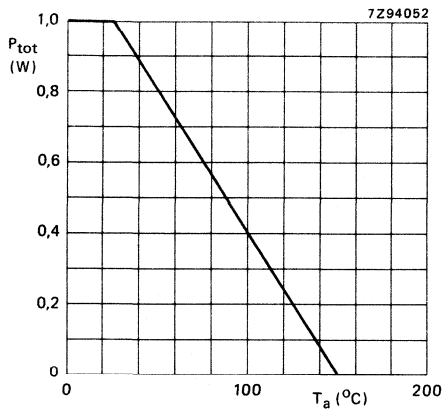


Fig.4 Power derating curve.

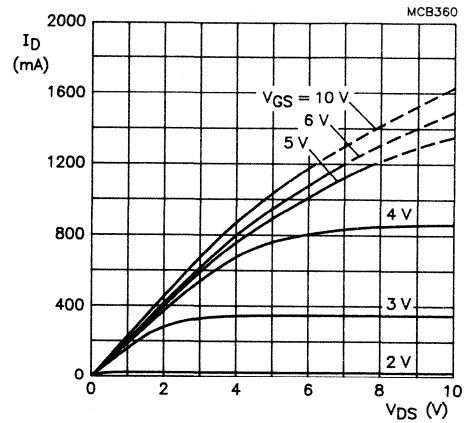


Fig.5 Output characteristics; T_j = 25 °C; typical values.

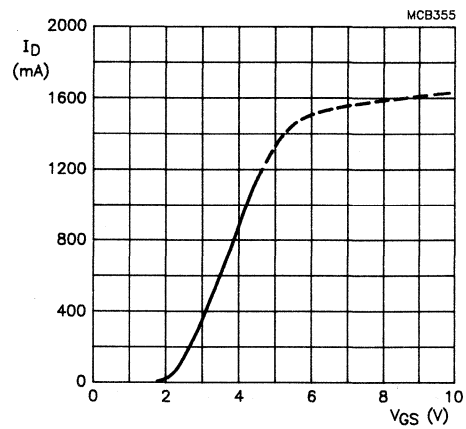


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

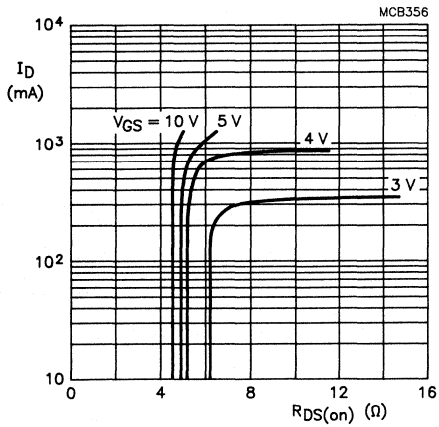


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

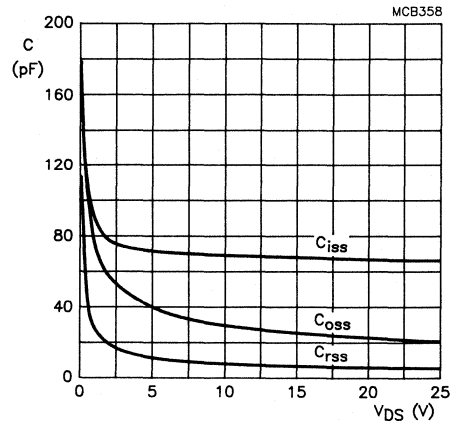


Fig.8 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

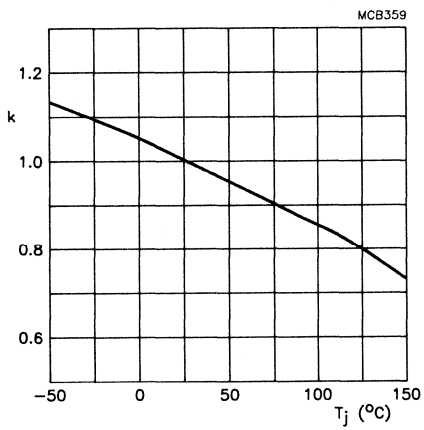


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$;

$V_{GS(th)}$ at 1 mA; typical values.

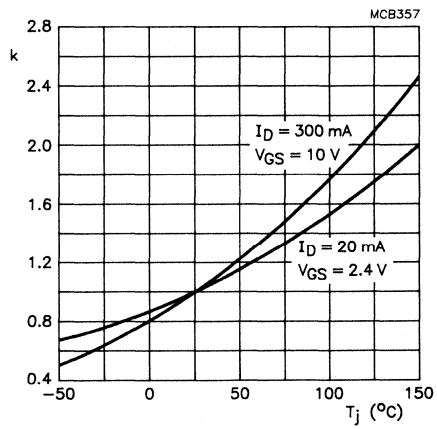


Fig.10 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^oC}$;

typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

BSN274/BSN274A

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

MECHANICAL DATA

Dimensions in mm

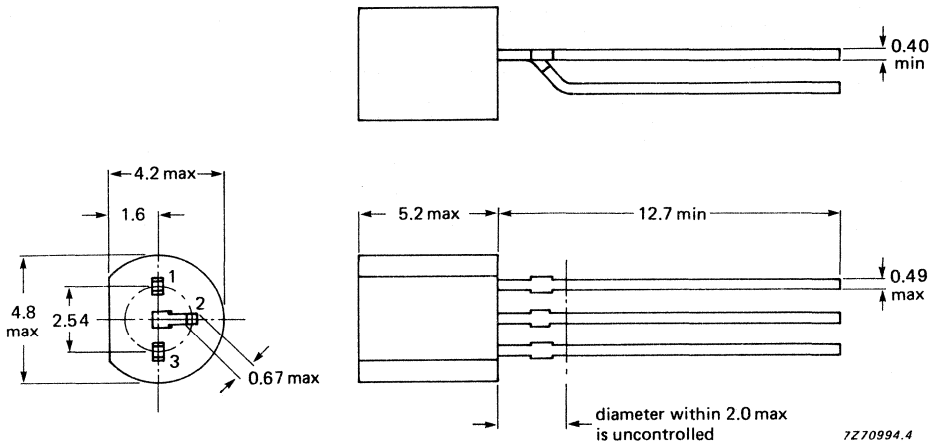


Fig.1 TO-92 variant.

PIN CONFIGURATION

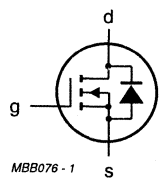


Fig.2 Pin configuration.

PINNING (BSN274)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING (BSN274A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	250	mA
I_{DM}	drain current	peak	-	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain leads minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	270	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V V_{GS} = 0	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA V_{GS} = 10 V	-	6.5	8	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.4 V	-	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 25 V	200	400	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	65	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	5	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

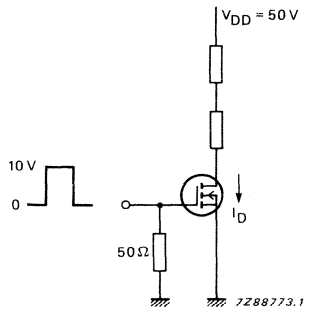


Fig.2 Switching time test circuit.

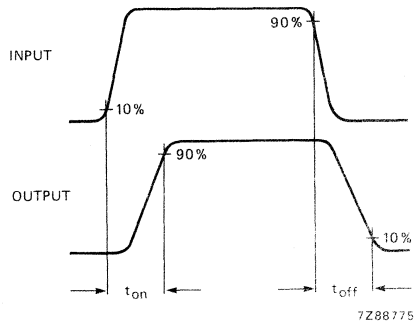


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN304; BSN304A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
BSN304	
1	gate
2	drain
3	source
BSN304A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{GS} = V_{DS}$	0.8	2	V

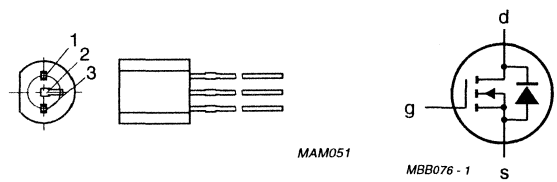


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	125 K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

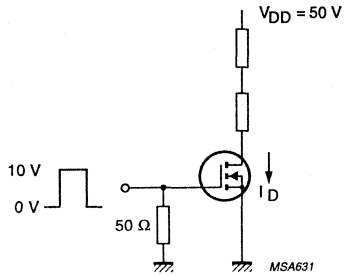


Fig.2 Switching times test circuit.

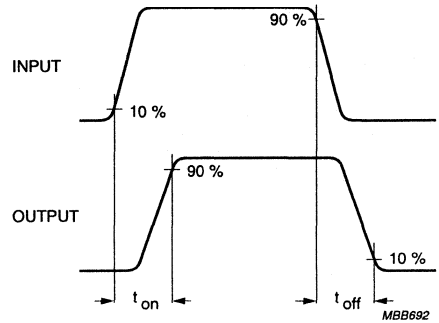


Fig.3 Input and output waveforms.

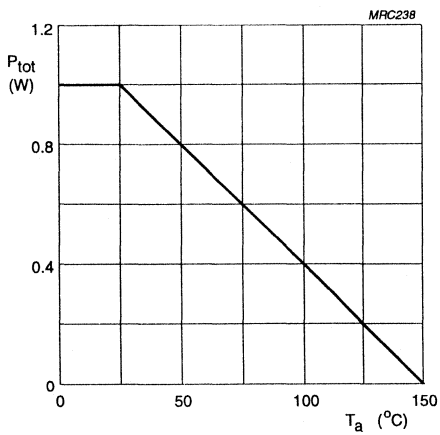
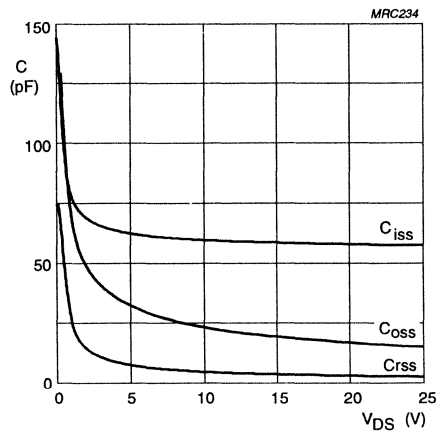
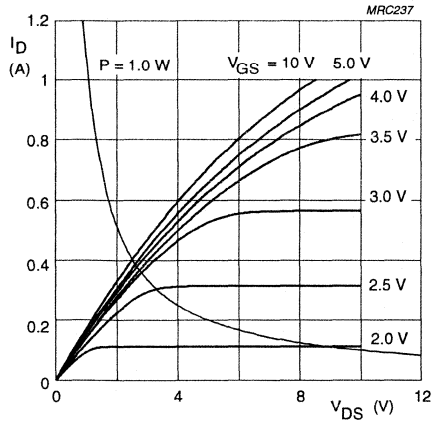


Fig.4 Power derating curve.



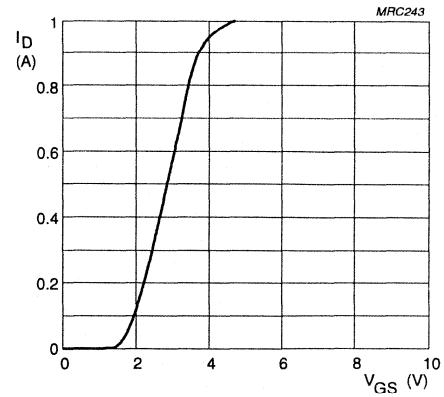
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



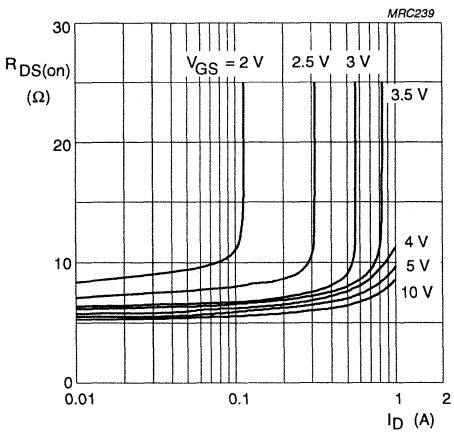
T_j = 25 °C.

Fig.6 Typical output characteristics.



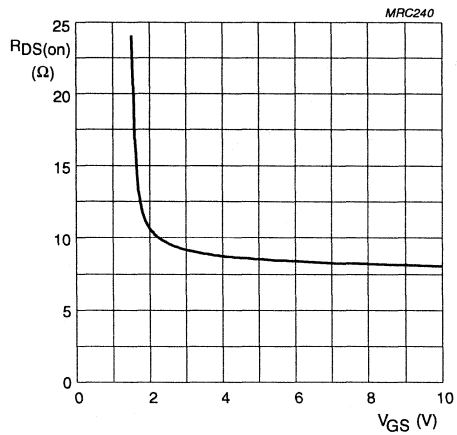
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

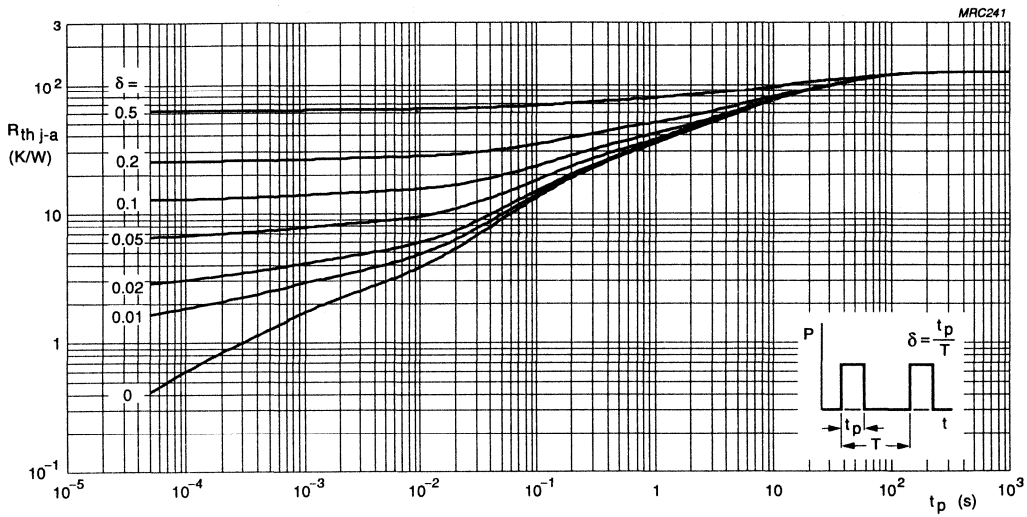
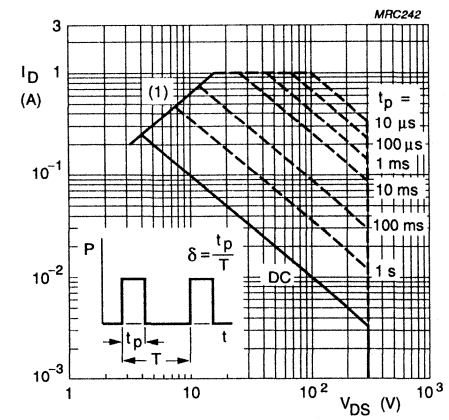


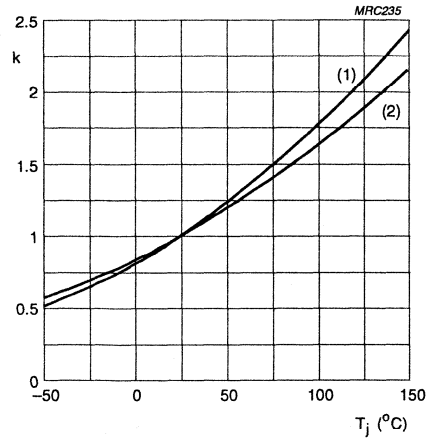
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



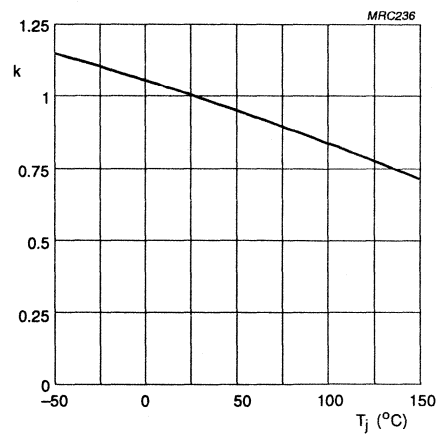
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 10 V.

(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptors in telephone sets and for application in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

PINNING

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

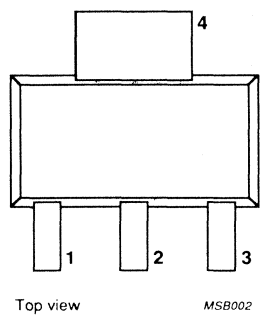


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

N-channel enhancement mode vertical D-MOS transistor

BSP89

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	240	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 340 mA; V_{GS} = 10 V	–	4	6	Ω
		I_D = 340 mA; V_{GS} = 4.5 V	–	–	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 340 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	65	140	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	9	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

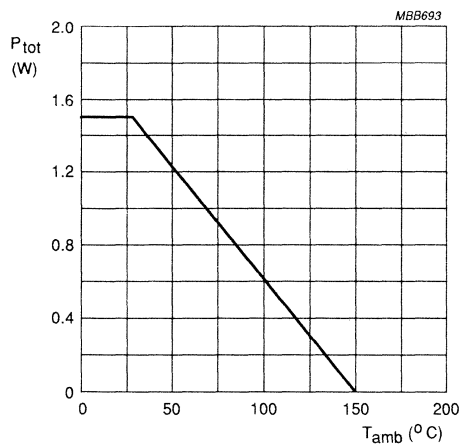
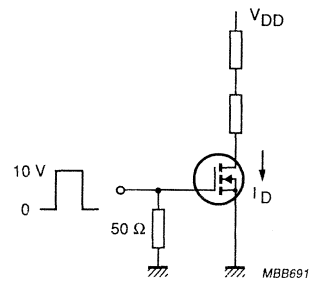


Fig.2 Power derating curve.



V_{DD} = 50 V.

Fig.3 Switching times test circuit.

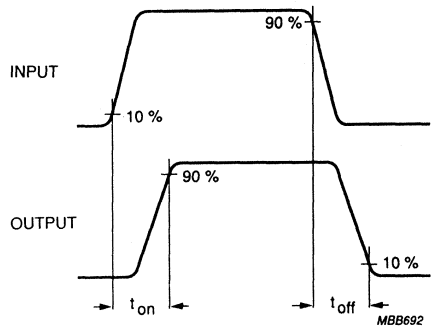


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSP92

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

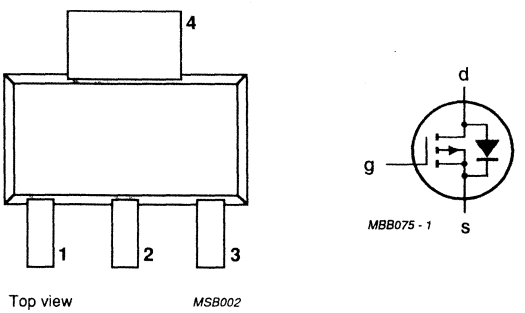


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

P-channel enhancement mode vertical D-MOS transistor

BSP92

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA; V_{GS} = 0	240	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$-V_{GS}$	gate-source voltage	$-I_D$ = 50 mA; $-V_{DS}$ = 5 V	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 180 mA; $-V_{GS}$ = 10 V	–	10	20	Ω
		$-I_D$ = 100 mA; $-V_{GS}$ = 5 V	–	–	18	Ω
		$-I_D$ = 25 mA; $-V_{GS}$ = 2.8 V	–	–	20	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 180 mA; $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	6	15	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	20	30	ns

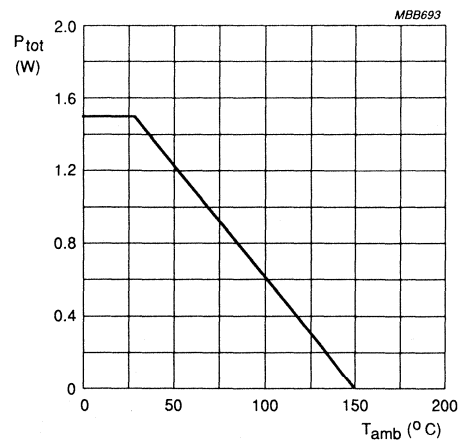
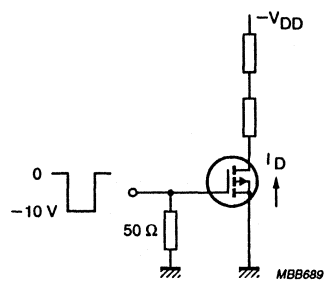


Fig.2 Power derating curve.



$-V_{DD}$ = 50 V.

Fig.3 Switching times test circuit.

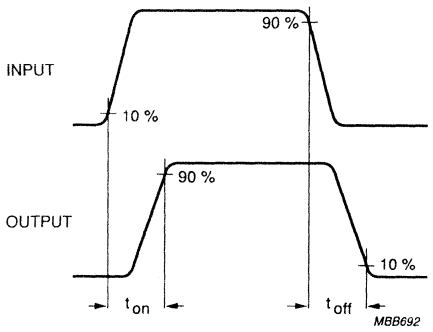


Fig.4 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP100

FEATURES

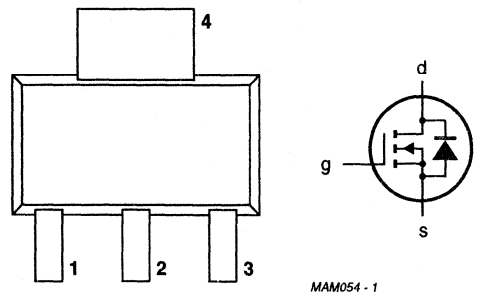
- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers, power switching, etc.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a plastic SOT223 SMD package.



Top view

Fig.1 Simplified outline and symbol.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.65	W

N-channel enhancement mode vertical D-MOS transistor

BSP100

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100°C$	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	up to T_s = 100 °C	–	5	W
		up to T_{amb} = 25 °C; note 2	–	1.65	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100°C$	–	2	A
I_{SM}	peak pulsed source current	note 1	–	7	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

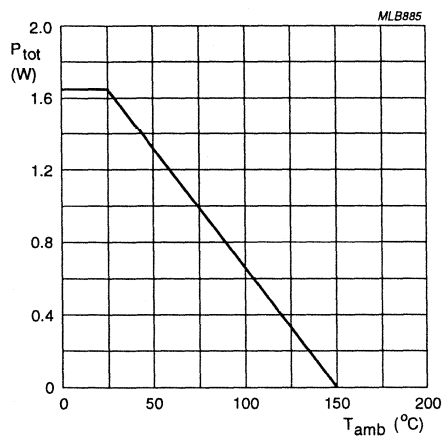
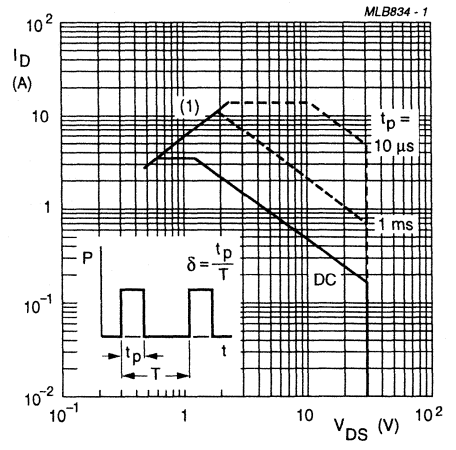


Fig.2 Power derating curve.



δ = 0.01.
Solder point temperature T_s = 100 °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR.

N-channel enhancement mode vertical D-MOS transistor

BSP100

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

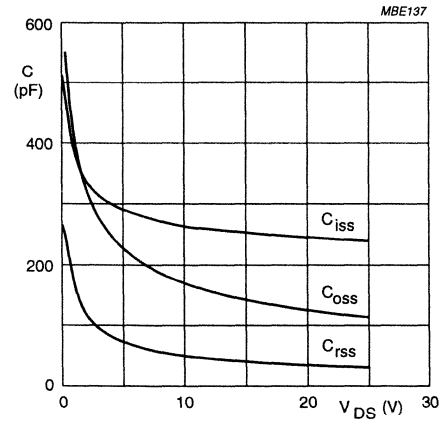
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	75	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GS} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns

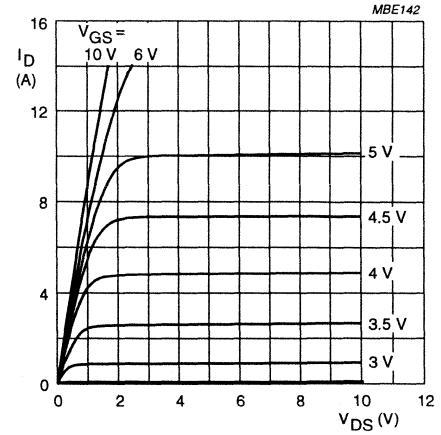
N-channel enhancement mode vertical D-MOS transistor

BSP100



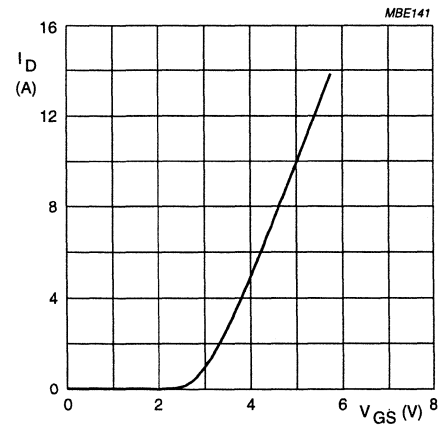
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



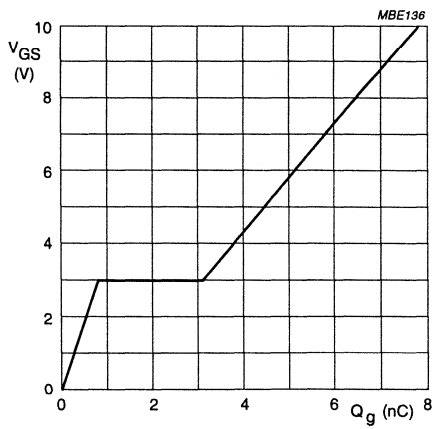
T_j = 25 °C.

Fig.5 Typical output characteristics.



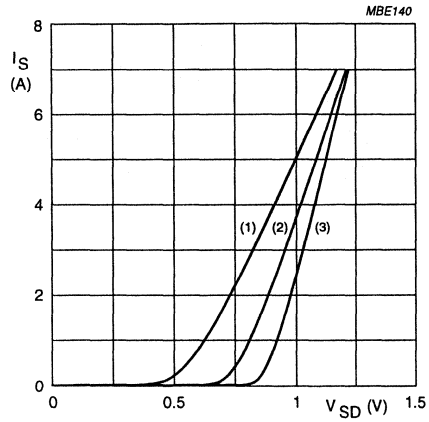
V_{DS} = 10 V.
T_j = 25 °C.

Fig.6 Typical transfer characteristics.



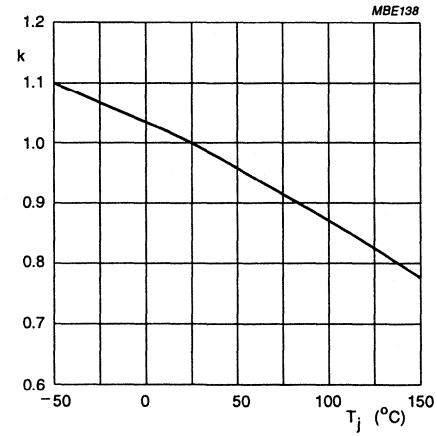
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.7 Gate-source voltage as a function of total gate charge.



$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

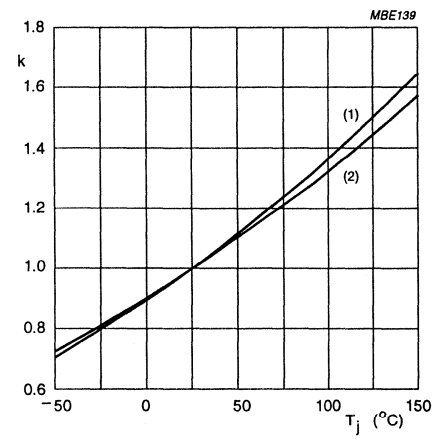
Fig.8 Source current as a function of source-drain diode forward voltage.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{th}$.

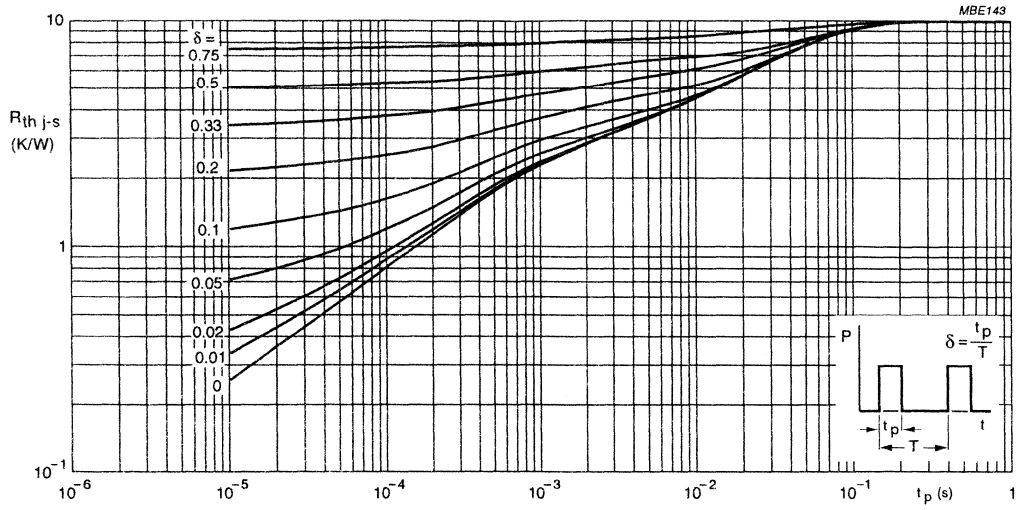
Fig.9 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) $I_D = 2.2$ A; $V_{GS} = 10$ V.
(2) $I_D = 1$ A; $V_{GS} = 4.5$ V.

Fig.10 Temperature coefficient of drain-source on-resistance.



Solder point temperature T_s = 100 °C.

Fig.11 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

BSP106
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

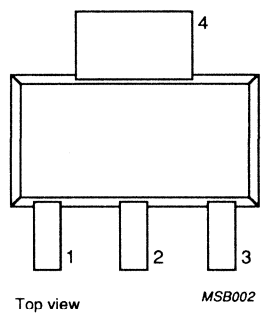


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP106

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP106

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
		V_{DS} = 25 V V_{GS} = 0	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	–	2.5	4	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10	–	10	15	ns

N-channel enhancement mode vertical D-MOS transistor

BSP106

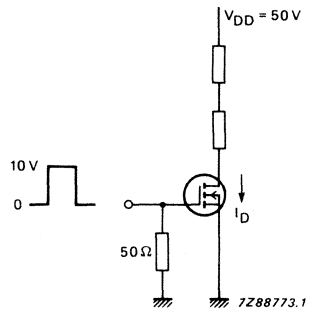


Fig.2 Switching time test circuit.

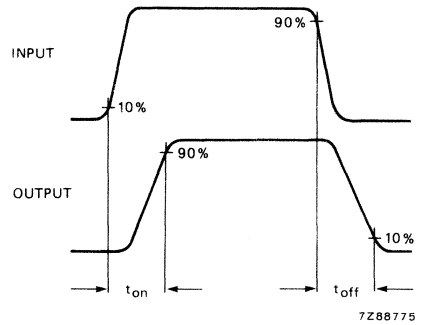


Fig.3 Input and output waveforms.

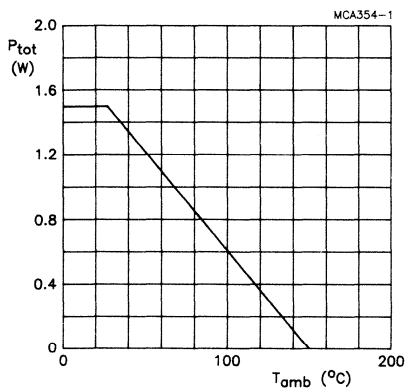


Fig.4 Power derating curve.

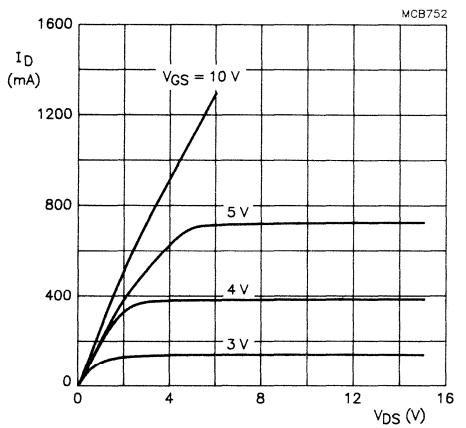


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

BSP106

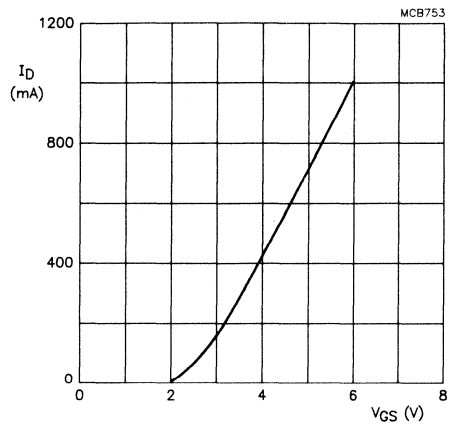


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

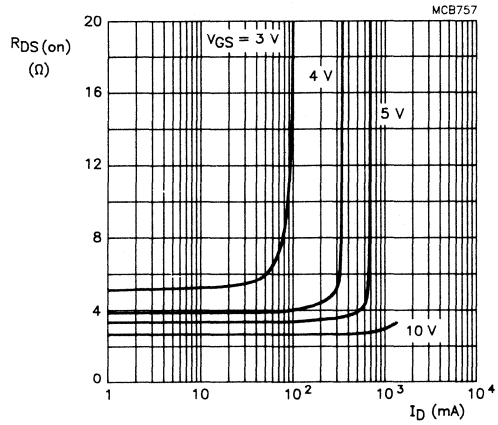


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

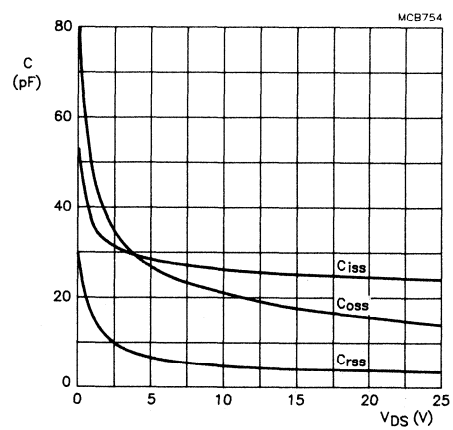


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

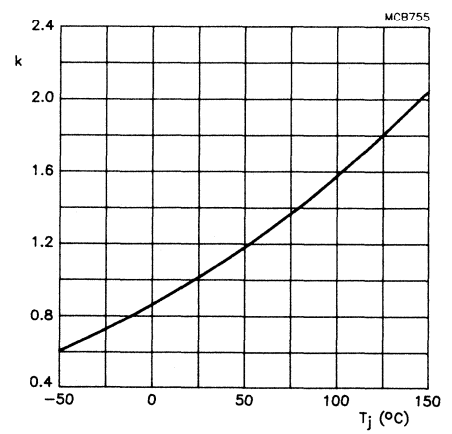


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at 200 mA/10 V.

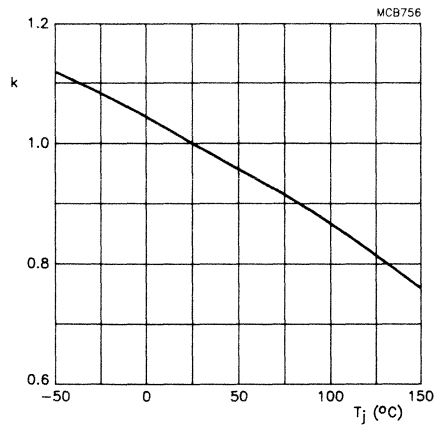


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BSP107

FEATURES

- Direct interface to C-MOS, TTL, etc due to low threshold voltage
- High-speed switching
- No secondary breakdown.

DESCRIPTION

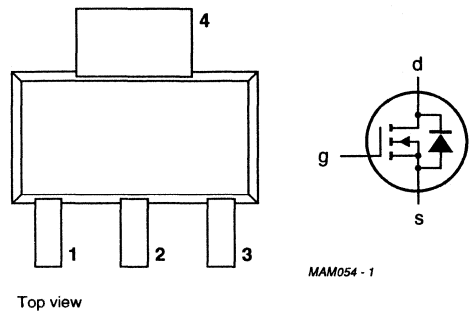
N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer driver switching.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
V_{GSth}	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	200	mA
R_{DSon}	drain-source on-state resistance	28	Ω



Top view

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP107

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	200	mA
I_{DM}	drain current	peak	-	350	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy printed circuit board, 40 mm x 40 mm x 1.5 mm. Mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 µA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSP107

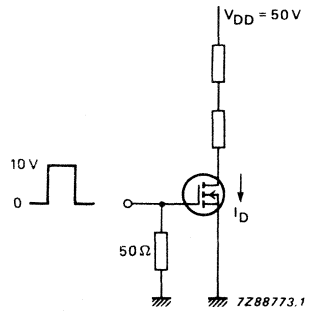


Fig.2 Switching time test circuit.

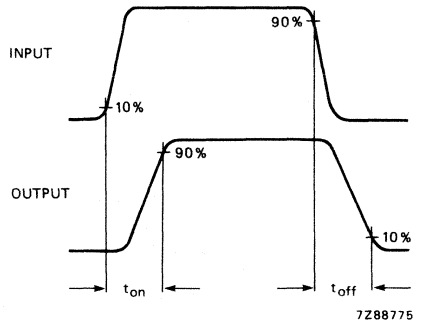


Fig.3 Input and output waveforms.

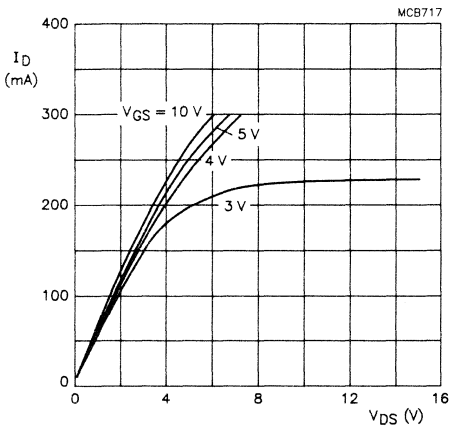


Fig.4 Typical output characteristics; T_j = 25° C.

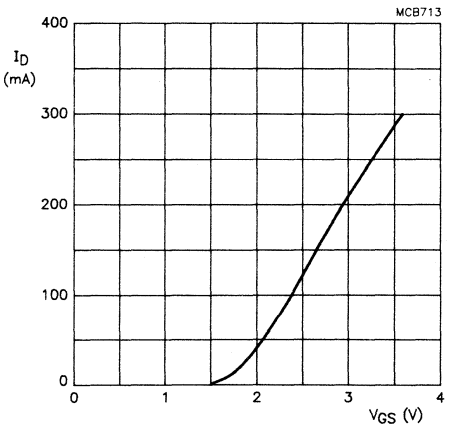


Fig.5 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25° C.

N-channel enhancement mode vertical D-MOS transistor

BSP107

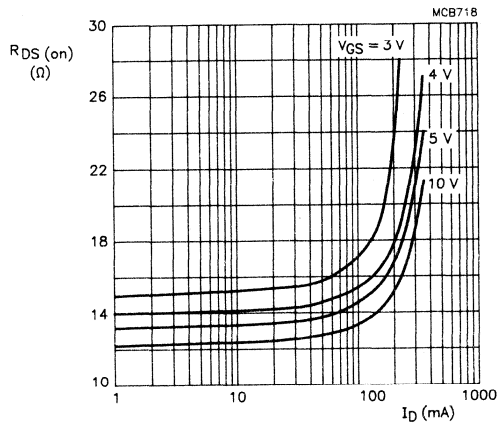


Fig.6 Typical on-resistance as a function of drain current; T_j = 25° C.

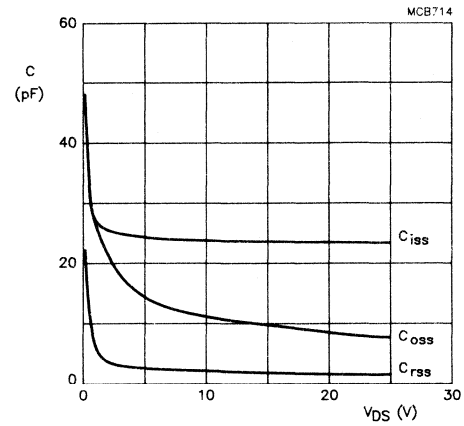


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25° C

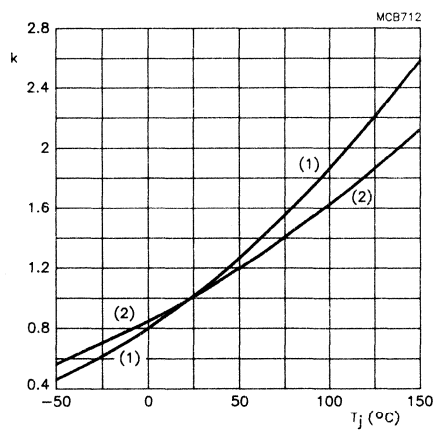


Fig.8 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25°C}$;

typical $R_{DS(on)}$ at 150 mA/10 V;

(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V;

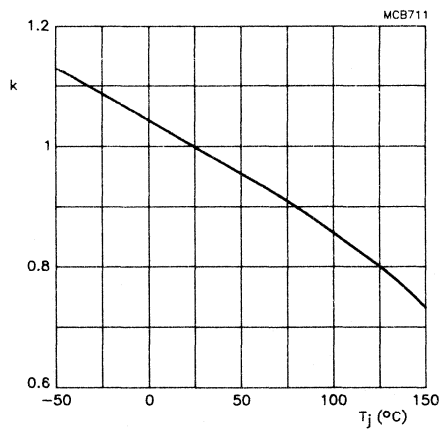


Fig.9 Temperature coefficient of gate-source threshold voltage;

$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25°C}$; typical $V_{Gs(th)}$ at 1 mA.

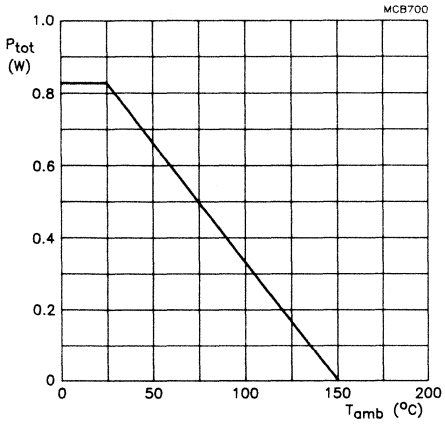


Fig.10 Power derating curve.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.0 Ω 3.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	min. typ.	150 mS 300 mS

MECHANICAL DATA

Dimensions in mm

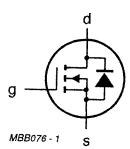
Fig.1 SOT223.

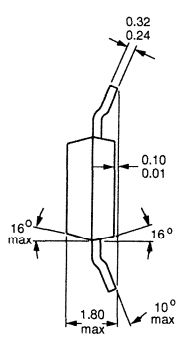
Marking code

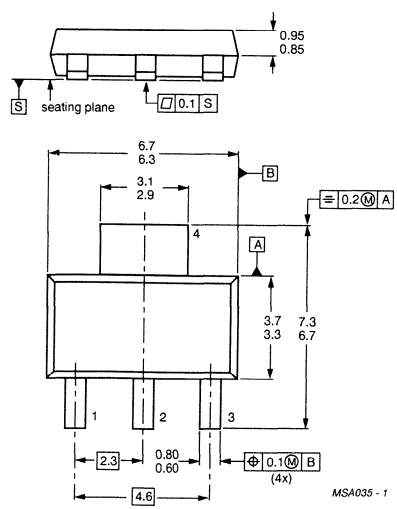
BSP108

Pinning

1 = gate
2 = drain
3 = source
4 = drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	500	mA
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	$R_{DS\ on}$	typ. max.	2.0 3.0	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	min. typ.	150 300	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 60	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 8	ns ns
	t_{off}	typ. max.	10 15	ns ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

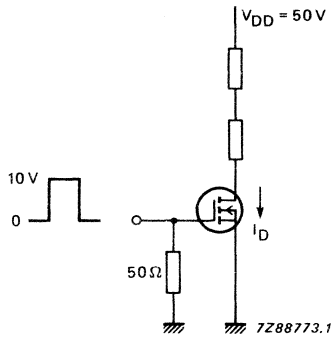


Fig.2 Switching times test circuit.

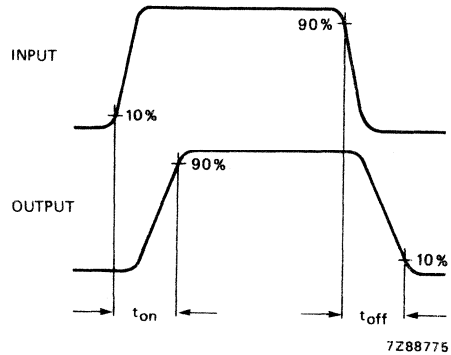


Fig.3 Input and output waveforms.

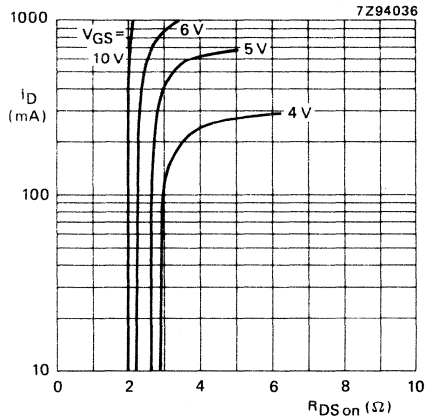


Fig.4 T_j = 25 °C; typical values.

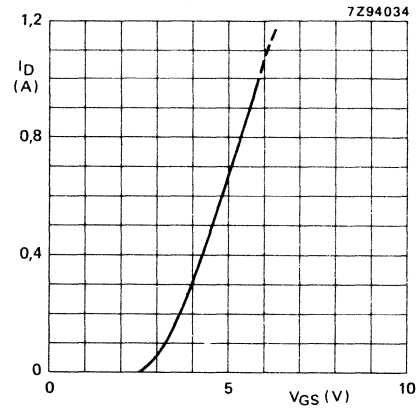


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

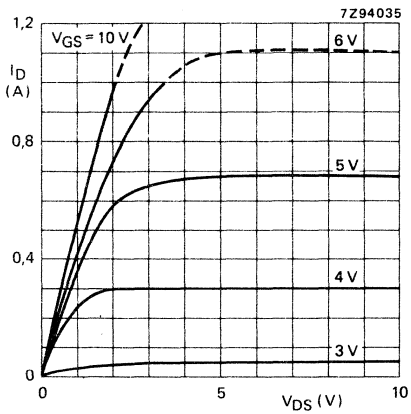


Fig.6 T_j = 25 °C; typical values.

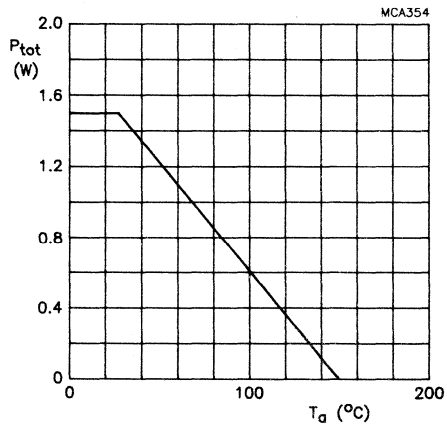


Fig.7 Power derating curve.

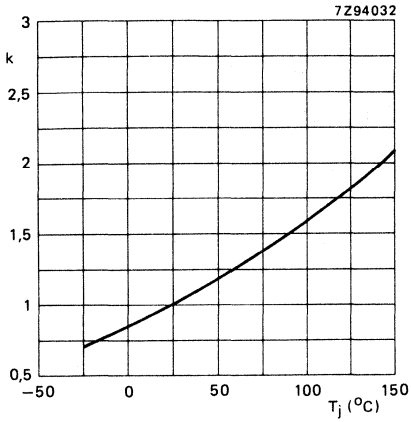


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; typ. values at 500 mA/10 V.

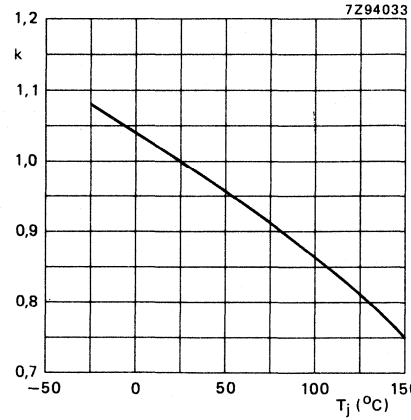


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

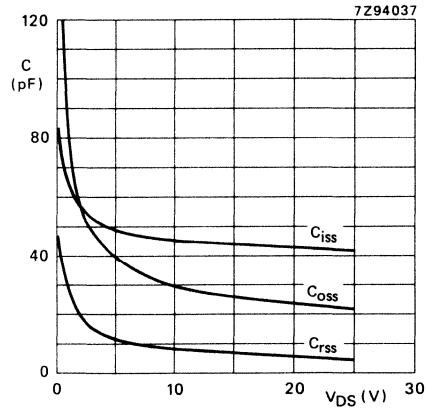


Fig.10 $T_j = 25\,^{o}C$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	325 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance I_D = 200 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 7 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	min. typ.	75 mS 150 mS

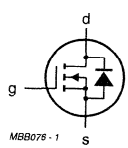
MECHANICAL DATA

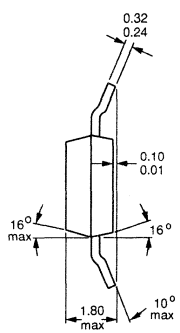
Fig.1 SOT223.

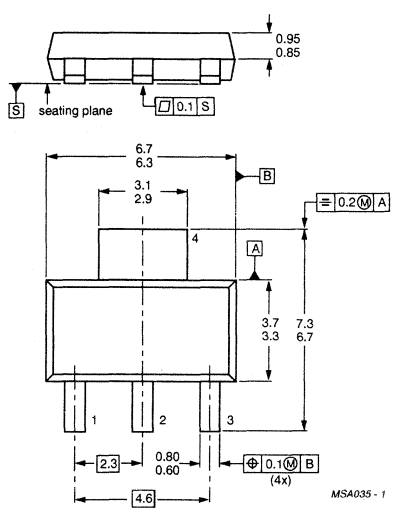
Dimensions in mm

Pinning

1 = gate
2 = drain
3 = source
4 = drain







Marking code

BSP110

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	325 mA
Drain current (peak)	I_{DM}	max.	650 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$I_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
I_D = 200 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 7 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	min. typ.	75 mS 150 mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 pF 20 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3 pF
		max.	6 pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	2 ns
		max.	5 ns
	t_{off}	typ.	5 ns
		max.	10 ns

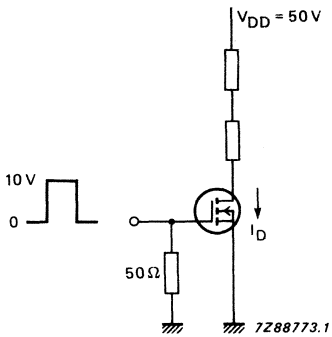


Fig.2 Switching time test circuit.

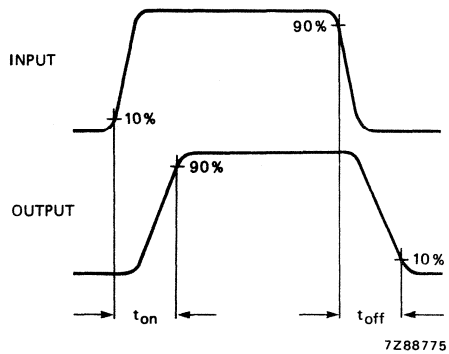


Fig.3 Input and output waveforms.

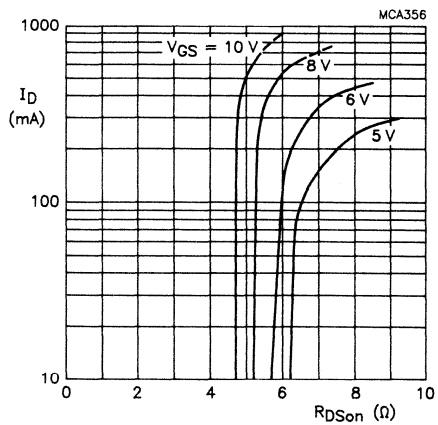


Fig.4 T_j = 25 °C; typical values.

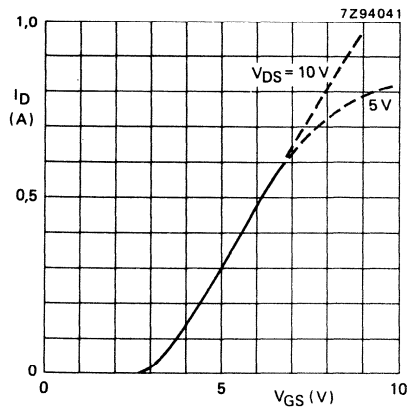


Fig.5 T_j = 25 °C; typical values.

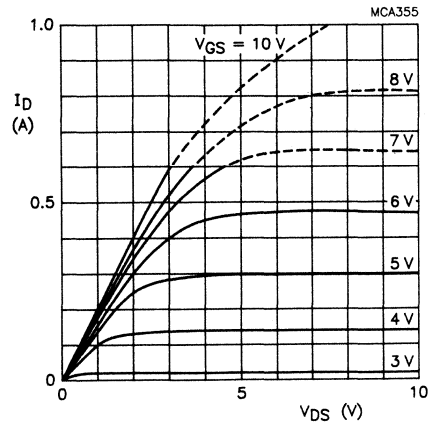


Fig.6 T_j = 25 °C; typical values.

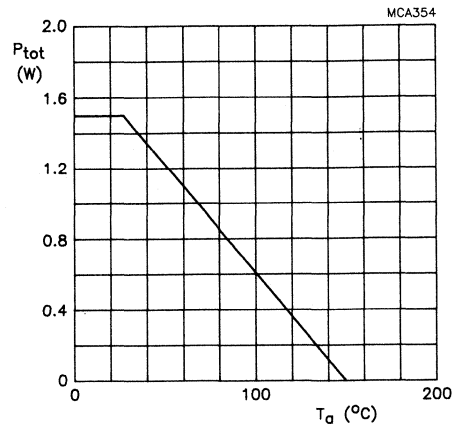


Fig.7 Power derating curve.

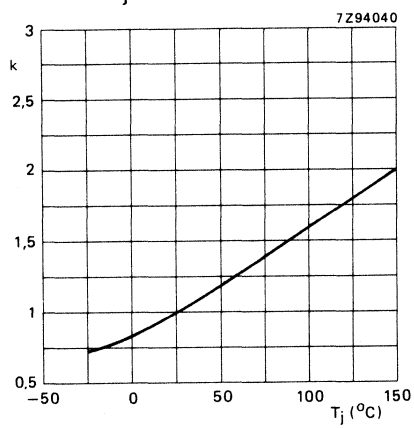


Fig.8 $k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ ^oC}$;

typical values at 150 mA/5 V.

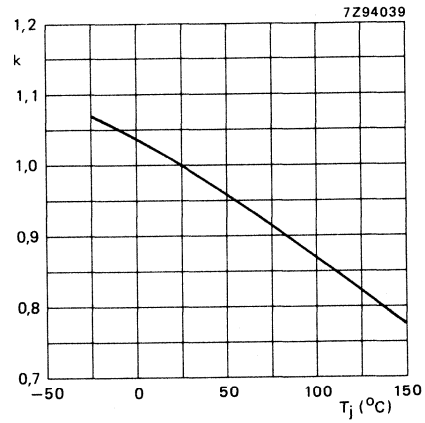


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$;

$V_{GS(th)}$ at 1 mA; typical values.

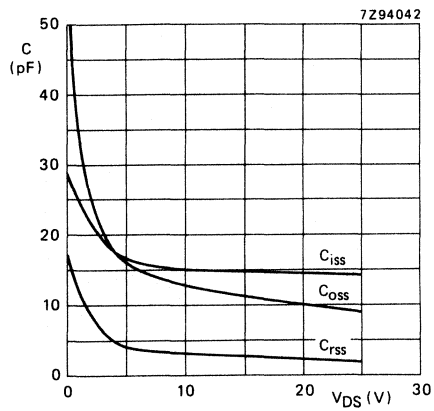


Fig.10 T_j = 25 °C; V_{GS} = 0;
f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Drain-current (DC)	I_D	max.	250 mA
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	7 Ω 12 Ω
Gate threshold voltage	$V_{GS(th)}$	max.	2.8 V

MECHANICAL DATA Dimensions in mm

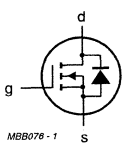
Fig.1 SOT223.

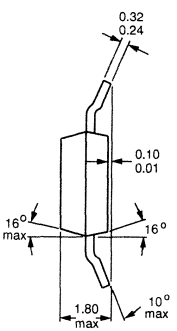
Marking code

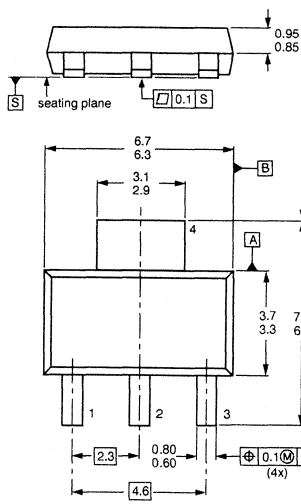
BSP120

Pinning

1 = gate
2 = drain
3 = source
4 = drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Drain-source ON-resistance (see Fig.4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	7 Ω 12 Ω
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	125 mS 250 mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 65 pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V;
V_{GS} = 0 to 10 V

t_{on}	typ.	3 ns
	max.	6 ns
t_{off}	typ.	15 ns
	max.	20 ns

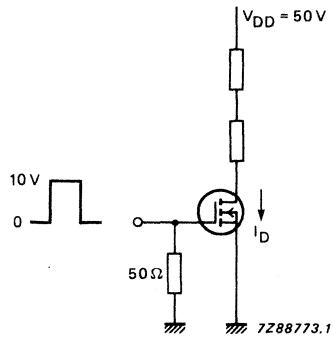


Fig.2 Switching time test circuit.

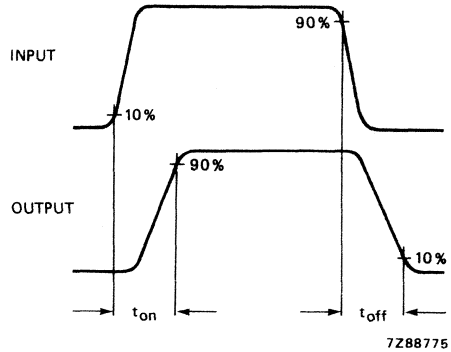


Fig.3 Input and output waveforms.

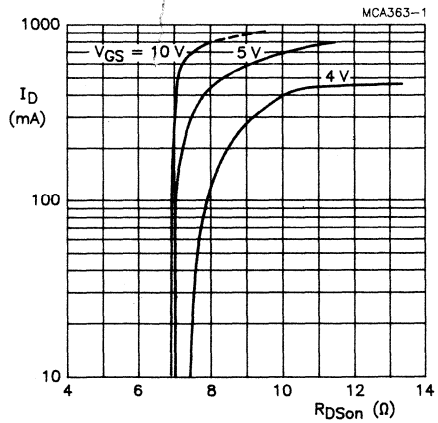


Fig.4 T_j = 25 °C; typical values.

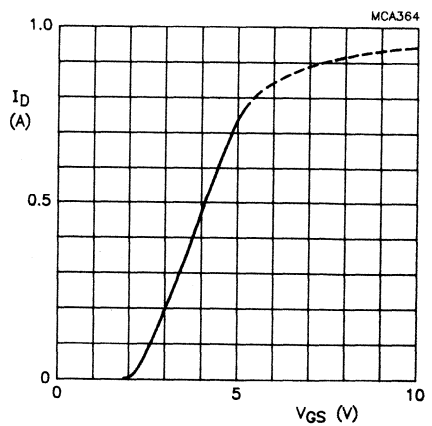


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

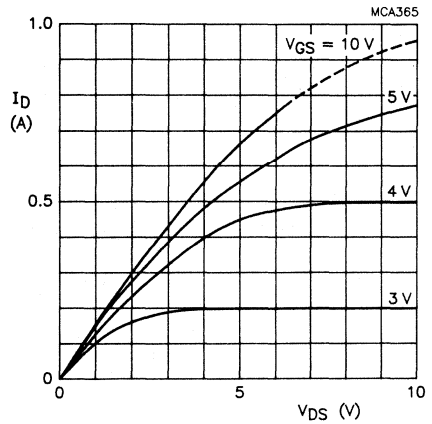


Fig.6 T_j = 25 °C; typical values.

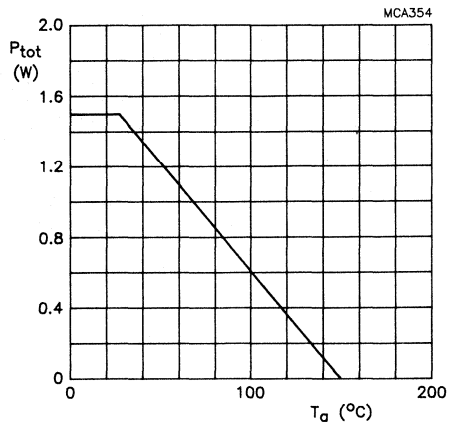


Fig.7 Power derating curve.

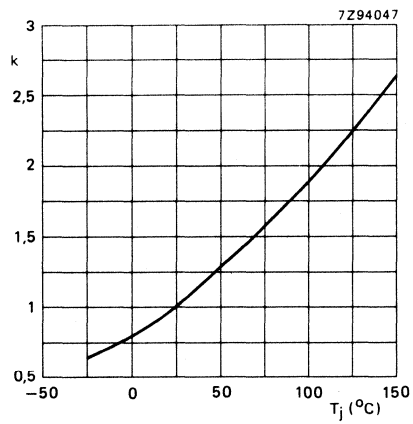


Fig.8 $k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ ^oC}$; at 250 mA/10 V; typical values.

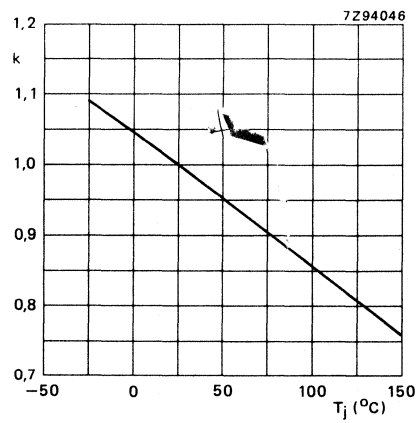


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

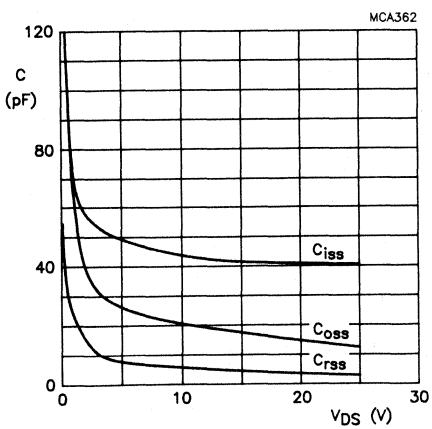


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

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Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min. typ.	200 mS 350 mS

MECHANICAL DATA

Dimensions in mm

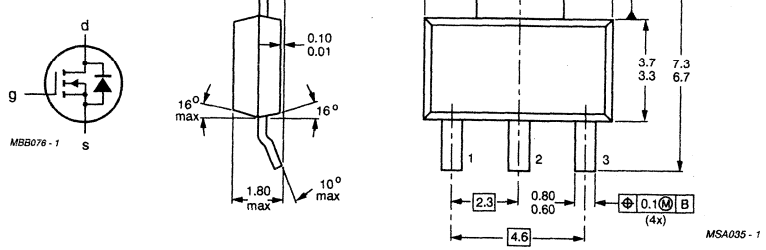
Fig.1 SOT223.

Pinning:

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP121



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{thj\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0 V_{DS} = 60 V; V_{GS} = 0	I_{DSS} I_{DSS}	max. max.	1.0 μA 200 nA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V

t_{on}	typ.	5	ns
	max.	10	ns
t_{off}	typ.	15	ns
	max.	20	ns

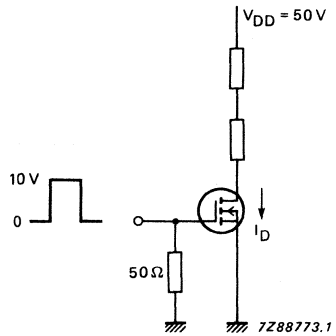


Fig.2 Switching time test circuit

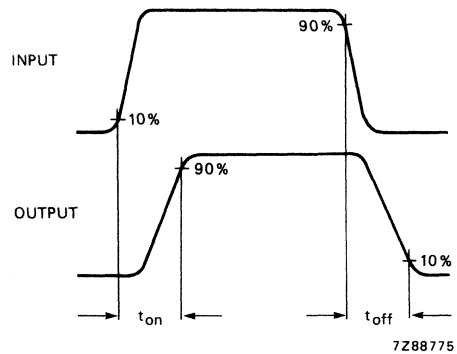


Fig.3 Input and output waveforms.

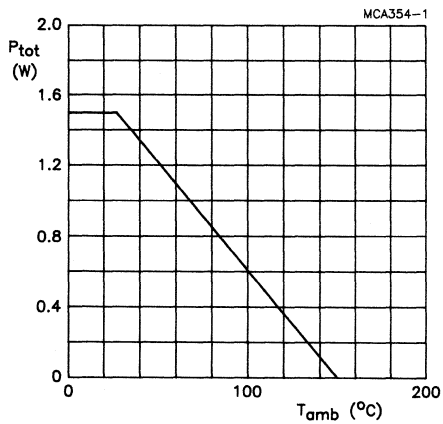


Fig.4 Power derating curve.

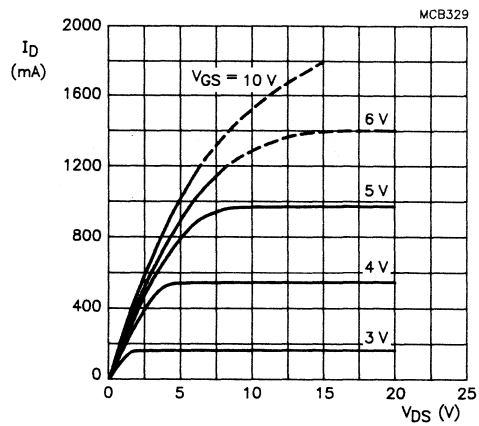


Fig.5 Output characteristic;
T_j = 25 °C; typical value.

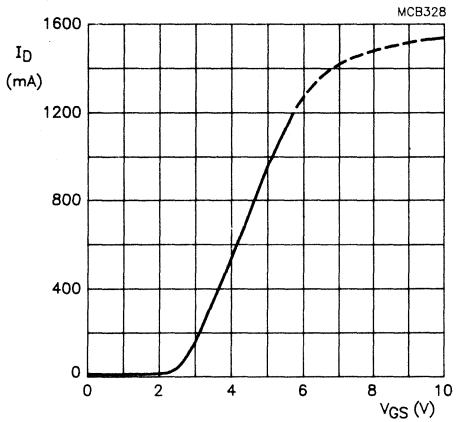


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical values.

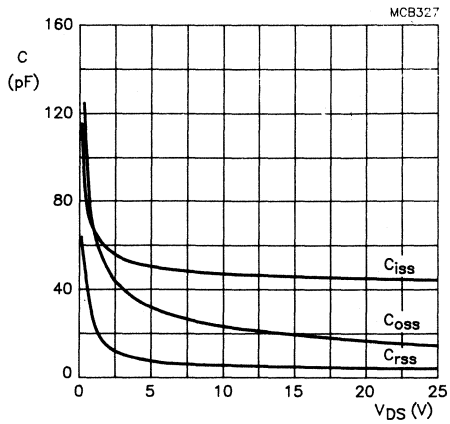


Fig.7 Capacitance as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

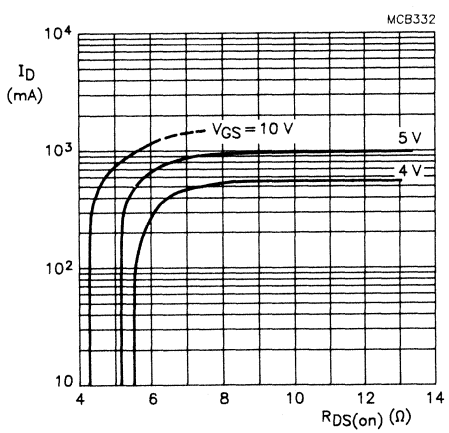


Fig.8 T_j = 25 °C; typical values.

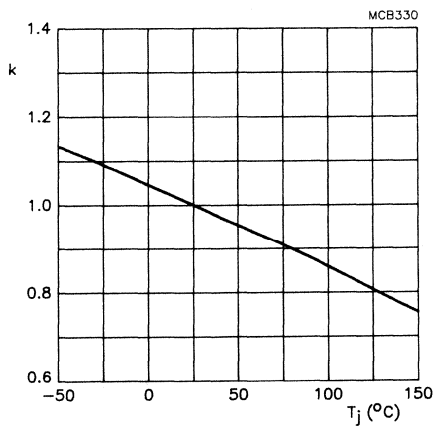


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

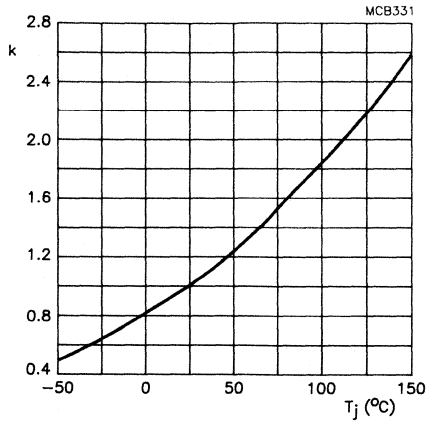


Fig.10 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^{o}C}$; at 400 mA/10V; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP122

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	550	mA
$R_{DS(on)}$	drain-source on-resistance	2.5	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

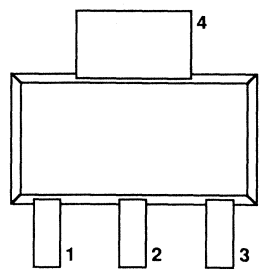


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

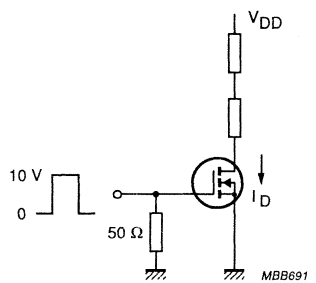
N-channel enhancement mode vertical D-MOS transistor

BSP122

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	1.6	2.5	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	2.5	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	800	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	165	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	40	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	9	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	35	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	50	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

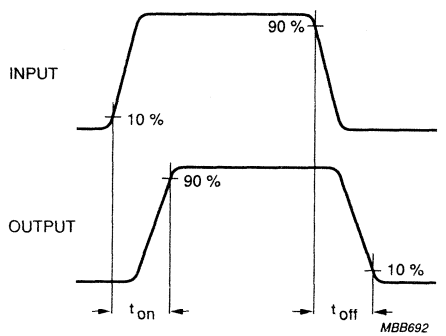


Fig.3 Input and output waveforms.

N-channel depletion mode vertical D-MOS transistor

BSP124

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 µA; V_{DS} = 60 V	–1.65	–0.75	V

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

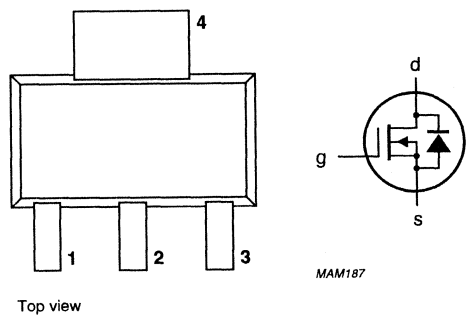


Fig.1 Simplified outline and symbol.

N-channel depletion mode vertical D-MOS transistor

BSP124

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm².

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = –3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = –3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	–1.65	–0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	–1.4	–0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = –3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = –3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to –3 V	–	30	ns

N-channel depletion mode vertical D-MOS transistor

BSP124

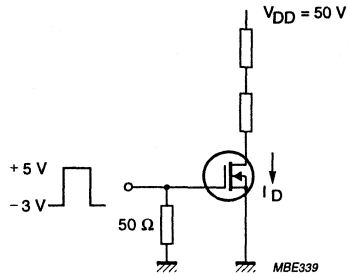


Fig.2 Switching times test circuit.

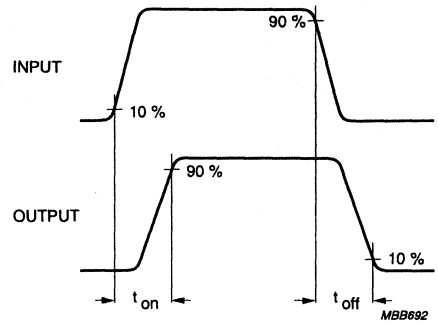


Fig.3 Input and output waveforms.

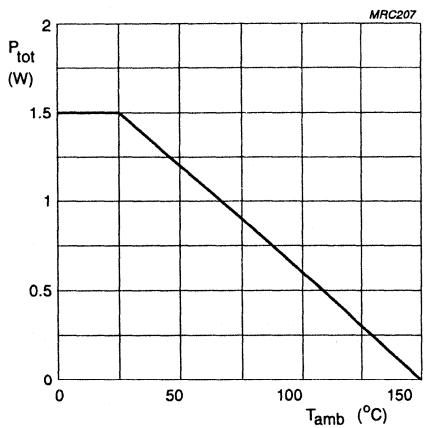
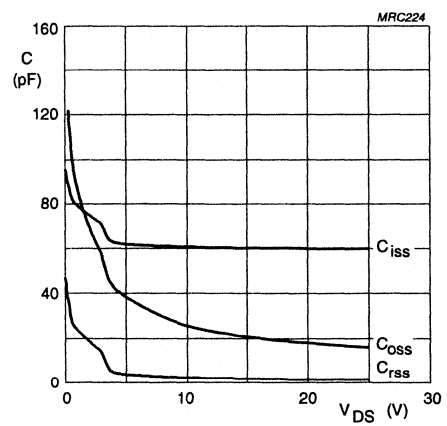


Fig.4 Power derating curve.

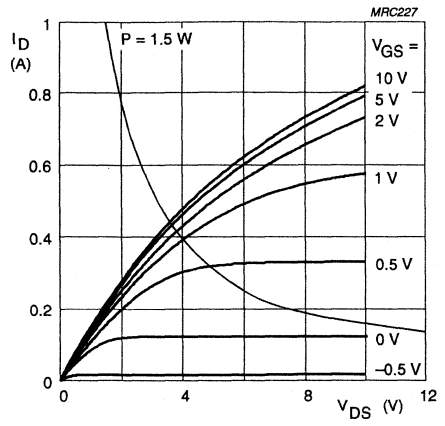


V_{GS} = −3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.

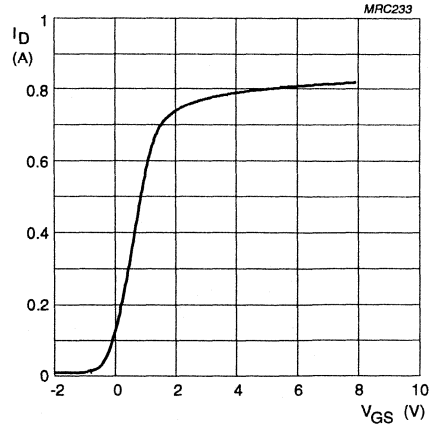
N-channel depletion mode vertical D-MOS transistor

BSP124



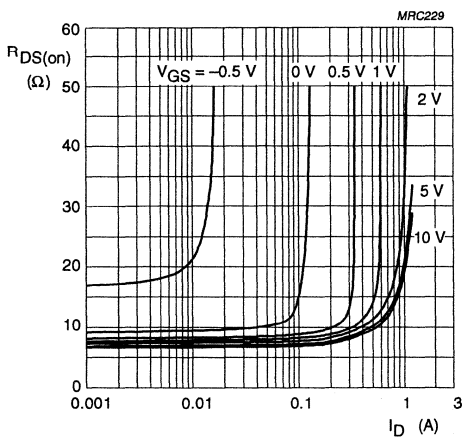
T_j = 25 °C.

Fig.6 Typical output characteristics.



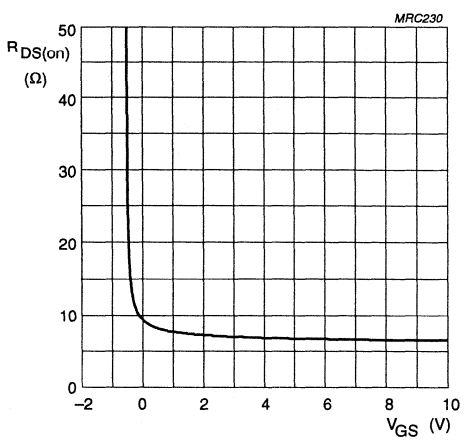
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

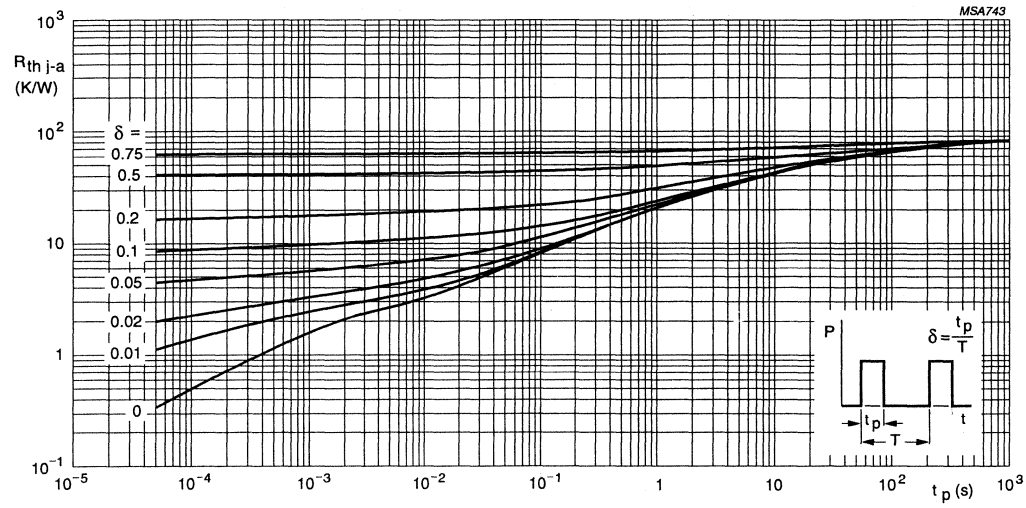
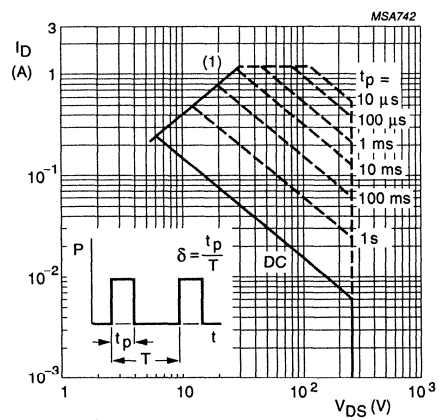


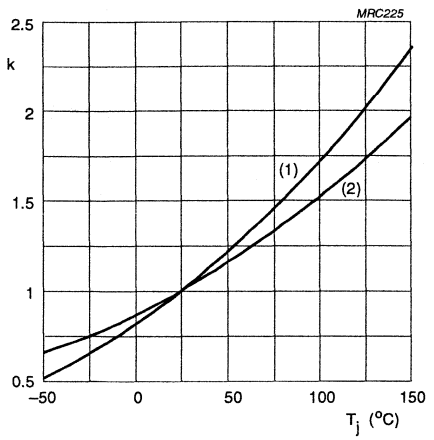
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



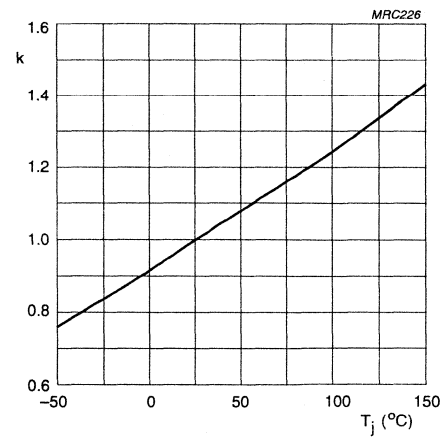
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\,°C}$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,°C}$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

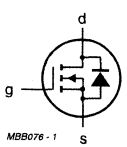
MECHANICAL DATA

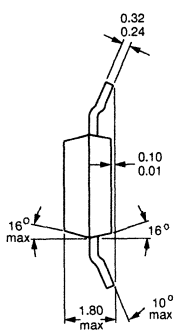
Fig.1 SOT223.

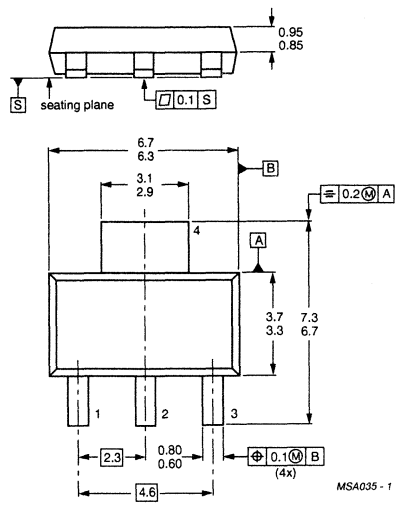
Dimensions in mm

Pinning

1 = gate
2 = drain
3 = source
4 = drain







Marking code

BSP126

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250 V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.0 V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 400 mS
Input capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 pF 90 pF
Output capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 15 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V;
V_{GS} = 0 to 10 V

t_{on}	typ.	5 ns
	max.	10 ns
t_{off}	typ.	20 ns
	max.	30 ns

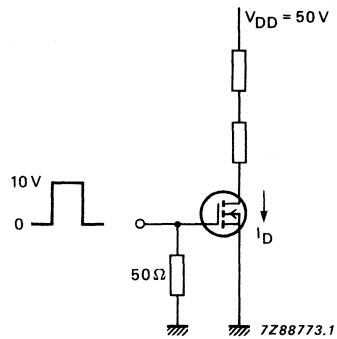


Fig.2 Switching time test circuit.

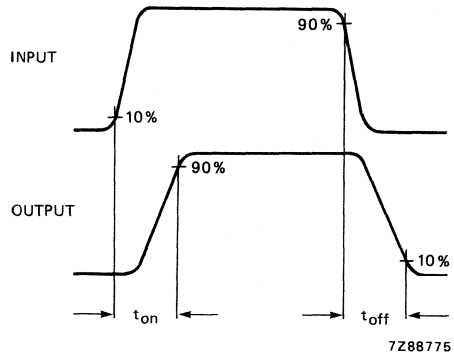


Fig.3 Input and output waveforms.

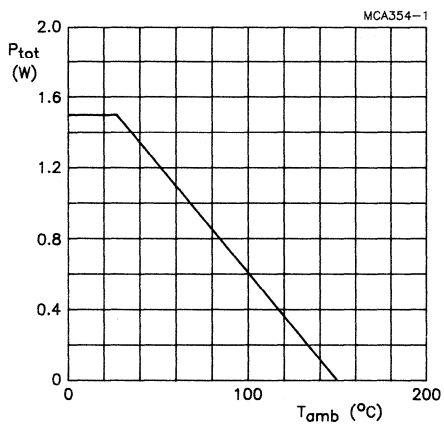


Fig.4 Power derating curve.

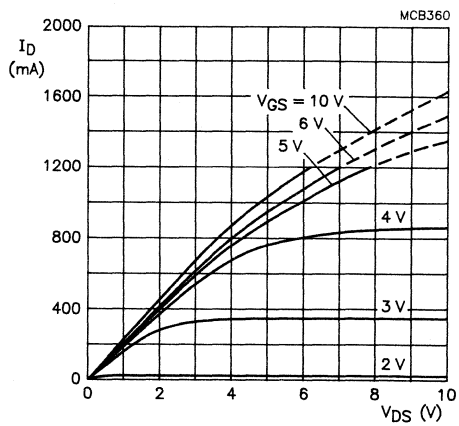


Fig.5 Output characteristics; T_j = 25 °C; typical values.

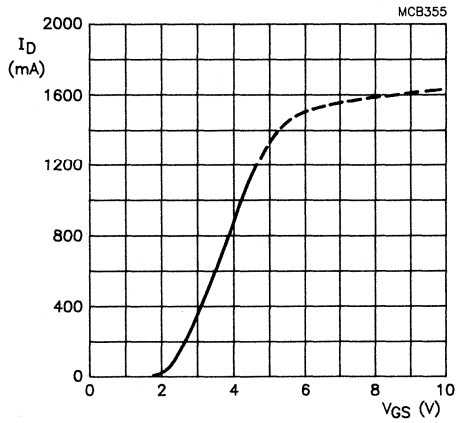


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

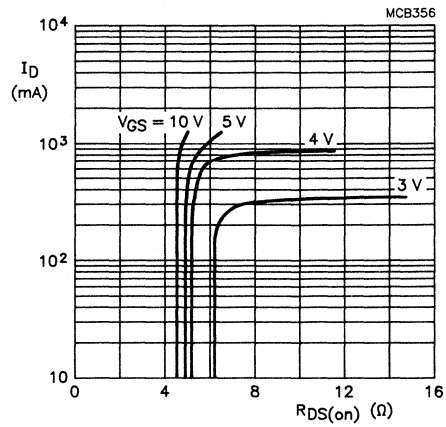


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

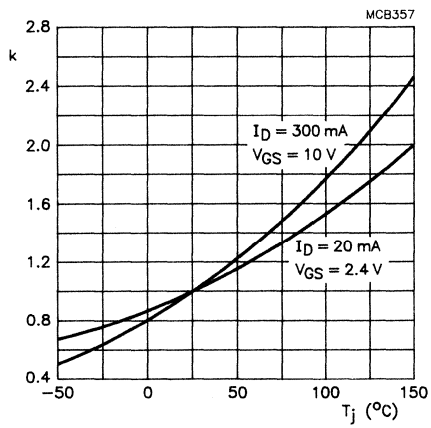


Fig.8 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^\circ C}$; typical values.

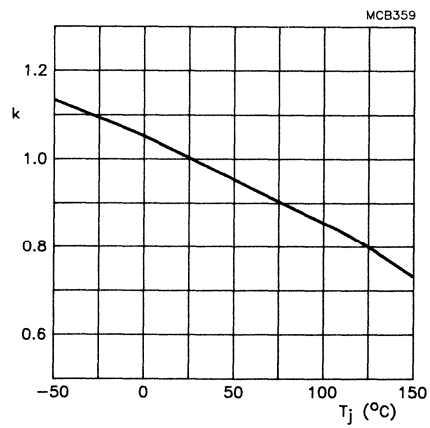


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^\circ C}$; $V_{GS(th)}$ at 1 mA; typical values.

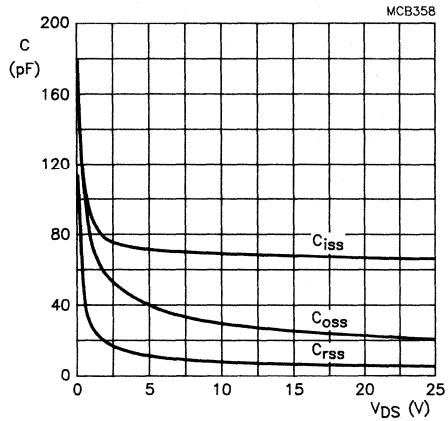


Fig.10 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP127

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
Code: BSP127	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

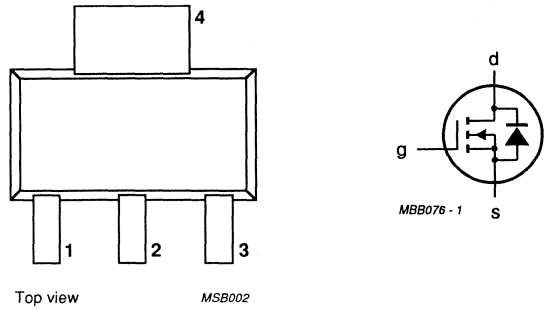


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

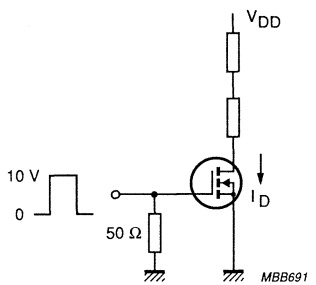
N-channel enhancement mode vertical D-MOS transistor

BSP127

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	270	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.5	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	55	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

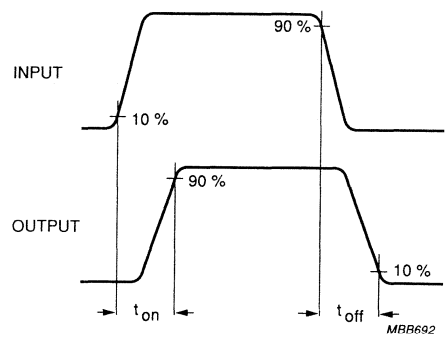


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP128

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
Code: BSP128	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

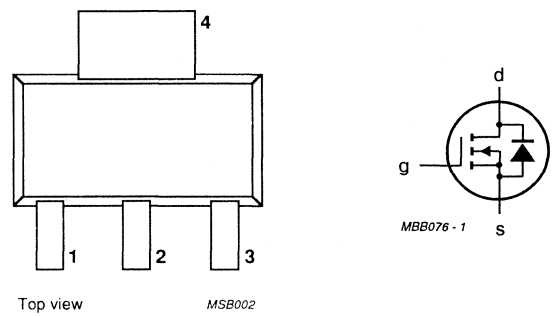


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

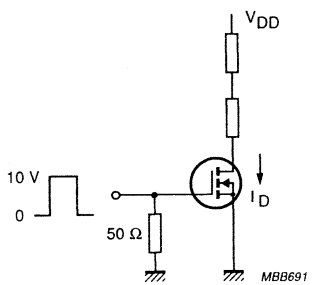
N-channel enhancement mode vertical D-MOS transistor

BSP128

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

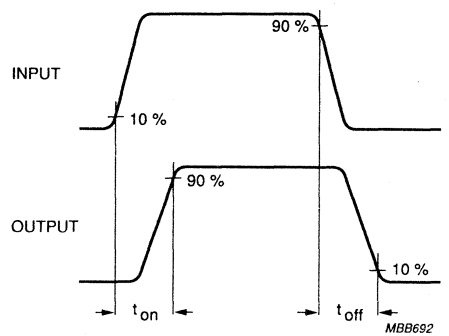


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP130

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

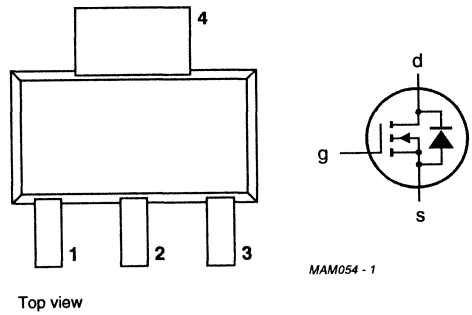
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	0.8	2	V



Top view

Marking code
BSP130.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP130

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	300	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm².

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
		I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

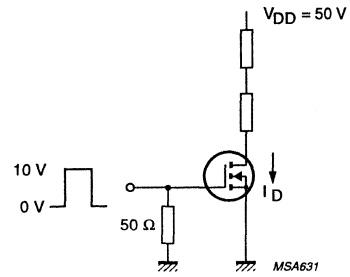


Fig.2 Switching times test circuit.

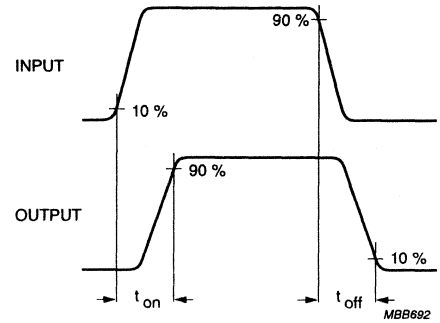


Fig.3 Input and output waveforms.

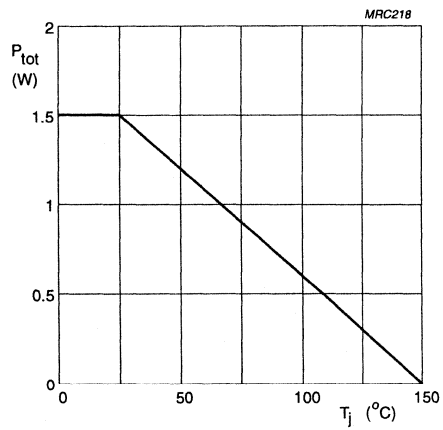
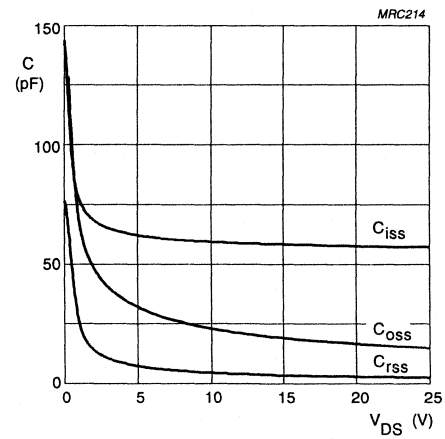


Fig.4 Power derating curve.

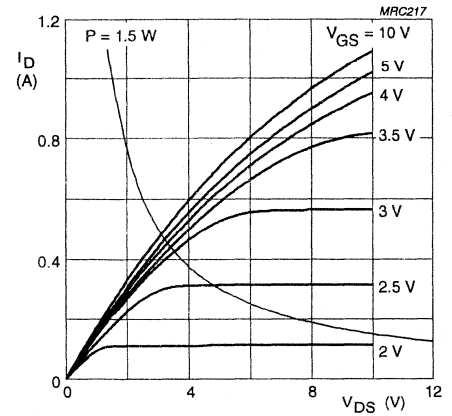


V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.

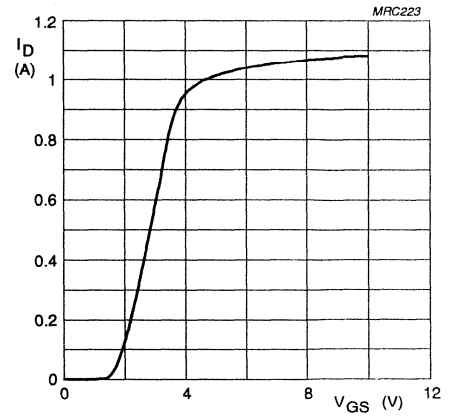
N-channel enhancement mode vertical D-MOS transistor

BSP130



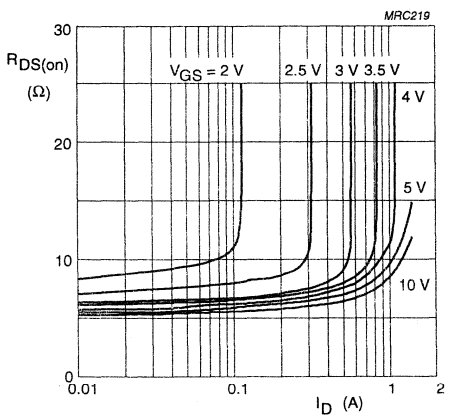
T_j = 25 °C.

Fig.6 Typical output characteristics.



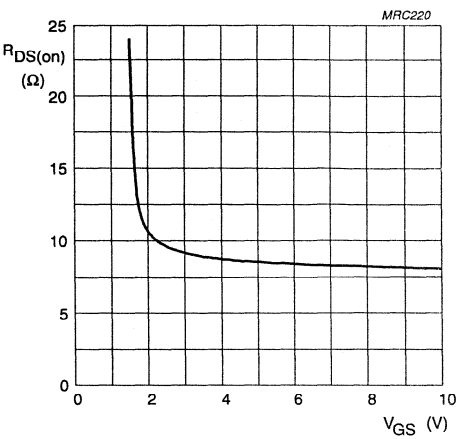
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

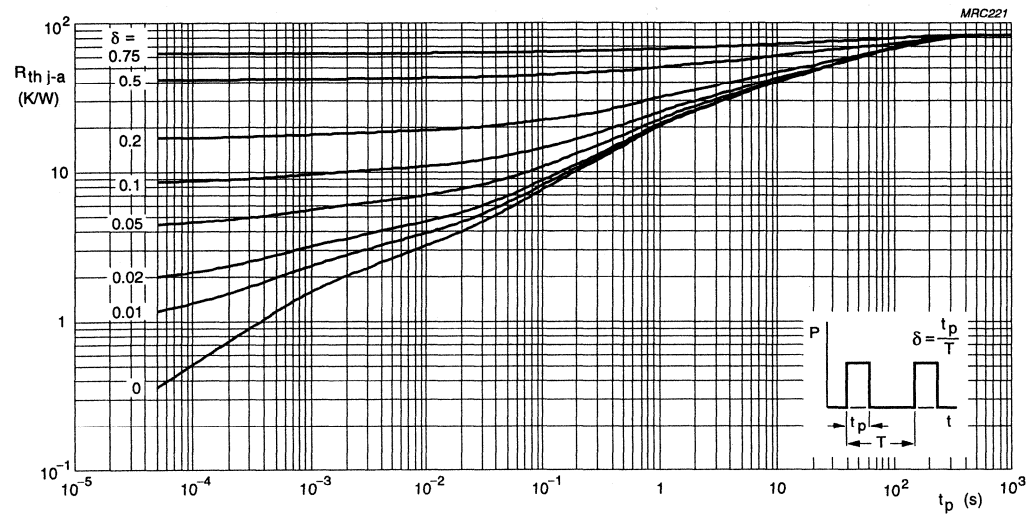
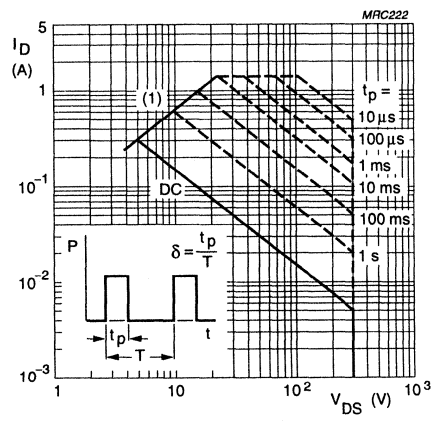


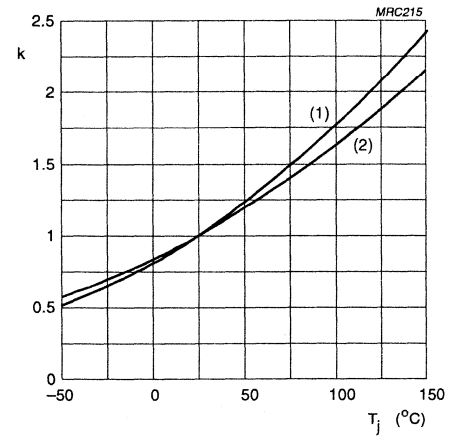
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



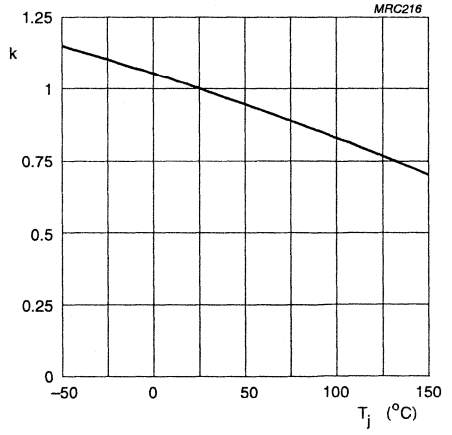
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$;

(1) I_D = 250 mA; V_{GS} = 10 V.

(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP145

FEATURES

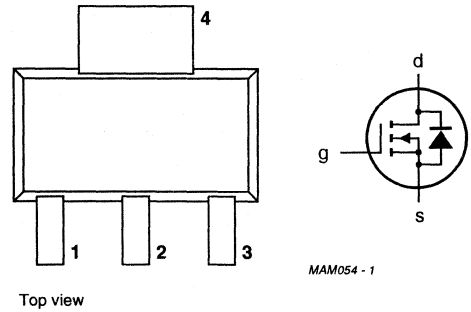
- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for applications in relay, high speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.



Top view

Fig.1 Simplified outline and symbol.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	450	V
V_{GSO}	gate-source voltage	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	3	4	V
I_D	drain current		–	250	mA
R_{DSon}	drain-source on-state resistance	I_D = 100 mA; V_{GS} = 10 V	10	14	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W

N-channel enhancement mode vertical D-MOS transistor

BSP145

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	450	V
V_{GSO}	gate-source voltage	open drain	–	±20	V
I_D	drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	83.3	K/W

Note to the "Limiting values" **and** "Thermal characteristics"

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	450	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3	4	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 350 V	–	–	1	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 100 mA	–	10	14	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 25 V; I_D =250 mA	200	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 25 V; f = 1 MHz	–	90	120	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 25 V; f = 1 MHz	–	25	35	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 25 V; f = 1 MHz	–	2	5	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 200 V; I_D = 100 mA	–	–	10	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} =200 V; I_D = 100 mA	–	–	100	ns

N-channel enhancement mode vertical D-MOS transistor

BSP145

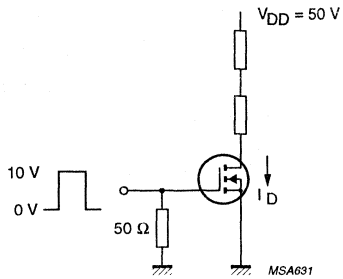


Fig.2 Switching time test circuit.

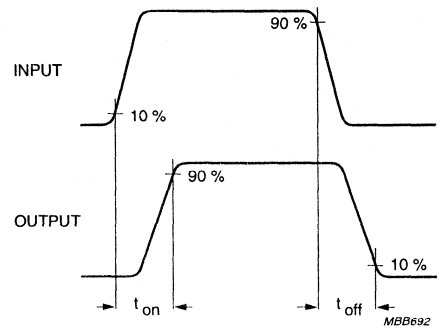


Fig.3 Input and output waveforms.

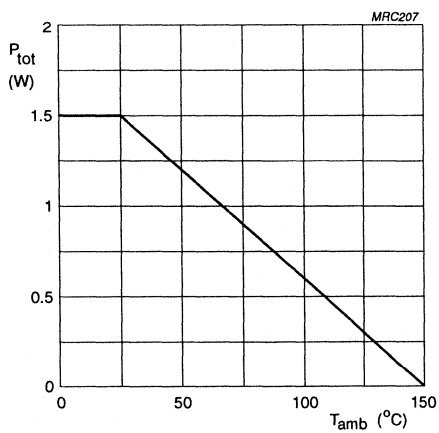
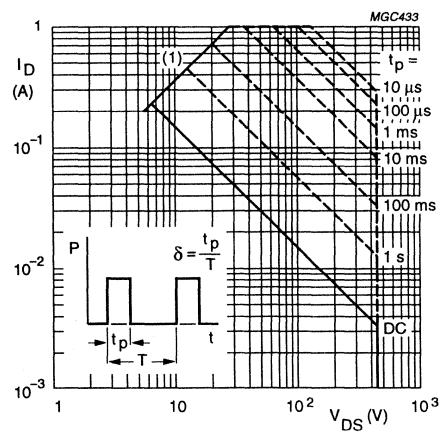


Fig.4 Power derating curve.

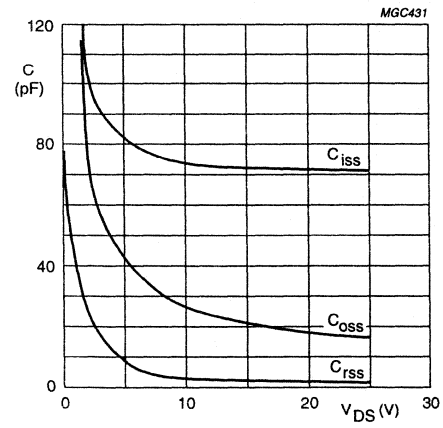


δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

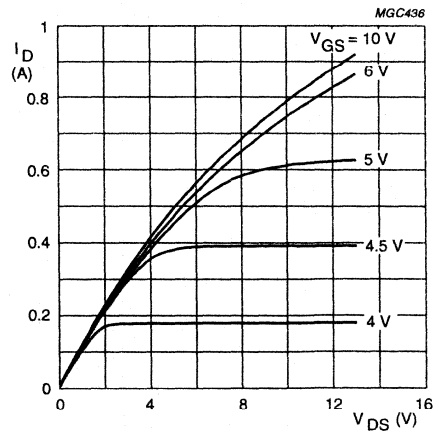
N-channel enhancement mode vertical D-MOS transistor

BSP145



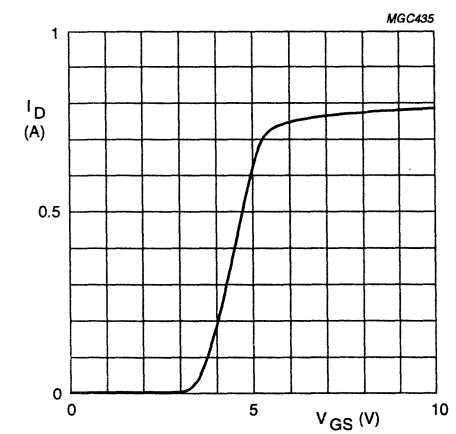
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



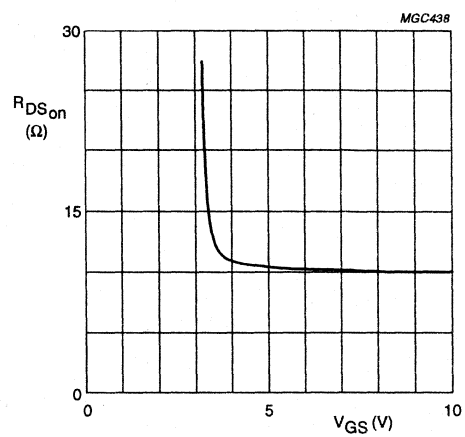
T_j = 25 °C.

Fig.7 Typical output characteristics.



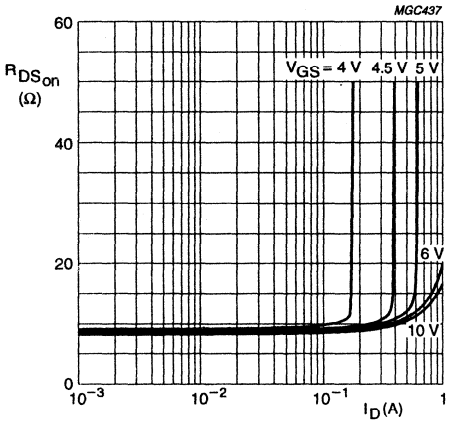
V_{DS} = 10 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



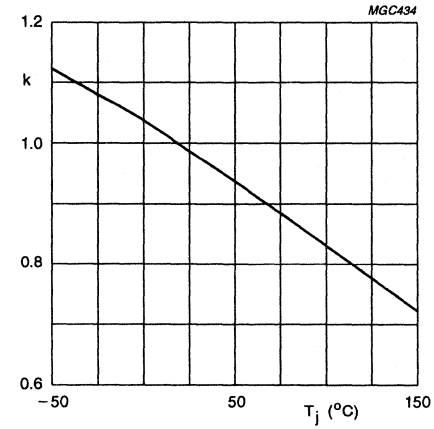
I_D = 10 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C.

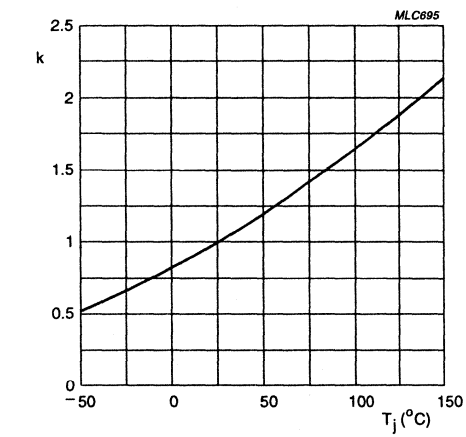
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\ °C}$$

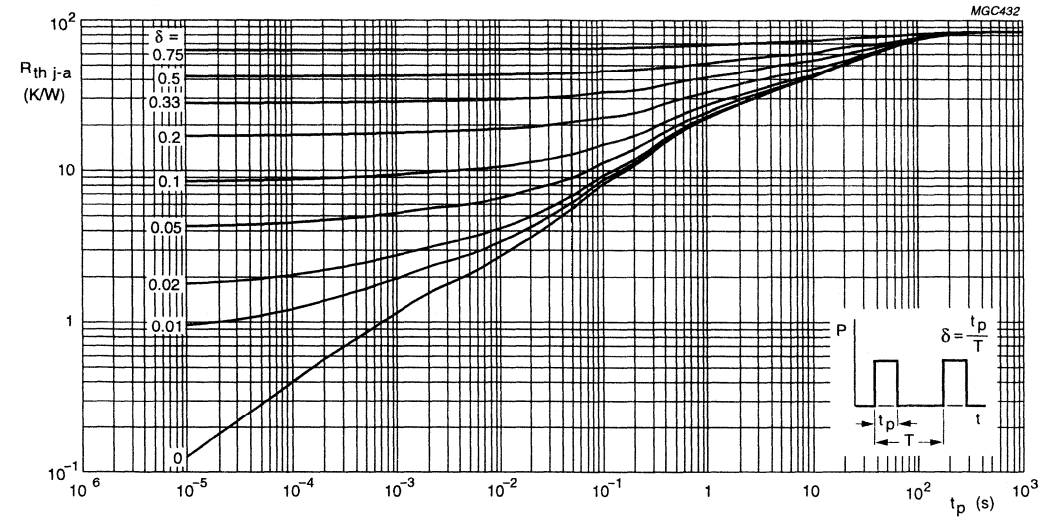
I_D = 1 mA; V_{DS} = V_{GS}.

Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Thermal resistance from junction to ambient as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP152

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

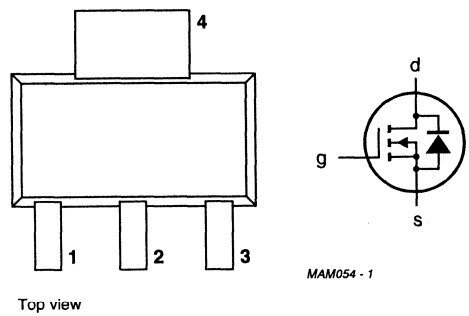
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
I_D	DC drain current		–	550	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	2.5	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1.5	3.5	V



Top view

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP152

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm².

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 40 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1.5	–	3.5	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	–	2.5	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	–	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	100	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	42	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	8	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	15	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	–	30	ns

N-channel enhancement mode vertical D-MOS transistor

BSP152

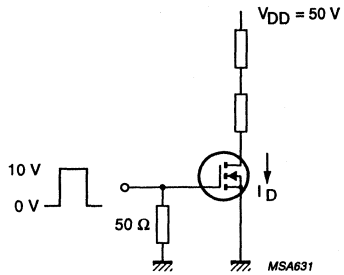


Fig.2 Switching times test circuit.

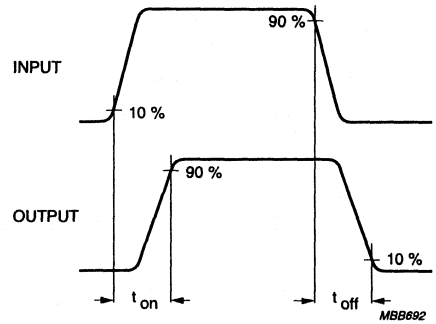


Fig.3 Input and output waveforms.

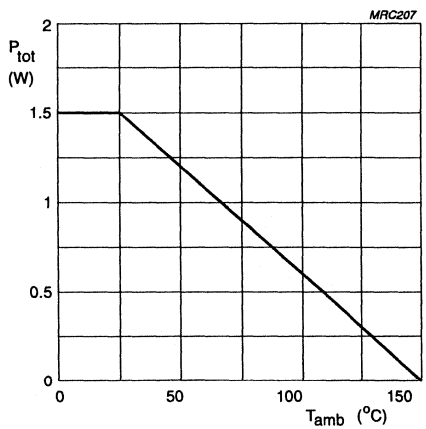
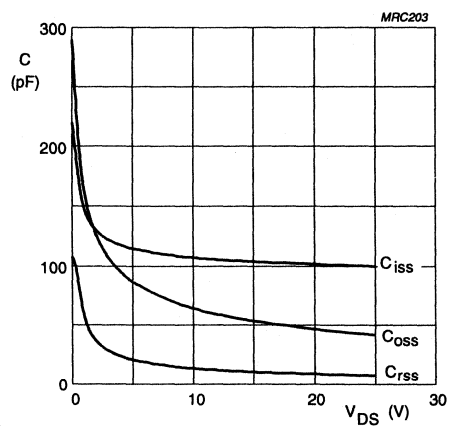
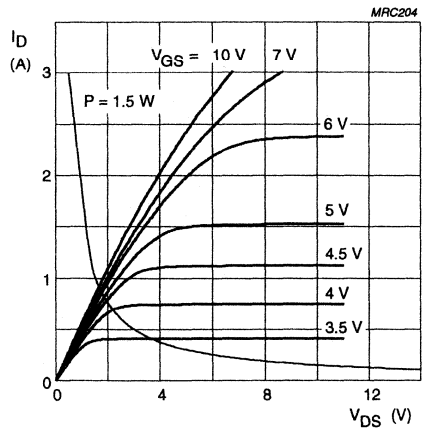


Fig.4 Power derating curve.



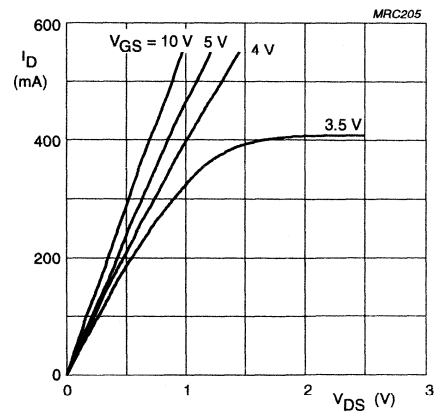
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



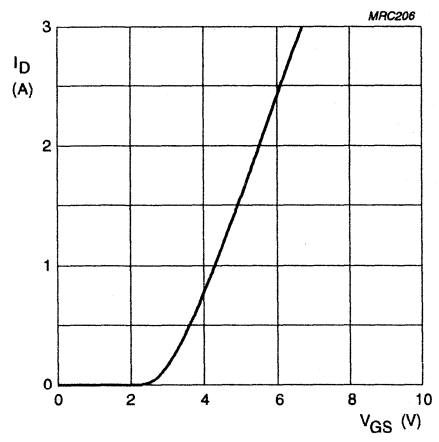
T_j = 25 °C.

Fig.6 Typical output characteristics.



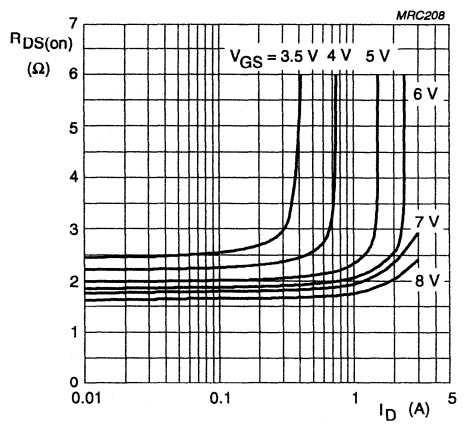
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics.

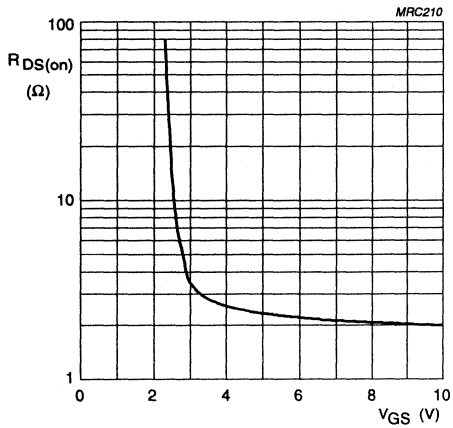


T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of drain current, typical values.

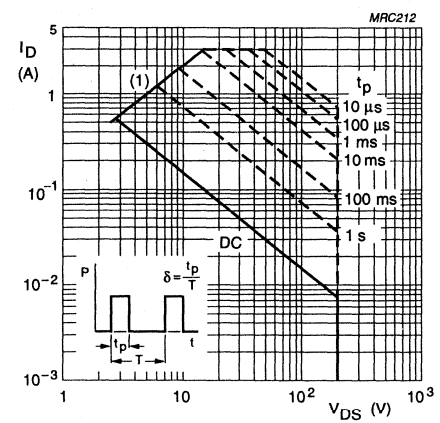
N-channel enhancement mode vertical D-MOS transistor

BSP152



V_{DS} = 100 mV; T_j = 25 °C.

Fig.10 Drain-source on-resistance as a function of gate-source voltage, typical values.



δ = 0.01; T_{amb} = 25 °C.

(1) R_{DSon} limitation.

Fig.11 SOAR curve.

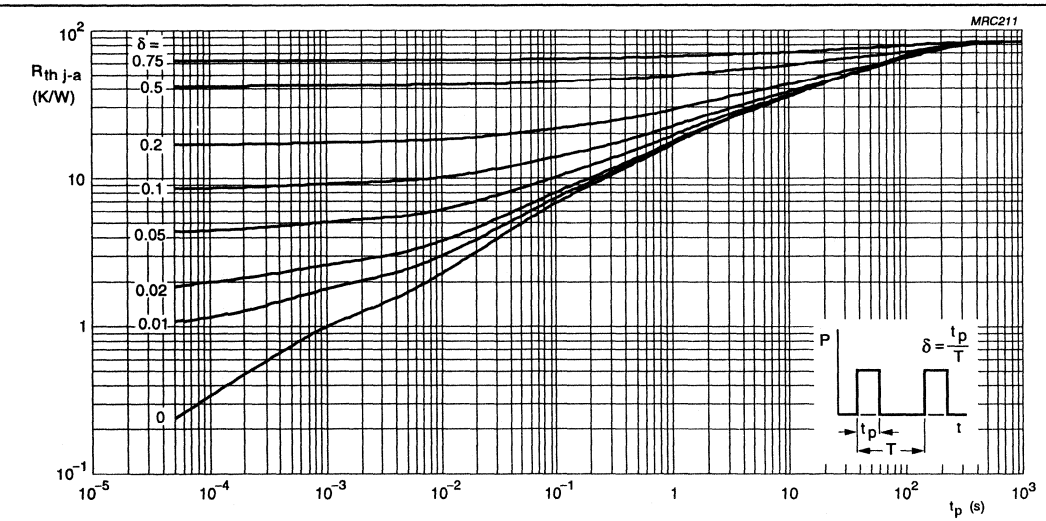
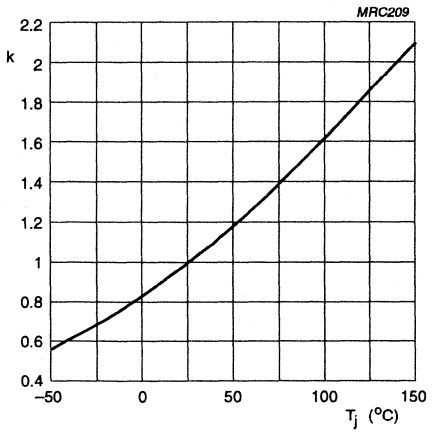


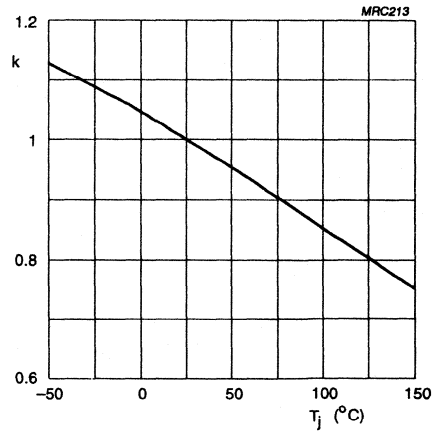
Fig.12 Transient thermal resistance from junction to ambient as a function of pulse time.



$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical R_{DSon} at I_D = 750 mA; V_{GS} = 10 V.

Fig.13 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at I_D = 1 mA.

Fig.14 Temperature coefficient of gate-source threshold voltage.

Data sheet	
status	Product specification
date of issue	April 1995

BSP204/BSP204A
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant (BSP204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

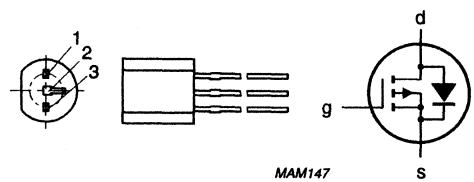


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
$-I_D$	drain current	DC value	–	250	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

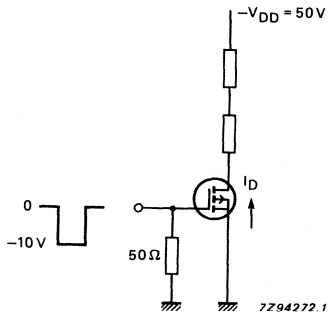


Fig.2 Switching time test circuit.

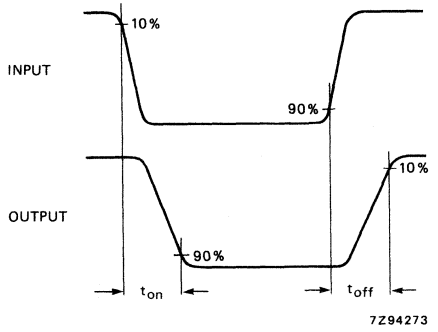


Fig.3 Input and output waveforms.

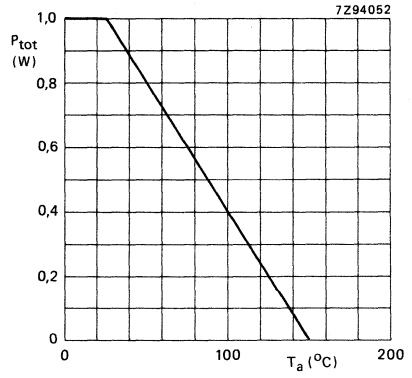


Fig.4 Power derating curve.

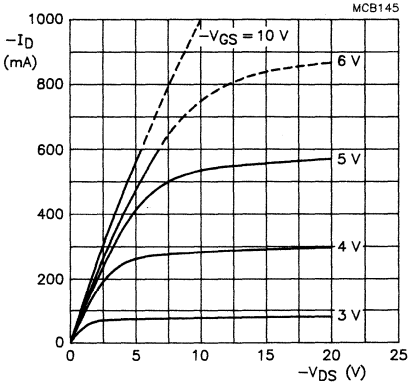


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

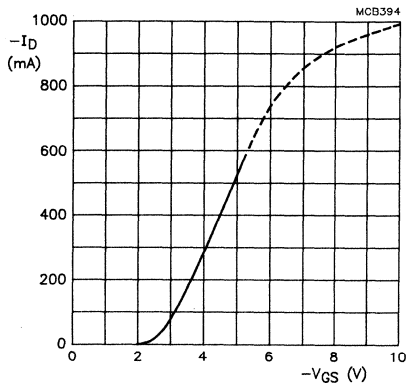


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

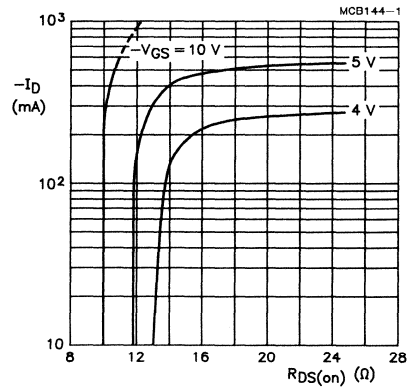


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

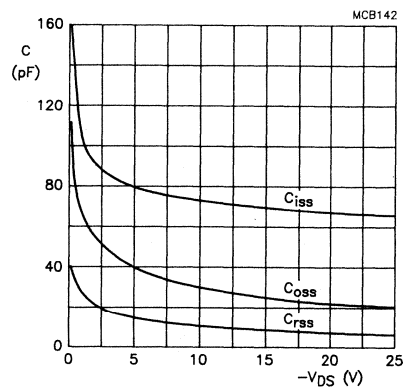


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

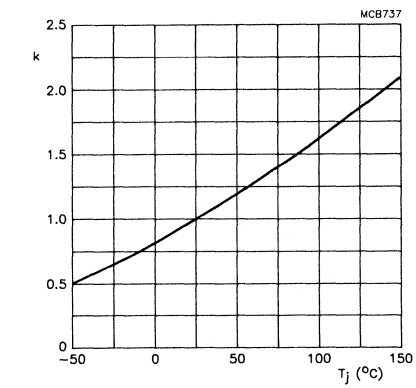


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

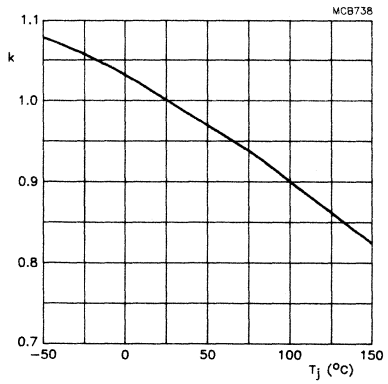


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS(th)}\ at\ 25\ °C}$; typical $-V_{GS(th)}$ at −1 mA.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	275 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	10 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA Dimensions in mm

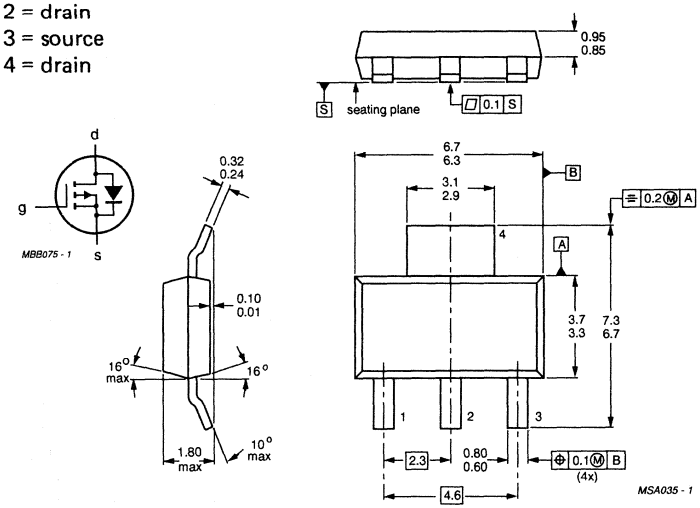
Fig.1 SOT223.

Marking code

BSP205

Pinning:

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	275 mA
Drain current (peak)	$-I_{DM}$	max.	550 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	typ. max.	7.5 Ω 10 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	60 mS 125 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	3 ns 6 ns
	t_{off}	typ. max.	10 ns 15 ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

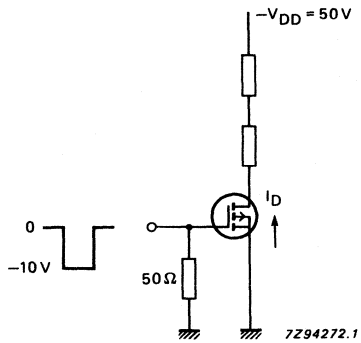


Fig.2 Switching time test circuit.

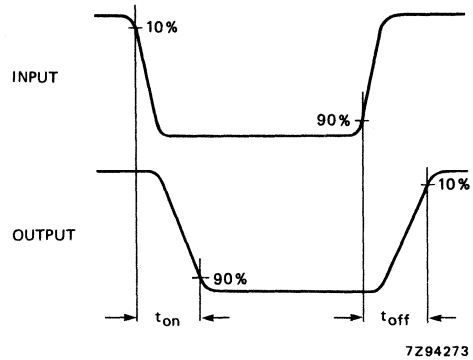


Fig.3 Input and output waveforms.

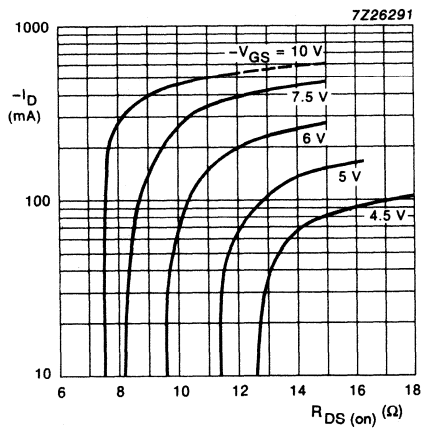


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

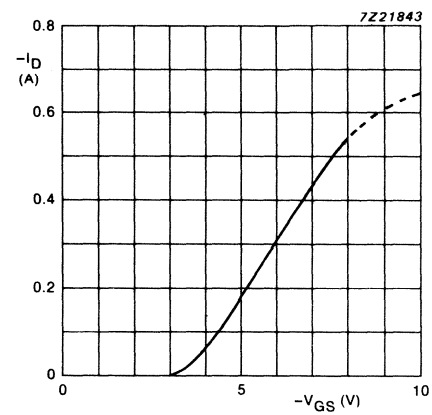


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

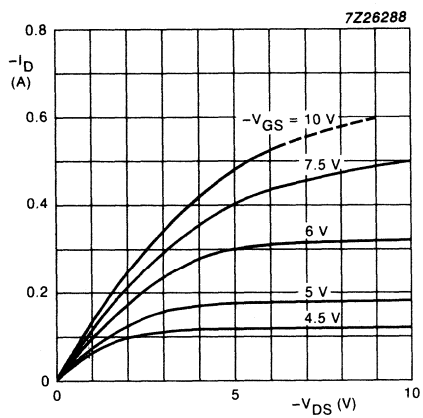


Fig.6 Output characteristics; T_j = 25 °C; typical values.

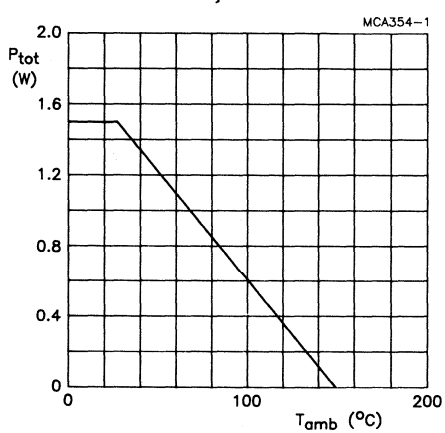


Fig.7 Power derating curve.

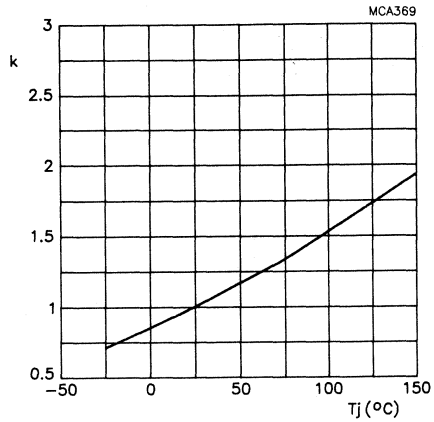


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10 V; typical values.

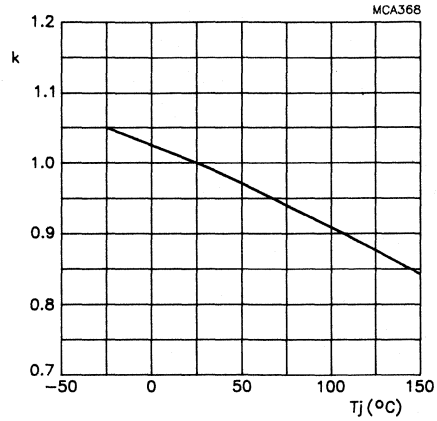


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

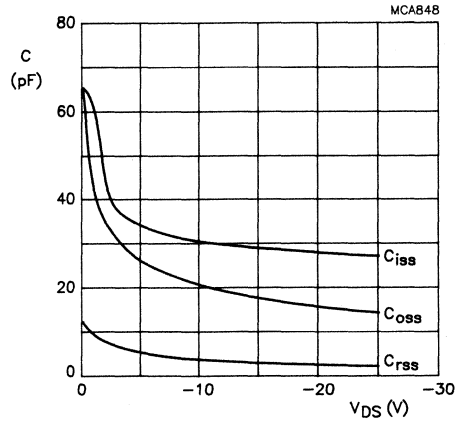


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	6 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA Dimensions in mm

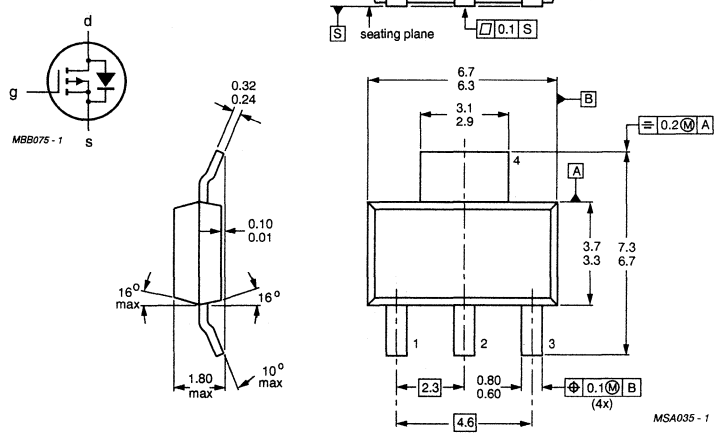
Fig.1 SOT223.

Marking code

BSP206

Pinning:

1 = gate
2 = drain
3 = source
4 = drain



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain current (peak)	$-I_{DM}$	max.	700 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	4 ns 8 ns
	t_{off}	typ. max.	15 ns 25 ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

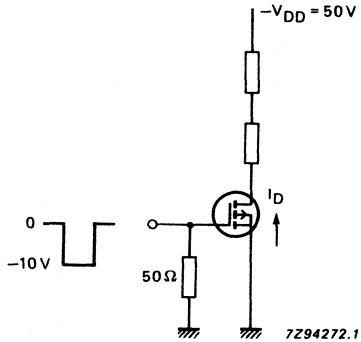


Fig.2 Switching time test circuit.

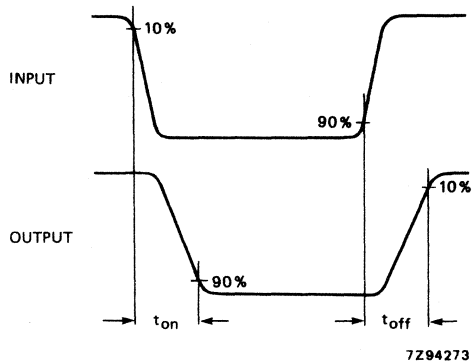


Fig.3 Input and output waveforms.

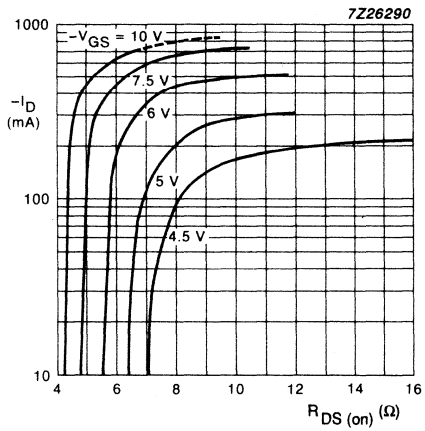


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

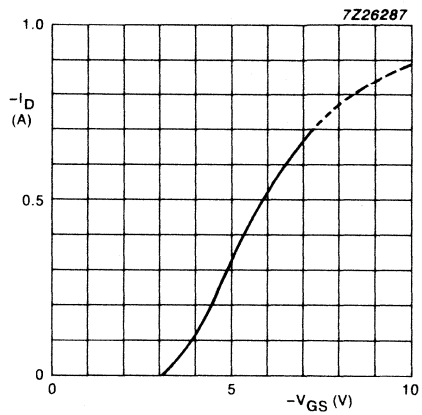


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

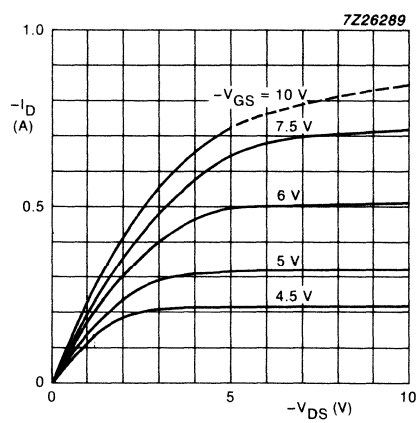


Fig.6 Output characteristics; T_j = 25 °C; typical values.

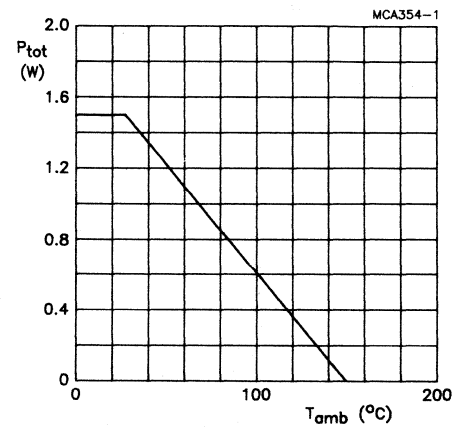


Fig.7 Power derating curve.

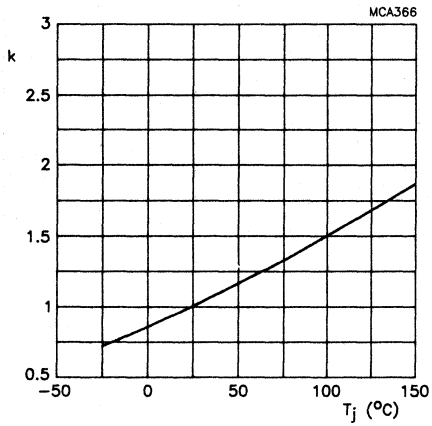


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10V; typical values.

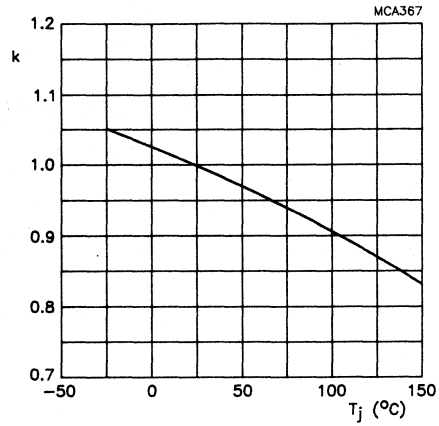


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

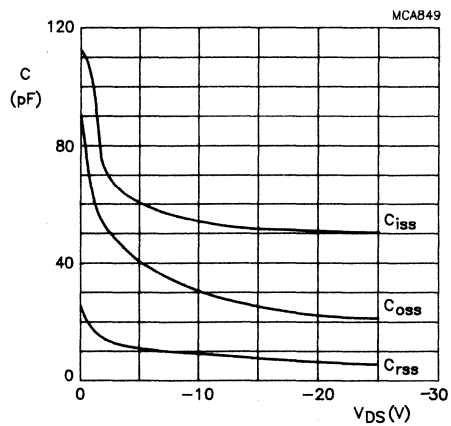


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

BSP220

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

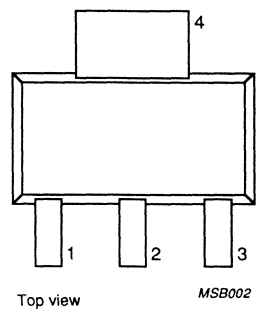
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	12	Ω
$-V_{GS(th)}$	gate-source threshold voltage		2.8	V

PIN CONFIGURATION



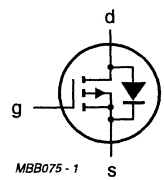


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP220

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP220

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	12	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	20	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP220

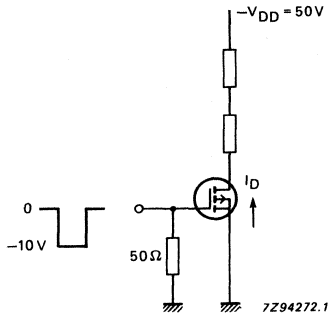


Fig.2 Switching time test circuit.

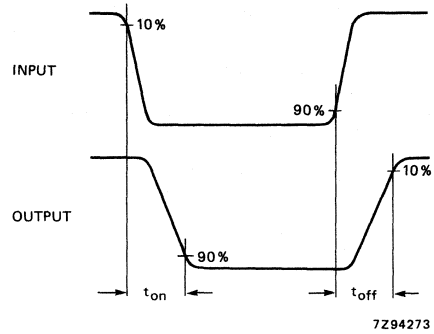


Fig.3 Input and output waveforms.

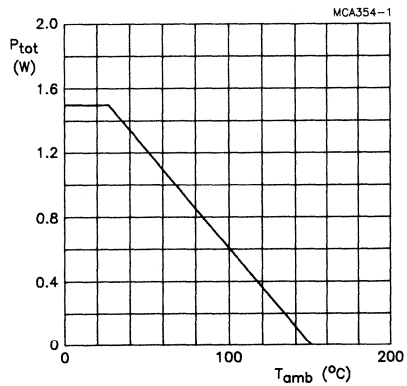


Fig.4 Power derating curve.

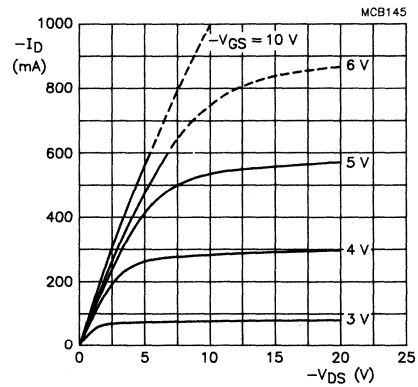


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP220

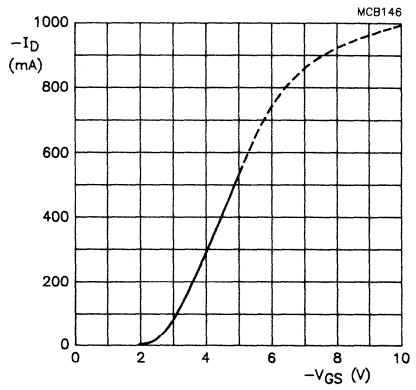


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

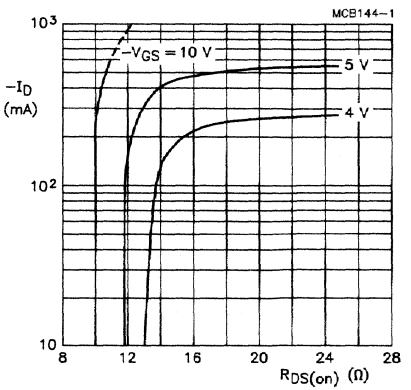


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

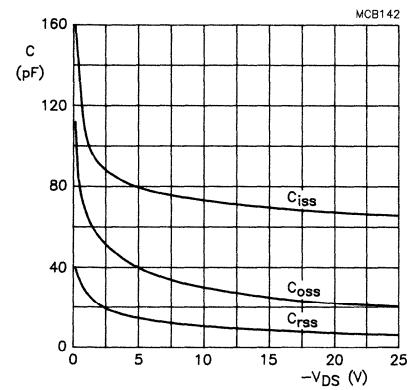


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

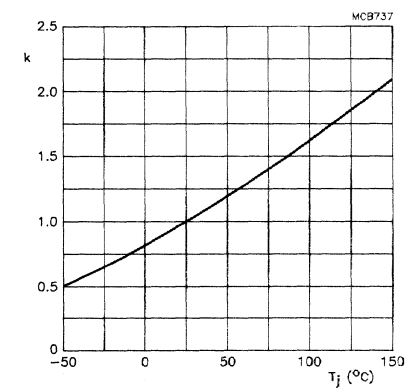


Fig.9 Temperature coefficent of drain-source on-resistance; $k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

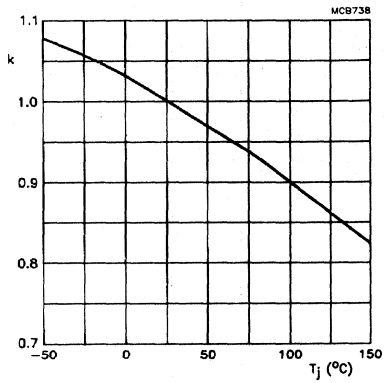


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $-V_{GS(th)}$ at −1 mA.

Data sheet	
status	Product specification
date of issue	April 1995

BSP225
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

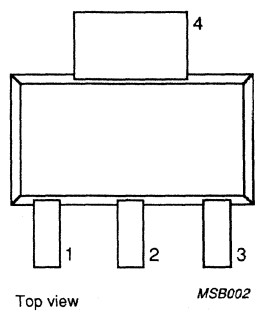


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP225

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP225

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 20 V	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP225

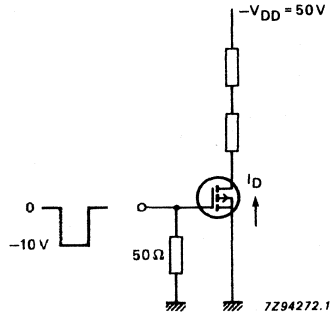


Fig.2 Switching time test circuit.

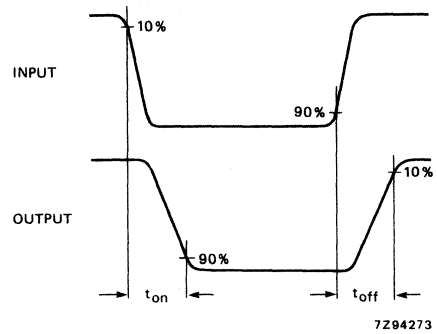


Fig.3 Input and output waveforms.

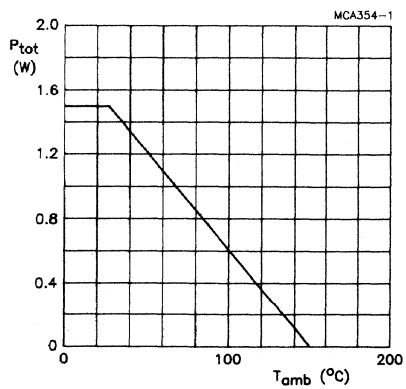


Fig.4 Power derating curve.

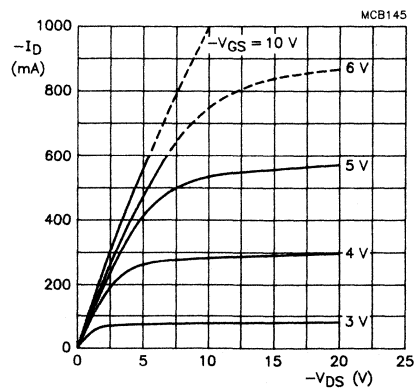


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP225

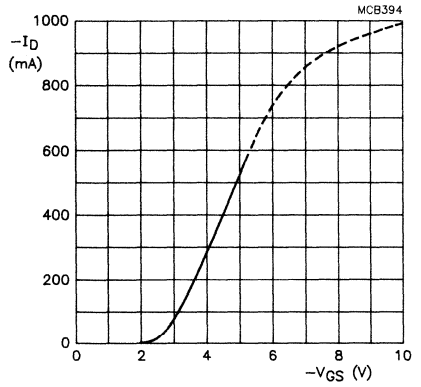


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

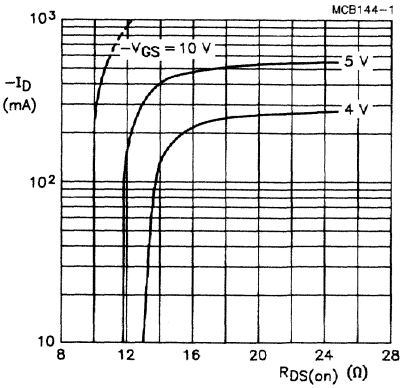


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C; $R_{DS(on)} = f(I_D)$.

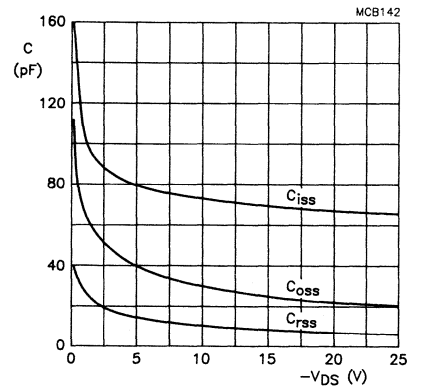


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

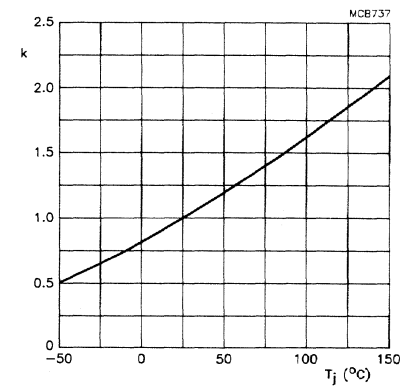


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

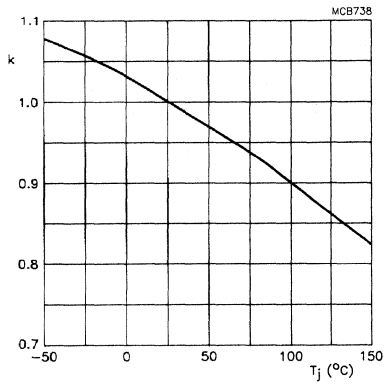


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS\,th}\ at\ 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP230

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

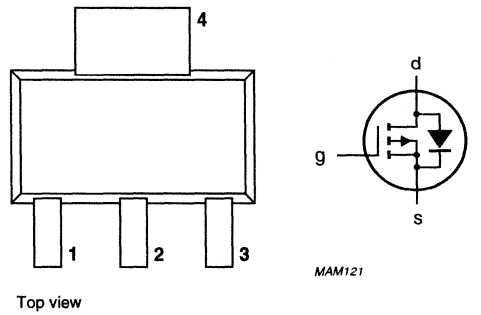


Fig.1 Simplified outline and symbol.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1.7	–2.55	V
I_D	drain current (DC)		–	–210	mA
R_{DSon}	drain-source on-state resistance	I_D = –170 mA; V_{GS} = –10 V	–	17	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W

P-channel enhancement mode vertical D-MOS transistor

BSP230

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–210	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	83.3	K/W

Note to the "Limiting values" and "Thermal characteristics"

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 µA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1.7	–	–2.55	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –170 mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –170 mA	100	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	15	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP230

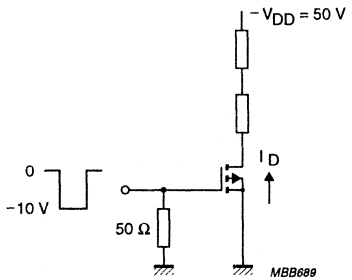


Fig.2 Switching time test circuit.

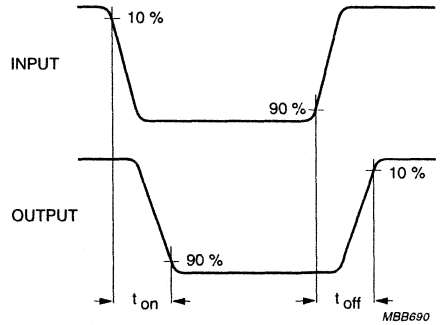


Fig.3 Input and output waveforms.

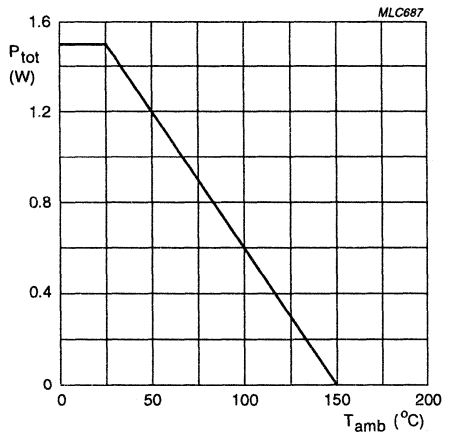
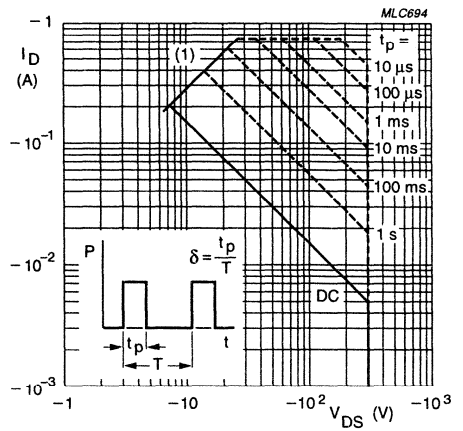


Fig.4 Power derating curve.

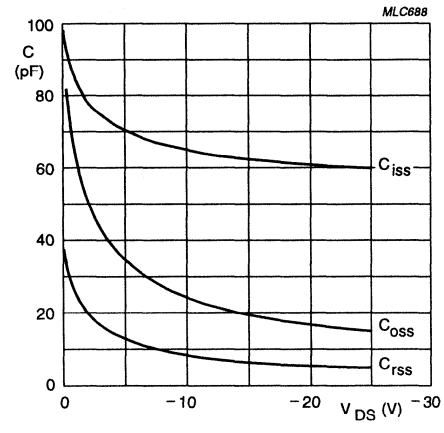


δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

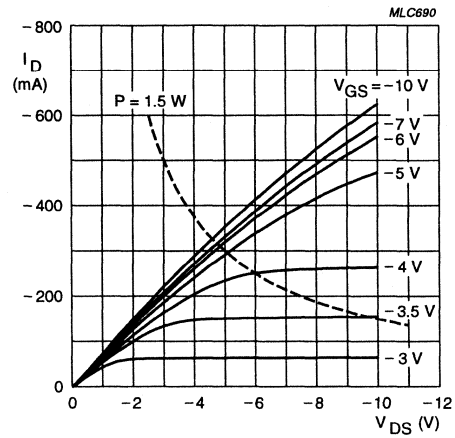
P-channel enhancement mode vertical D-MOS transistor

BSP230



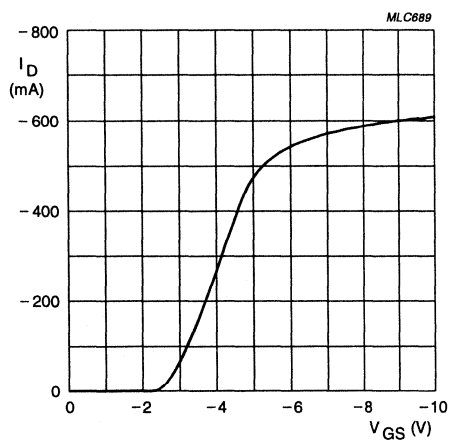
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



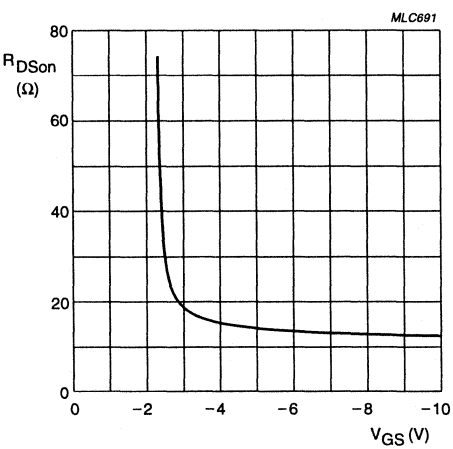
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.

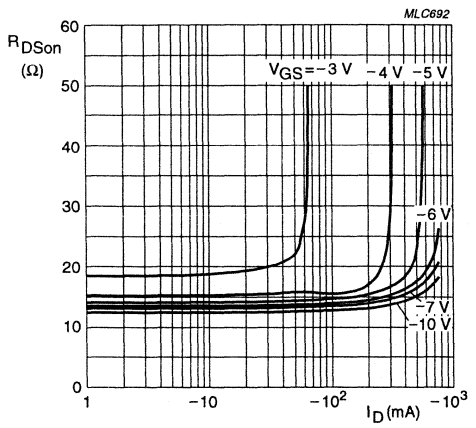


I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.

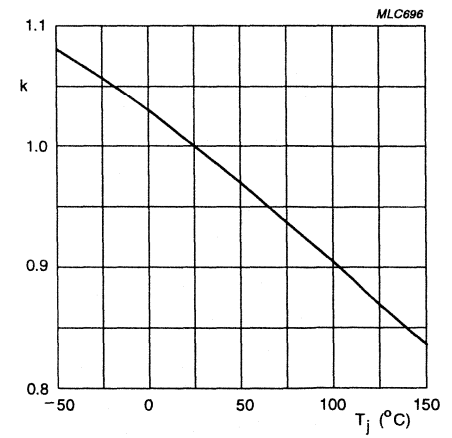
P-channel enhancement mode vertical D-MOS transistor

BSP230



T_j = 25 °C.

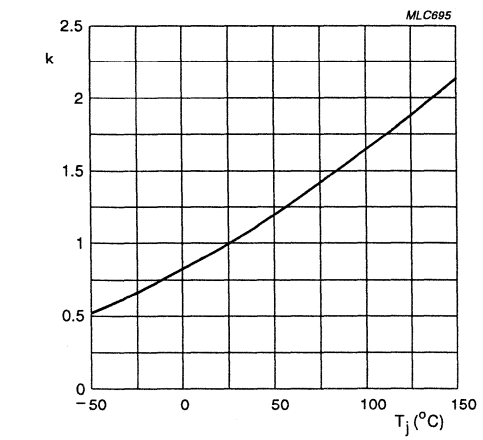
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS}.

Fig.11 Temperature coefficient of gate-source threshold voltage.



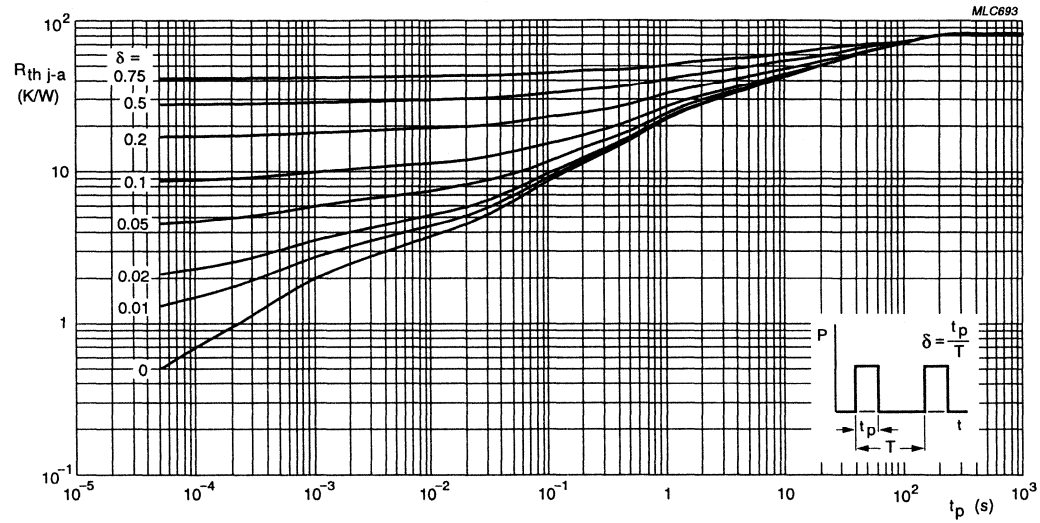
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at I_D = −170 mA; V_{GS} = −10 V.

Fig.12 Temperature coefficient of drain-source on-state resistance.

P-channel enhancement mode vertical D-MOS transistor

BSP230



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP250

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers, power switching, etc.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

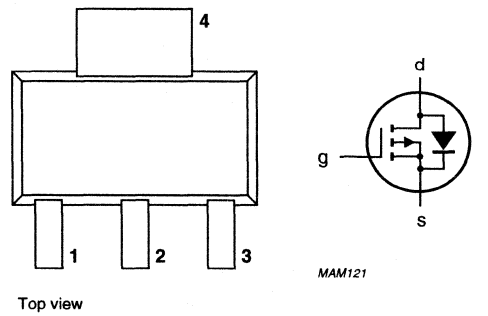


Fig.1 Simplified outline and symbol.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.65	W

P-channel enhancement mode vertical D-MOS transistor

BSP250

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100°C$	–	–3	A
I_{DM}	peak drain current	note 1	–	–12	A
P_{tot}	total power dissipation	up to T_s = 100 °C	–	5	W
		up to T_{amb} = 25 °C; note 2	–	1.65	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100°C$	–	–1.5	A
I_{SM}	peak pulsed source current	note 1	–	–6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

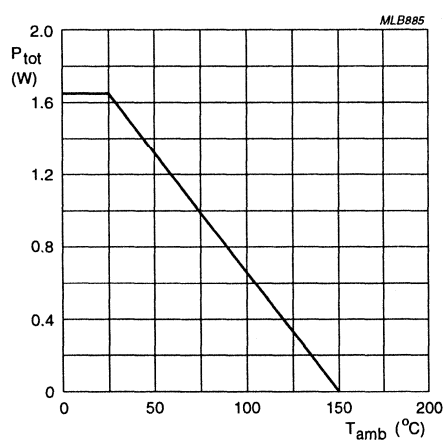
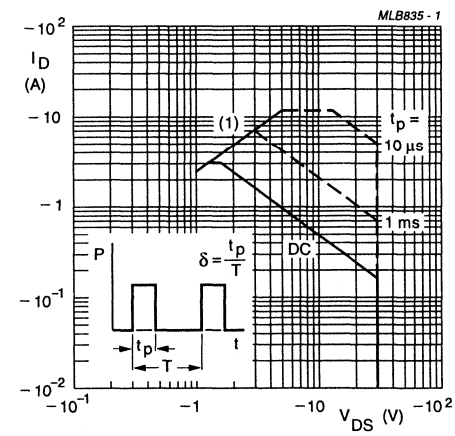


Fig.2 Power derating curve.



δ = 0.01.
Solder point temperature T_s = 100 °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR.

P-channel enhancement mode vertical D-MOS transistor

BSP250

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

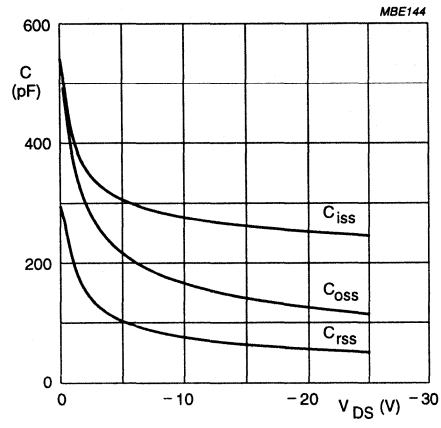
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GS} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns

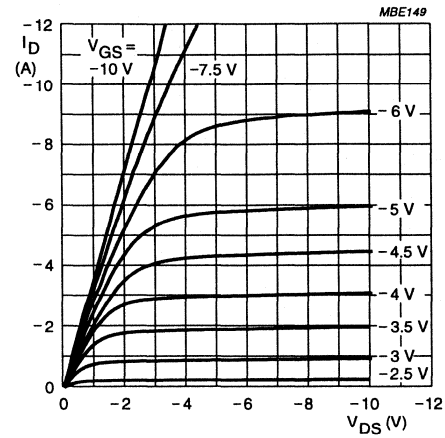
P-channel enhancement mode vertical D-MOS transistor

BSP250



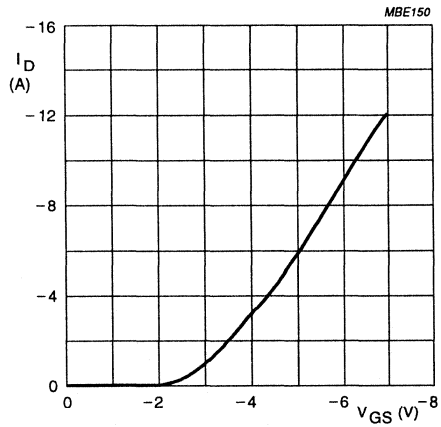
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain source voltage; typical values.



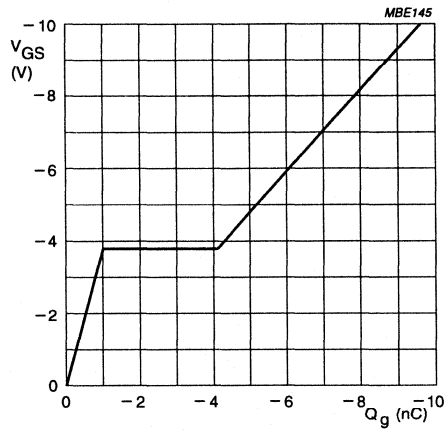
T_j = 25 °C.

Fig.5 Typical output characteristics.



V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Transfer characteristics, typical values.

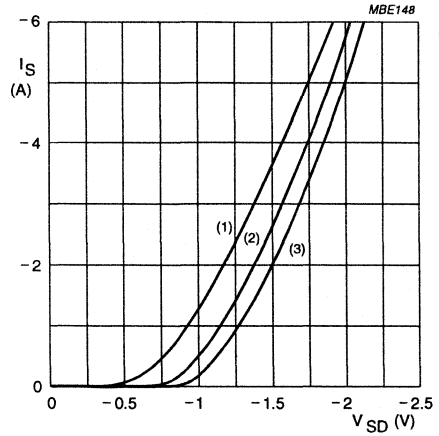


V_{DD} = −15 V.
I_D = −3 A.

Fig.7 Gate-source voltage as a function of total gate charge.

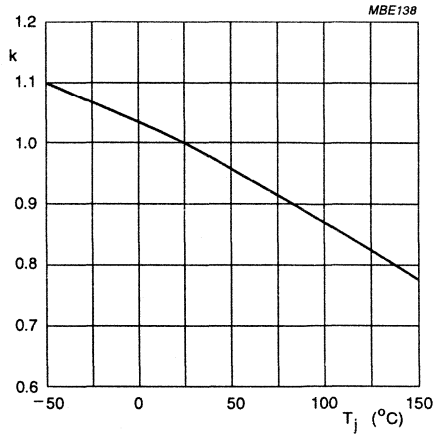
P-channel enhancement mode vertical D-MOS transistor

BSP250



$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

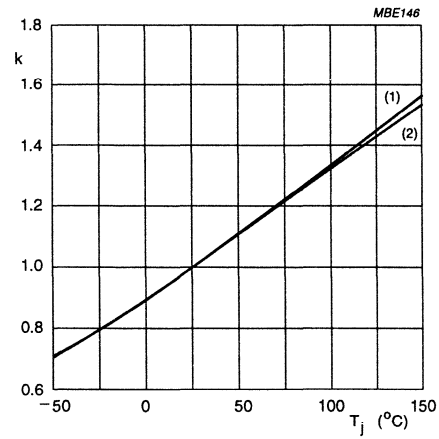
Fig.8 Source current as a function of source-drain diode forward voltage.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = -1$ mA; $V_{DS} = V_{GS} = V_{th}$.

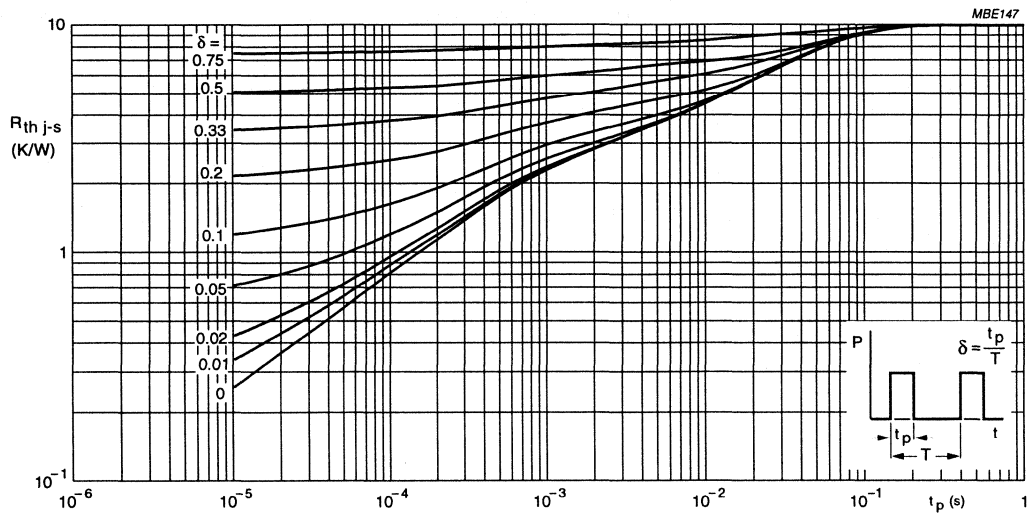
Fig.9 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) $I_D = -1$ A; $V_{GS} = -10$ V.
(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.10 Temperature coefficient of drain-source on-resistance.



Solder point temperature T_s = 100 °C.

Fig.11 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP254; BSP254A

FEATURES

- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant BSP254

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant BSP254A

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	–250	V
V_{GSO}	gate-source voltage	open drain	–	–	±20	V
$\lvert y_{fs} \rvert$	forward transfer admittance	ID = –200 mA; V_{DS} = –25 V	100	200	–	mS
I_D	drain current (DC)		–	–	–0.2	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	15	Ω
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	–	1	W

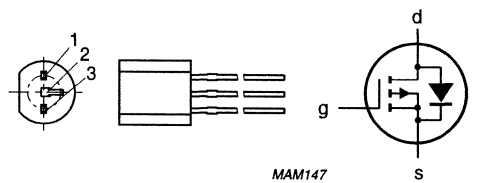


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
$-I_D$	drain current	DC	-	0.2	A
$-I_{DM}$	drain current	peak value	-	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{thj\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

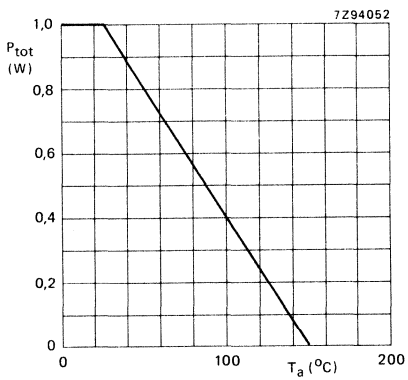


Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	250	-	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	V_{GS} = V_{DS} $-I_D$ = 1 mA	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	-	mS
C_{iss}	input capacitances	note 1	-	65	90	pF
C_{oss}	output capacitance	note 1	-	20	30	pF
C_{rss}	feedback capacitance	note 1	-	6	15	pF
t_{on}	turn-on time	note 2	-	5	10	ns
t_{off}	turn-off time	note 2	-	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

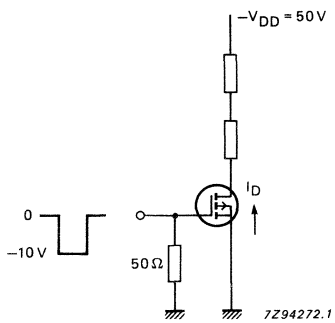


Fig.3 Switching times test circuit.

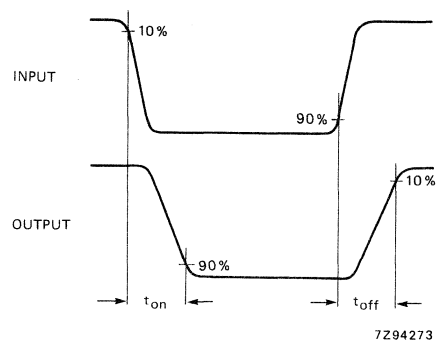


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

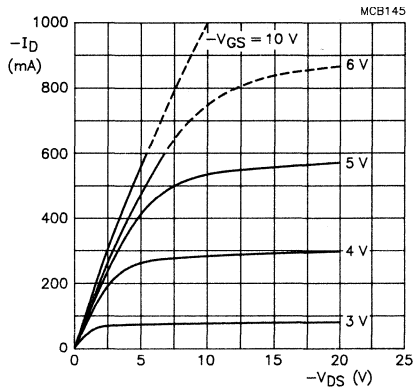


Fig.5 Typical output characteristics; T_j = 25 °C.

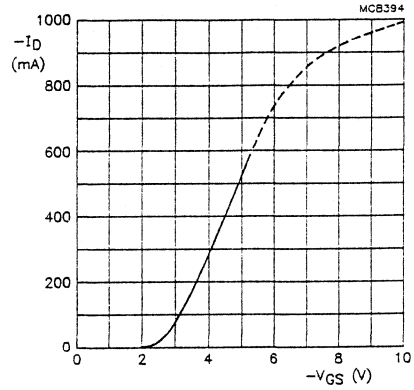


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

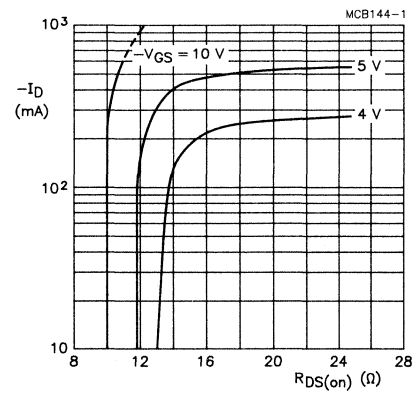


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

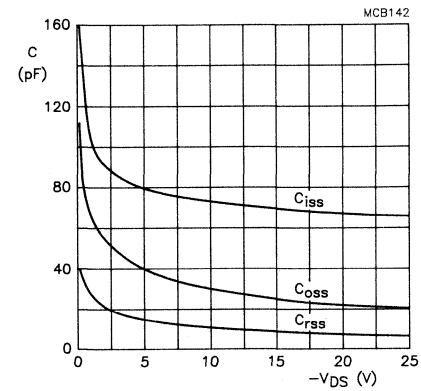


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

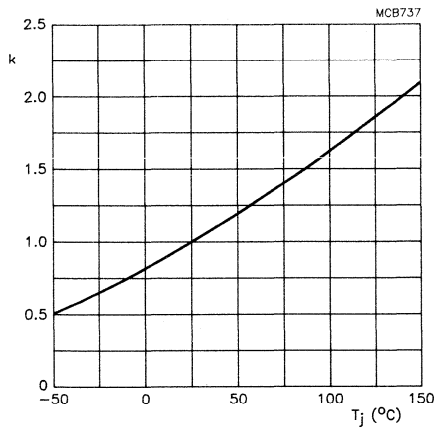


Fig.9 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V;

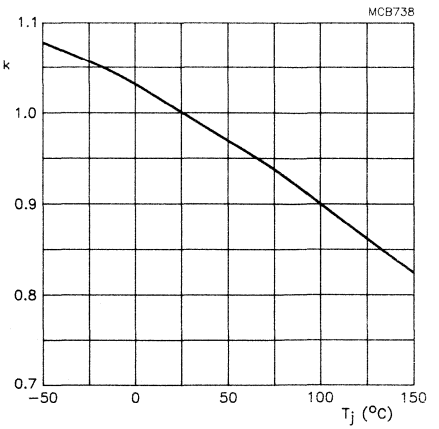


Fig.10 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

FEATURES

- Direct interface to C-MOS, TTL etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
BSP304		
1	g	gate
2	d	drain
3	s	source
BSP304A		
1	s	source
2	g	gate
3	d	drain

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

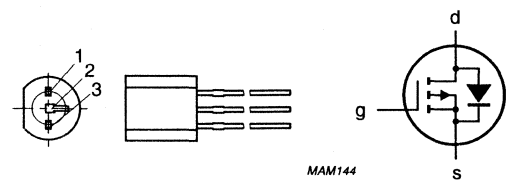


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1.7	–2.55	V
I_D	drain current (DC)		–	–170	mA
R_{DSon}	drain-source on-state resistance	I_D = –170 mA; V_{GS} = –10 V	–	17	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–170	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the "Limiting values" and "Thermal characteristics"

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 µA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1.7	–	–2.55	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –170 mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –170 mA	100	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	15	30	ns

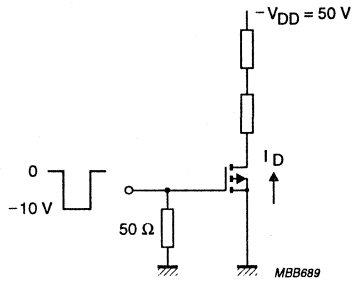


Fig.2 Switching time test circuit.

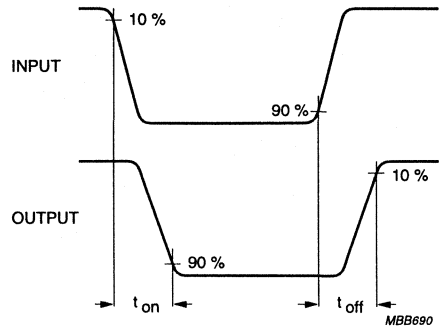


Fig.3 Input and output waveforms.

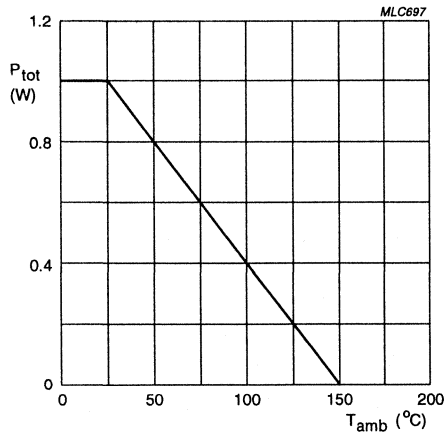
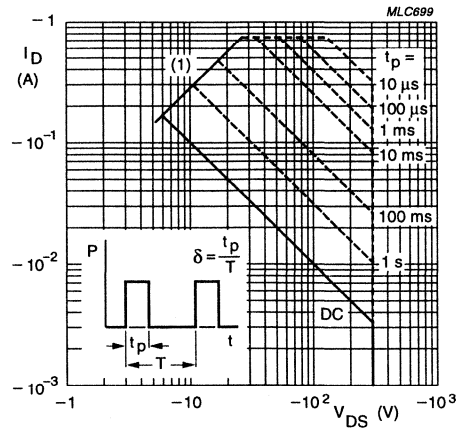
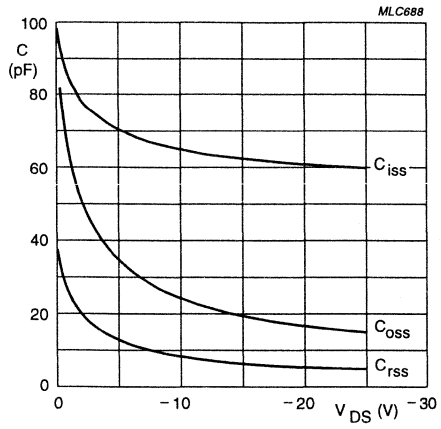


Fig.4 Power derating curve.



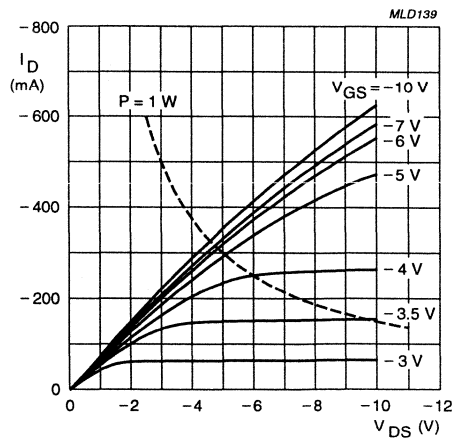
δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



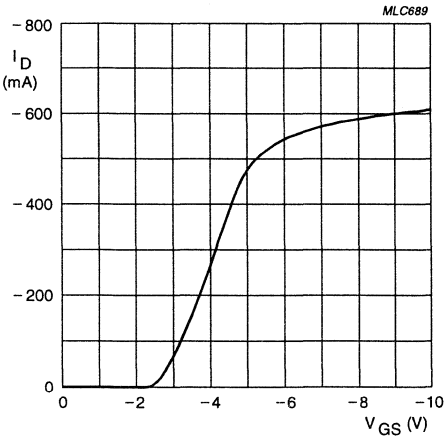
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



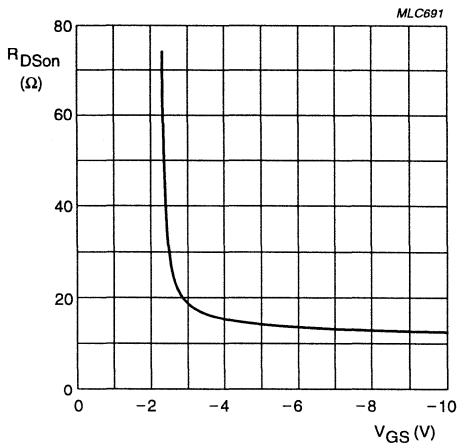
T_j = 25 °C.

Fig.7 Typical output characteristics.



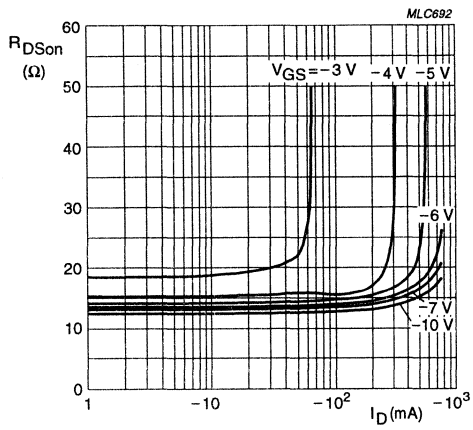
V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



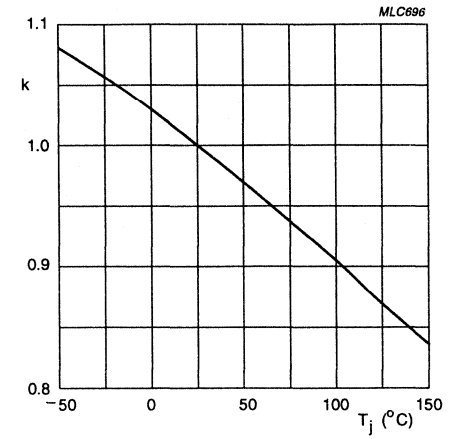
I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C.

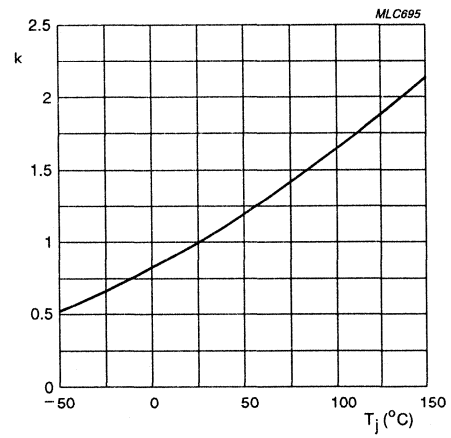
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS}.

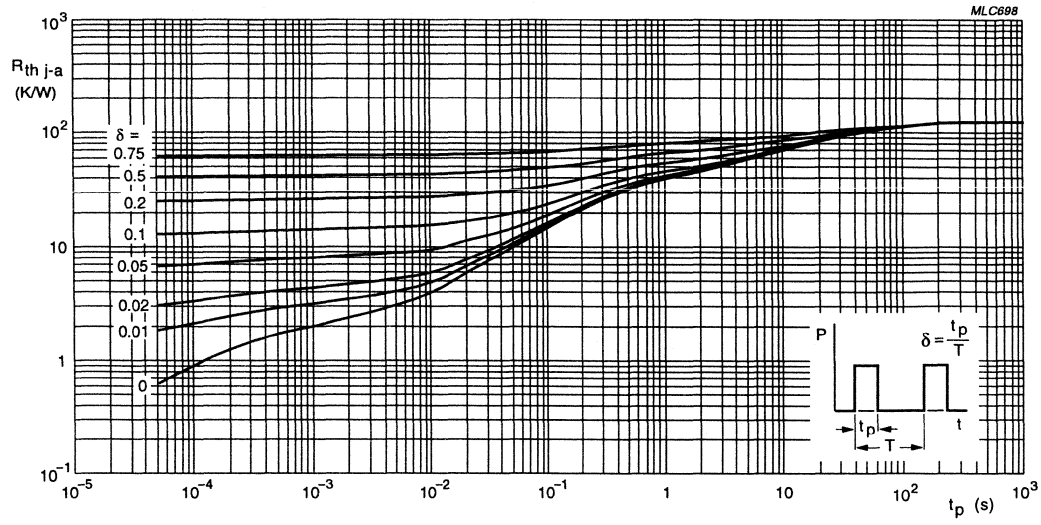
Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at I_D = −170 mA; V_{GS} = −10 V.

Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

N-CHANNEL FETS

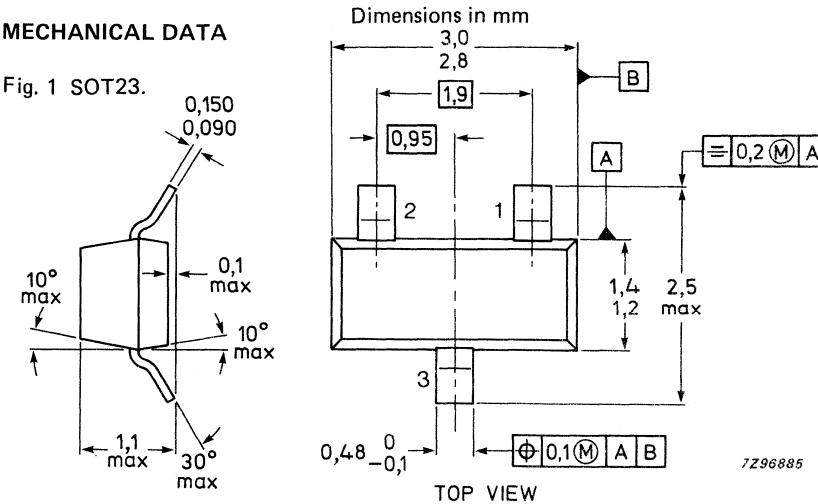
Symmetrical silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

QUICK REFERENCE DATA

			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	250	250	mW
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source cut-off voltage						
V_{DS} = 15 V; I_D = 0.5 nA	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rs}	<	5	5	5	pF
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 20 mA; $-V_{GSM}$ = 10 V	t_{off}	<	25	–	–	ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	t_{off}	<	–	50	–	ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	t_{off}	<	–	–	100	ns

MECHANICAL DATA

Fig. 1 SOT23.

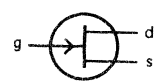


Marking code

BSR56 = M4p
BSR57 = M5p
BSR58 = M6p

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Forward gate current	I_{GF}	max.	50	mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source cut-off current					
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	max.	1.0		nA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	max.	1.0		nA

			BSR56	BSR57	BSR58	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	750	–	–	mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	500	–	mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0; T_a = 25 °C	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rss}	<	5	5	5	pF

Notes

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

			BSR56	BSR57	BSR58	
Switching times						
V_{DD} = 10 V; V_{GS} = 0						
Conditions I_D and $-V_{GSM}$	I_D	=	20	10	5	mA
	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

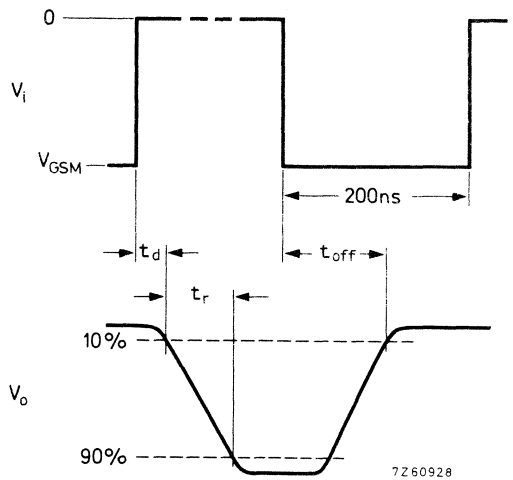


Fig. 2 Switching times waveforms.

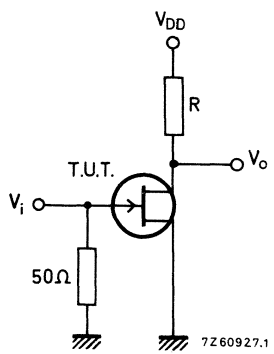


Fig. 3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leqslant 1$ ns
$\delta = 0.02$
$Z_o = 50\ \Omega$

Oscilloscope

$t_r \leqslant 0.75$ ns
$R_i \geqslant 1\ M\Omega$
$C_i \leqslant 2.5$ pF

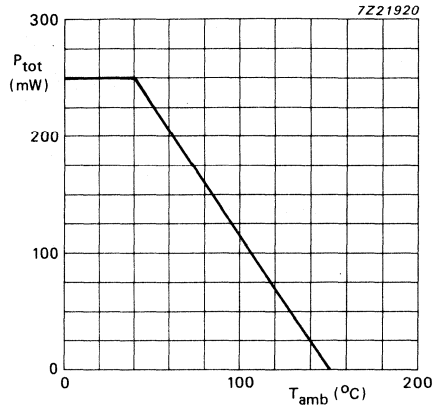


Fig.4 Power derating curve.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver

QUICK REFERENCE DATA

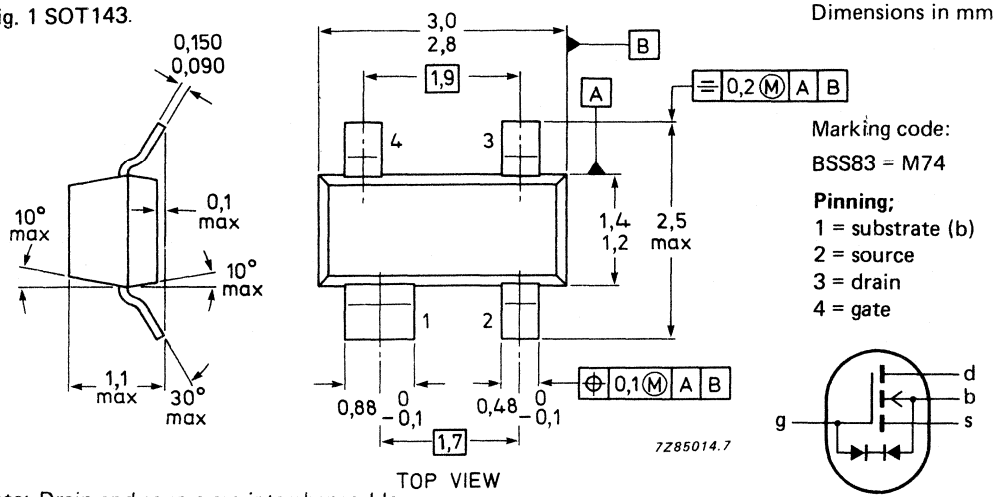
Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230 mW
Gate-source threshold voltage			
$V_{DS} = V_{GS}$; $V_{SB} = 0$;	$V_{GS(th)}$	>	0.1 V
$I_D = 1\ \mu A$		<	2.0 V
Drain-source ON-resistance			
V_{GS} = 10 V; V_{SB} = 0; I_D = 0.1 mA	R_{DSon}	<	45 Ω
Feed-back capacitance			
$V_{GS} = V_{BS} = -15$ V;			
V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6 pF

MECHANICAL DATA

SOT143 (see Fig. 1).

See also *Soldering recommendations*.

Fig. 1 SOT143.



Dimensions in mm

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

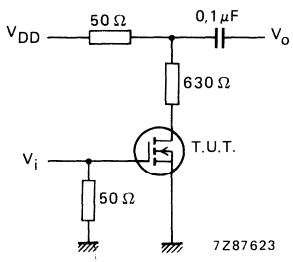
T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_D = 10 nA	$V_{(BR)DSX}$	>	10 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10 V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15 V
Source-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open drain	$V_{(BR)SBO}$	>	15 V
Drain-source leakage current $V_{GS} = V_{BS} = -2$ V; V_{DS} = 6,6 V	I_{DSoff}	<	10 nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Source-drain leakage current $V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6{,}6$ V	I_{SDoff}	<	10 nA
Forward transconductance at f = 1 kHz $V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	> typ.	10 mS 15 mS
Gate-source threshold voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu$A	$V_{GS(th)}$	> <	0,1 V 2,0 V
Drain-source ON-resistance $I_D = 0{,}1$ mA;			
$V_{GS} = 5$ V; $V_{SB} = 0$	R_{DSon}	<	70 Ω
$V_{GS} = 10$ V; $V_{SB} = 0$	R_{DSon}	<	45 Ω
$V_{GS} = 3{,}2$ V; $V_{SB} = 6{,}8$ V (see Fig. 4)	R_{DSon}	typ. <	80 Ω 120 Ω
Gate-substrate zener voltages			
$V_{DB} = V_{SB} = 0$; $-I_G = 10\ \mu$A	$V_{Z(1)}$	>	12,5 V
$V_{DB} = V_{SB} = 0$; $+I_G = 10\ \mu$A	$V_{Z(2)}$	>	12,5 V
Capacitances at f = 1 MHz $V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 2) $V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

Pulse generator:
$R_i = 50\ \Omega$
$t_r < 0{,}5$ ns
$t_f < 1{,}0$ ns
$t_p = 20$ ns
$\delta < 0{,}01$



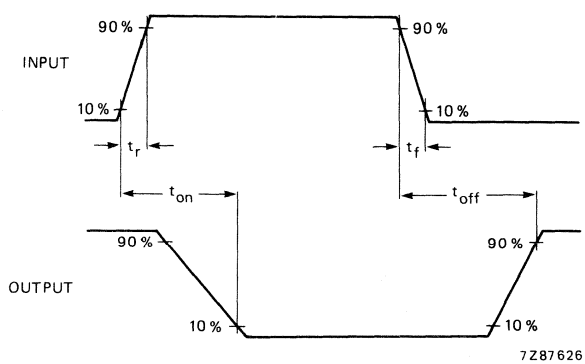


Fig. 2 Switching times test circuit and input and output waveforms.

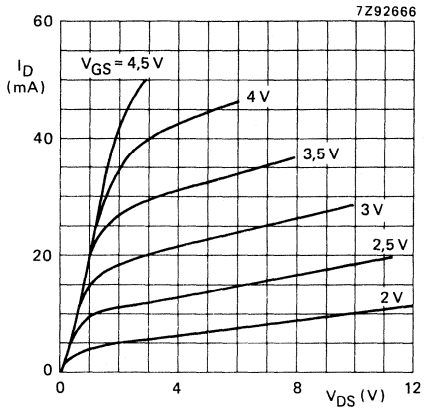


Fig. 3 V_{SB} = 0; typical values.

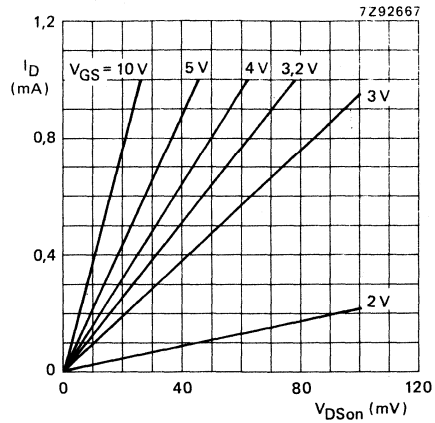


Fig. 4 V_{SB} = 6,8 V; typical values.

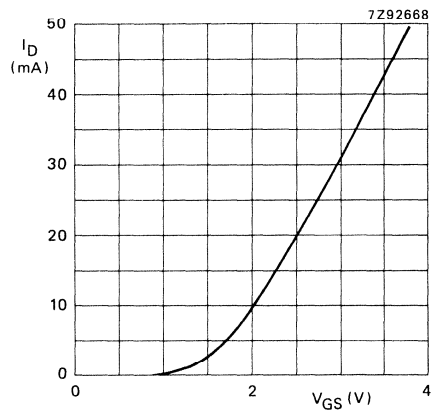


Fig. 5 V_{DS} = 10 V; V_{BS} = 0; typical values.

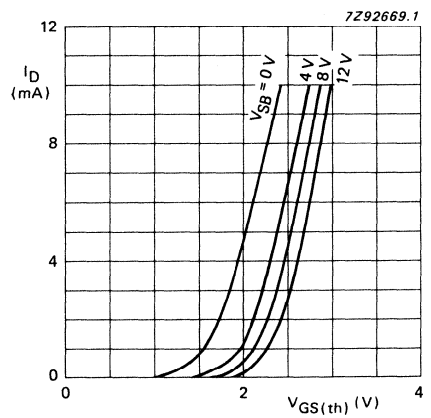


Fig. 6 $V_{DS} = V_{GS} = V_{GS(th)}$.

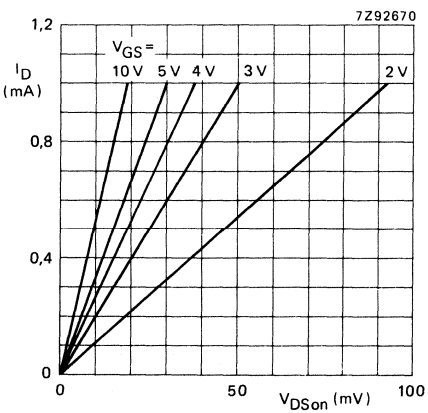


Fig. 7 V_{SB} = 0; typical values.

Conditions for Figs 3, 4, 5, 6 and 7:
T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSS84

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

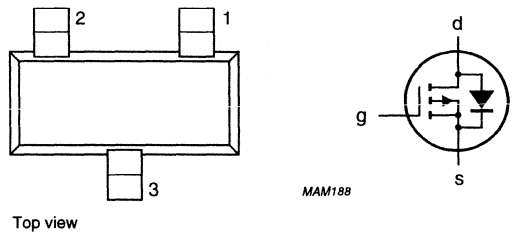


Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.8	–2	V
I_D	drain current (DC)		–	–130	mA
R_{DSon}	drain-source on-state resistance	I_D = –130 mA; V_{GS} = –10 V	–	10	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW

P-channel enhancement mode vertical D-MOS transistor

BSS84

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–130	mA
I_{DM}	peak drain current		–	–520	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	500	K/W

Note to the "Limiting values" and "Thermal characteristics"

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –40 V	–	–	–100	nA
		V_{GS} = 0; V_{DS} = –50 V	–	–	–10	μA
		V_{GS} = 0; V_{DS} = –50 V; T_j = 125 °C	–	–	–60	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –130 mA	–	–	10	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –130 mA	50	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	25	45	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	25	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	3.5	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –40 V; I_D = –200 mA	–	3	–	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –40 V; I_D = –200 mA	–	7	–	ns

P-channel enhancement mode vertical D-MOS transistor

BSS84

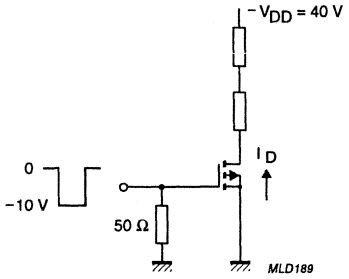


Fig.2 Switching time test circuit.

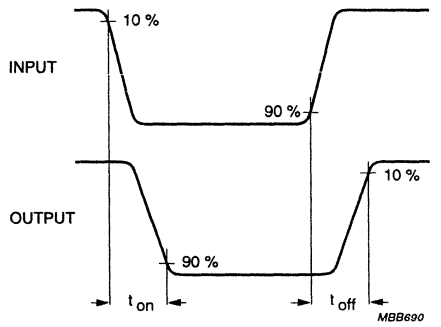


Fig.3 Input and output waveforms.

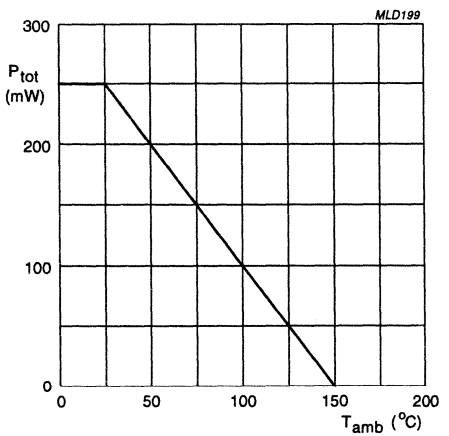
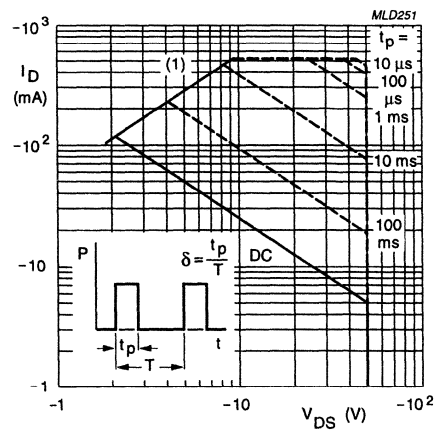


Fig.4 Power derating curve.

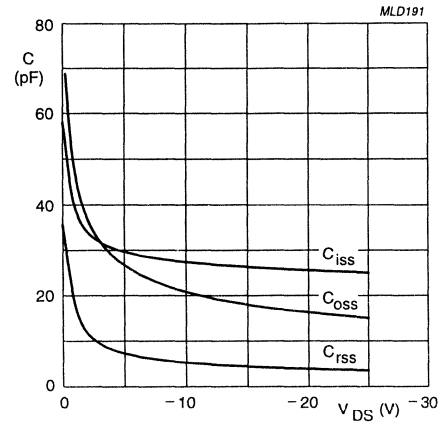


δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

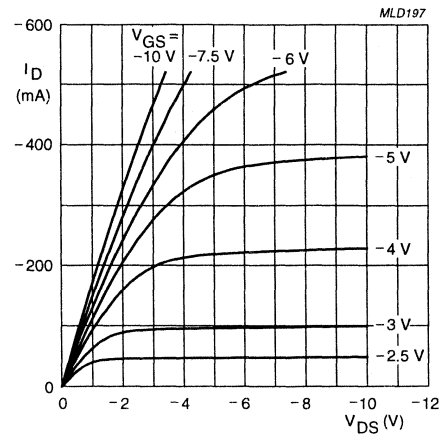
P-channel enhancement mode vertical D-MOS transistor

BSS84



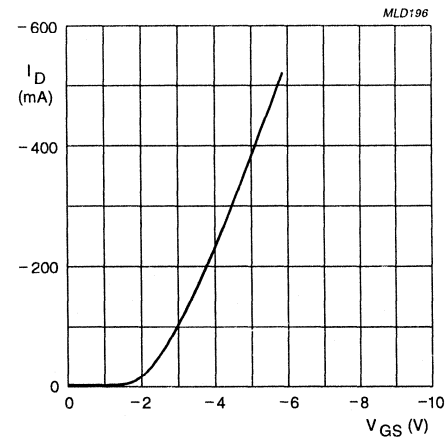
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



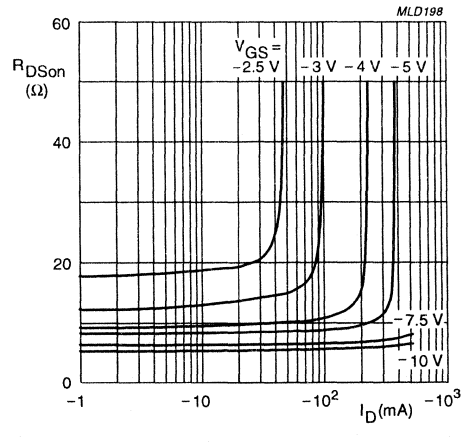
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = −10 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.

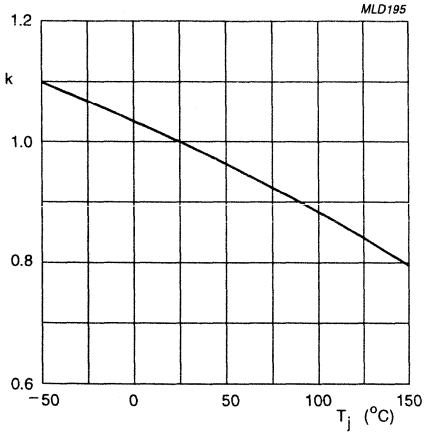


T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of drain current; typical values.

P-channel enhancement mode vertical D-MOS transistor

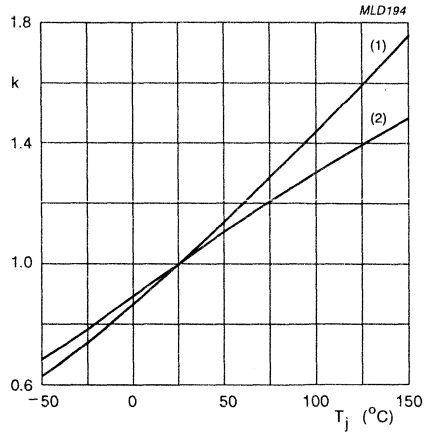
BSS84



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

$I_D = -1$ mA; $V_{DS} = V_{GS}$.

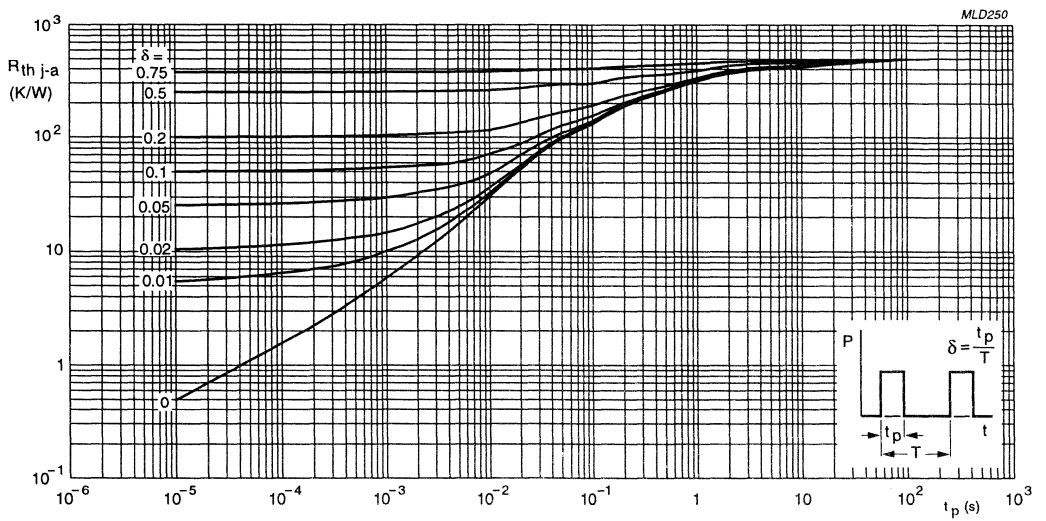
Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) $I_D = -130$ mA; $V_{GS} = -10$ V.
(2) $I_D = -20$ mA; $V_{GS} = -2.4$ V.

Fig.11 Temperature coefficient of drain-source on-state resistance.



$T_{amb} = 25$ °C.

Fig.12 Thermal resistance from junction to ambient as a function of pulse time; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in a SOT89 envelope.
Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	280 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS\ (on)}$	max. typ.	6 Ω 4.5 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ. min.	350 mS 140 mS

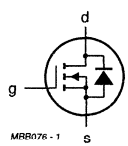
MECHANICAL DATA

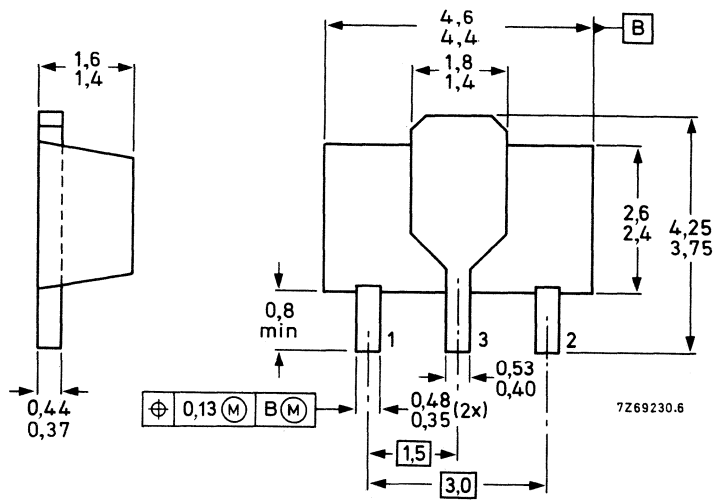
Dimensions in mm

Fig. 1 SOT89.

Pinning

1 = source
2 = gate
3 = drain





marking: KA

BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	280 mA
Drain current (peak)	I_{DM}	max.	1.1 A
Total power dissipation up to T_{amb} = 25 °C *	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient *	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	60 μA
		typ.	100 nA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8 V
		max.	2.8 V
Drain-source on-resistance			
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6 Ω
		typ.	4.5 Ω
Transfer admittance			
I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ.	350 mS
		min.	140 mS
Input capacitance f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	60 pF
		typ.	45 pF
Output capacitance f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	25 pF
		typ.	15 pF
Feedback capacitance f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	10 pF
		typ.	3.5 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V;	t_{on}	typ.	5 ns
		max.	10 ns
V_{GS} = 0 to 10	t_{off}	typ.	15 ns
		max.	25 ns

* Transistor mounted on ceramic substrate area 2.5 cm^2, thickness 0.7 mm.

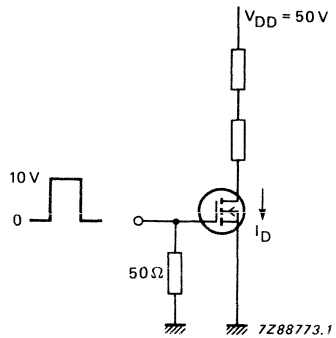


Fig. 2 Switching times test circuit.

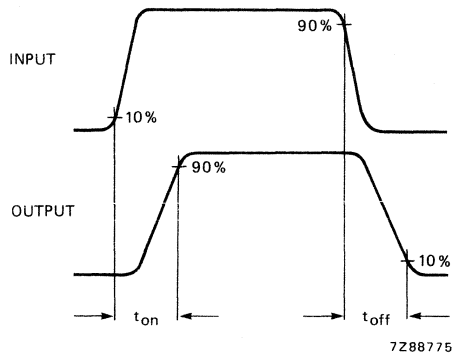


Fig. 3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS88

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	230	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.2	V

Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	230	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

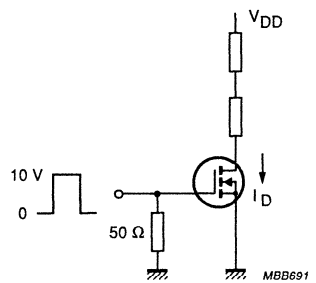
N-channel enhancement mode vertical D-MOS transistor

BSS88

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	230	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0	–	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 14 mA; V_{GS} = 1.8 V	–	6	15	Ω
		I_D = 150 mA; V_{GS} = 5 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 150 mA; V_{DS} = 25 V	140	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

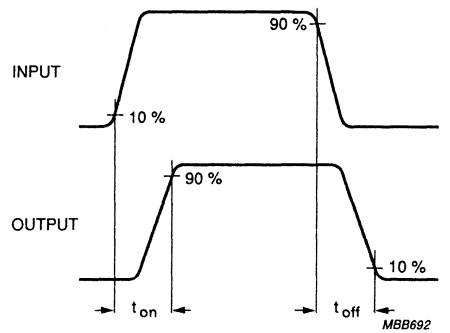


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

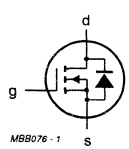
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	140 mS 350 mS

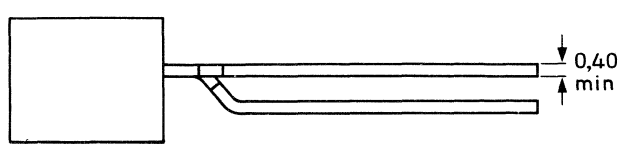
MECHANICAL DATA

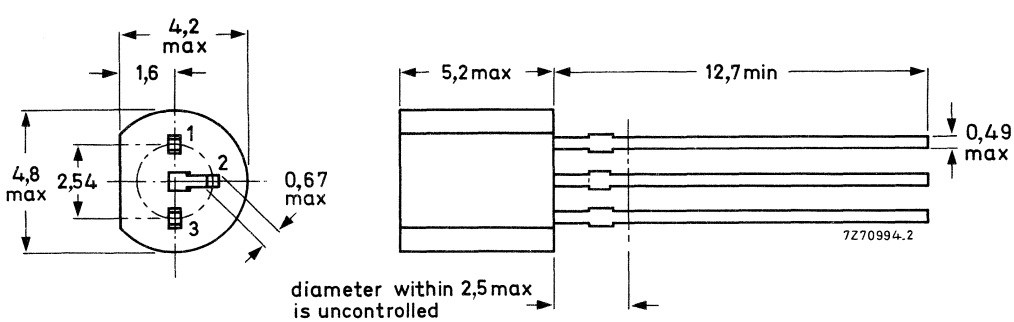
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = gate
2 = drain
3 = source







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ. max.	100 nA 60 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 ns 15 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

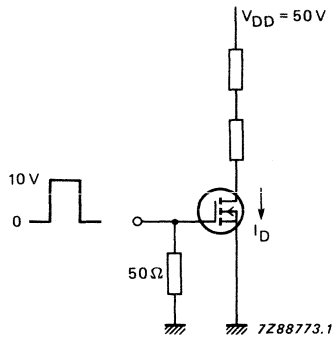


Fig. 2 Switching time test circuit.

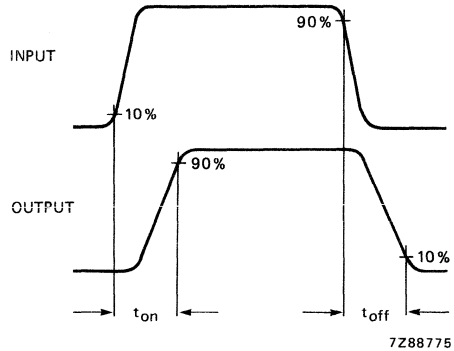


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-18 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	140 mS 350 mS

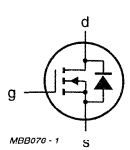
MECHANICAL DATA

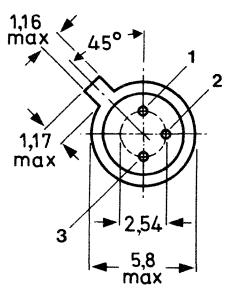
Dimensions in mm

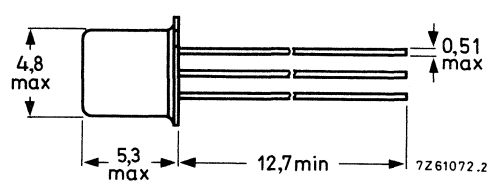
Fig. 1 TO-18.

Pinning

1 = source
2 = gate
3 = drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.4 A
Total power dissipation up to			
T_{amb} = 25 °C	P_{tot}	max.	0.4 W
T_{case} = 25 °C	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−55 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	310 K/W
From junction to case	$R_{th\ j\text{-}c}$	=	83 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ.	100 nA
		max.	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage	$V_{GS(th)}$	min.	0.8 V
I_D = 1 mA; V_{DS} = V_{GS}		max.	2.8 V
Drain-source ON-resistance	R_{DSon}	typ.	4.5 Ω
I_D = 400 mA; V_{GS} = 10 V		max.	6.0 Ω
Transfer admittance	$\lvert y_{fs} \rvert$	min.	140 mS
I_D = 400 mA; V_{DS} = 25 V		typ.	350 mS
Input capacitance at f = 1 MHz;	C_{iss}	typ.	45 pF
V_{DS} = 25 V; V_{GS} = 0		max.	60 pF
Output capacitance at f = 1 MHz;	C_{oss}	typ.	15 pF
V_{DS} = 25 V; V_{GS} = 0		max.	25 pF
Feedback capacitance at f = 1 MHz;	C_{rss}	typ.	3.5 pF
V_{DS} = 25 V; V_{GS} = 0		max.	10 pF
Switching times (see Figs 2 and 3)			
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	15 ns
	t_{off}	typ.	15 ns
		max.	25 ns

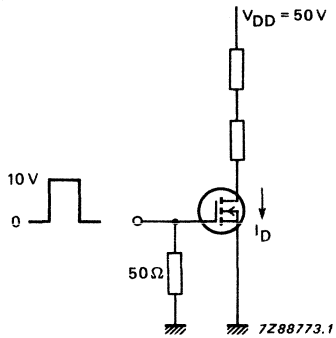


Fig. 2 Switching time test circuit.

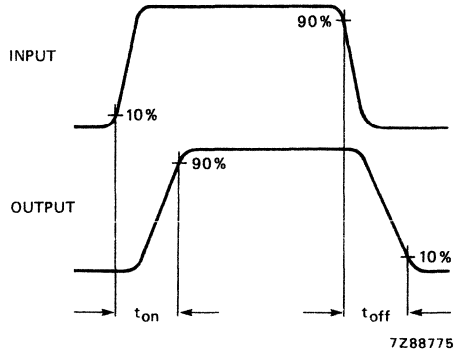


Fig. 3 Input and output waveforms.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

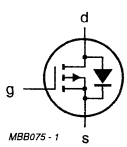
Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 20 Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\|y_{fs}\|$	min. typ.	60 mS 200 mS

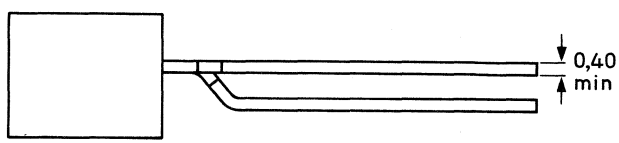
MECHANICAL DATA

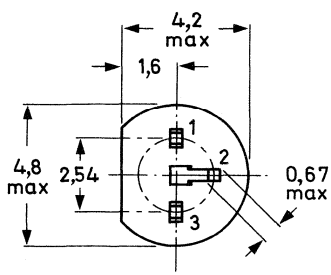
Dimensions in mm

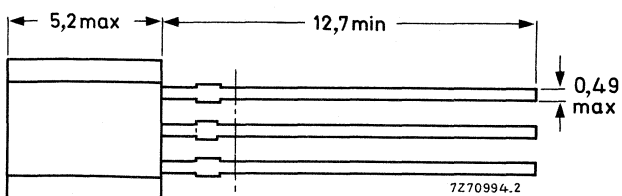
Fig. 1 TO-92 variant.

Pinning
1 = gate
2 = drain
3 = source









diameter within 2,5 max is uncontrolled

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.15	A
Drain current (peak)	$-I_{DM}$	max.	0.6	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 250 μA; $-V_{GS}$ = 0	$-V_{(BR)DS}$	min.	200	V
Drain-source leakage current $-V_{DS}$ = 60 V; $-V_{GS}$ = 0 $-V_{DS}$ = 200 V; $-V_{GS}$ = 0	$-I_{DSS}$ $-I_{DSS}$	max. max.	0.2 60	μA μA
Gate-source leakage current $-V_{GS}$ = 20 V; $-V_{DS}$ = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 20	Ω Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	60 200	mS mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{iss}	typ.	65	pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{oss}	typ.	20	pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{rss}	typ.	6	pF
Switching times (see Figs 2 and 3) $-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 20	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

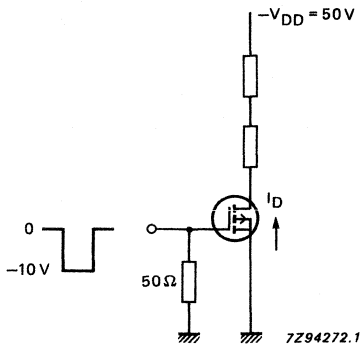


Fig. 2 Switching time test circuit.

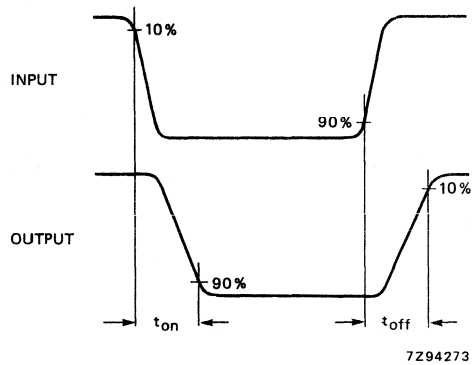


Fig. 3 Input and output waveforms.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

BSS100

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION

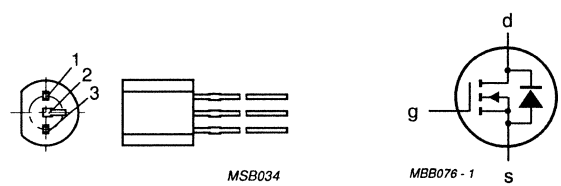


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS100

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	250	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150	K/W

Note

1. Transistor mounted on a printed circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm².

N-channel enhancement mode vertical D-MOS transistor

BSS100

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	40	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	25	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

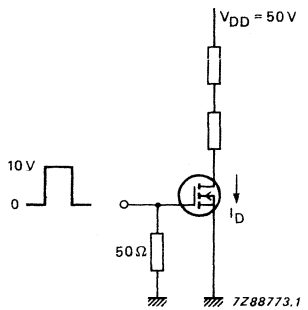


Fig.2 Switching time test circuit.

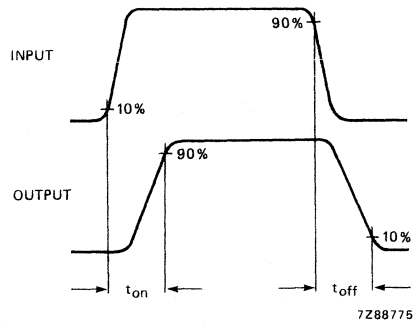


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSS110

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

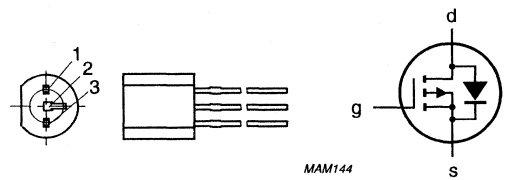


Fig.1 Simplified outline and symbol.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
1	s	source
2	g	gate
3	d	drain

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	−50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = −1 mA; V_{DS} = V_{GS}	−0.8	−2	V
I_D	drain current (DC)		–	−170	mA
R_{DSon}	drain-source on-state resistance	I_D = −170 mA; V_{GS} = −10 V	–	10	Ω
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW

P-channel enhancement mode vertical D-MOS transistor

BSS110

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–170	mA
I_{DM}	peak drain current		–	–520	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	830	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	150	K/W

Note to the "Limiting values" and "Thermal characteristics"

1. Device mounted on a printed-circuit board, maximum lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 µA	–50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –40 V	–	–	–100	nA
		V_{GS} = 0; V_{DS} = –50 V	–	–	–10	µA
		V_{GS} = 0; V_{DS} = –50 V; T_j = 125 °C	–	–	–60	µA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –170 mA	–	–	10	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = –25 V; I_D = –170 mA	50	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	25	45	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	25	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	3.5	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –40 V; I_D = –200 mA	–	3	–	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –40 V; I_D = –200 mA	–	7	–	ns

P-channel enhancement mode vertical D-MOS transistor

BSS110

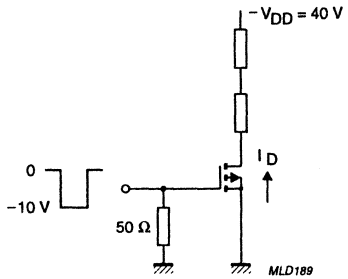


Fig.2 Switching time test circuit.

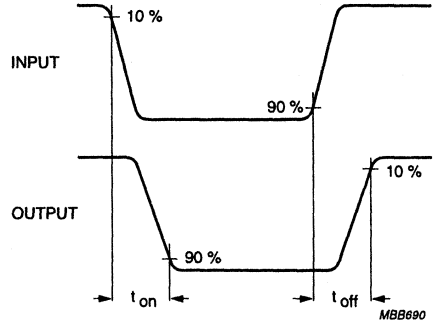


Fig.3 Input and output waveforms.

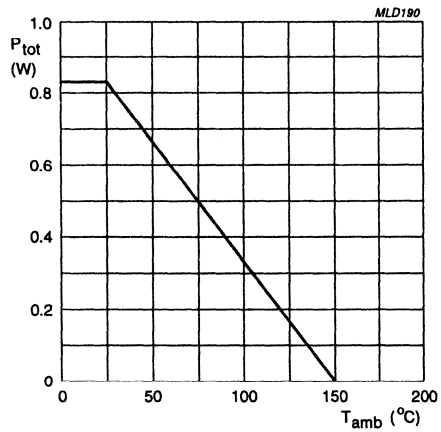
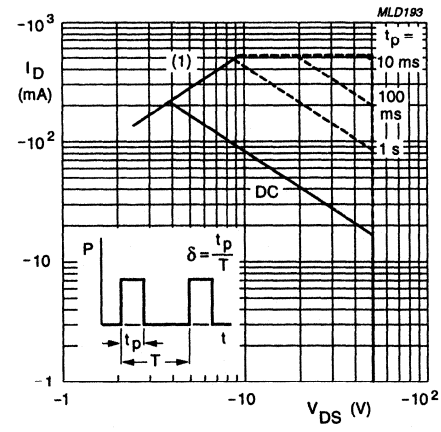


Fig.4 Power derating curve.

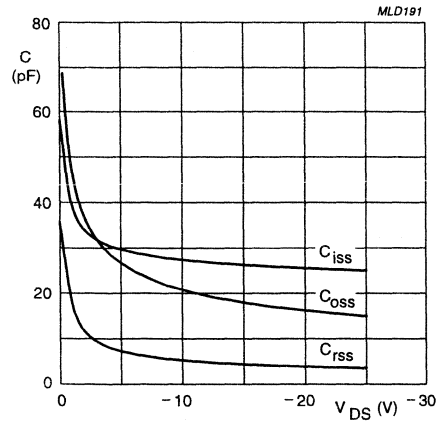


$\delta = 0.01$.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.

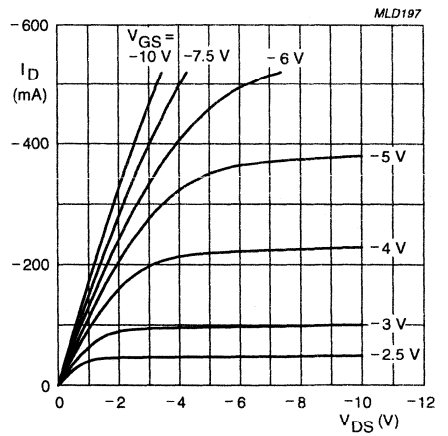
P-channel enhancement mode vertical D-MOS transistor

BSS110



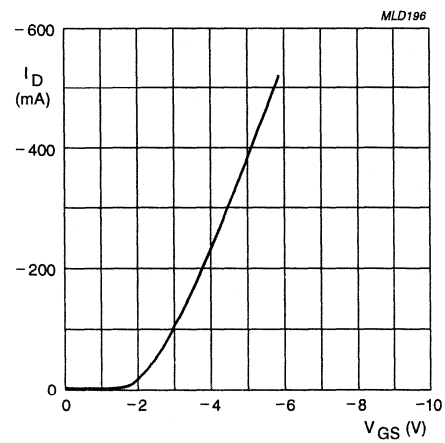
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



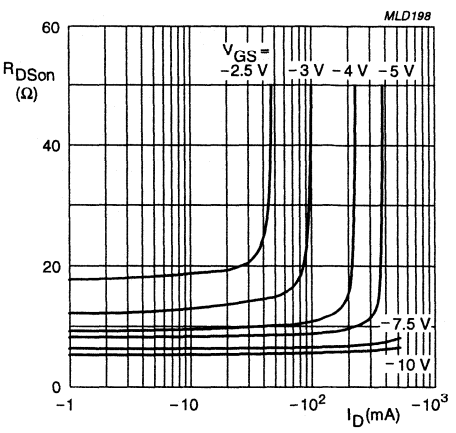
T_j = 25 °C.

Fig.7 Typical output characteristics.



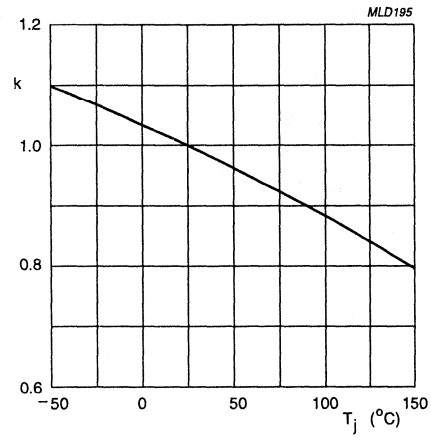
V_{DS} = −10 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



T_j = 25 °C.

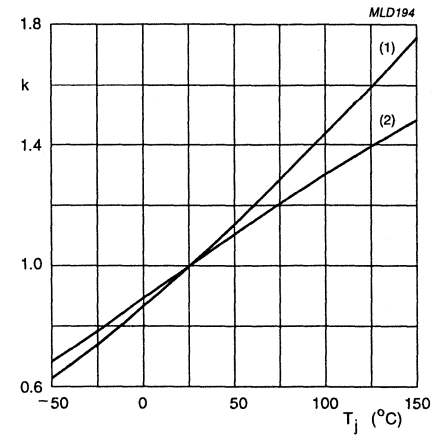
Fig.9 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

$I_D = -1$ mA; $V_{DS} = V_{GS}$.

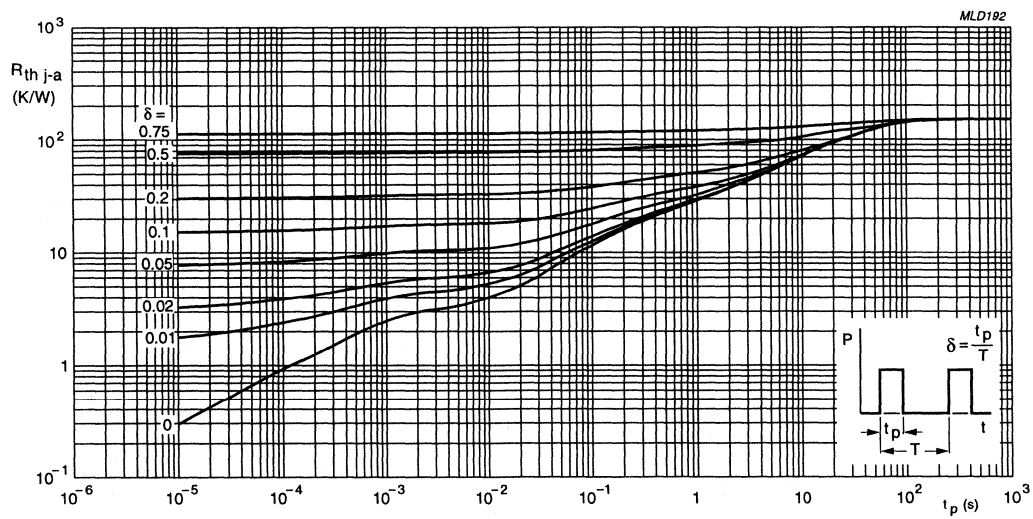
Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) $I_D = -170$ mA; $V_{GS} = -10$ V.
(2) $I_D = -20$ mA; $V_{GS} = -2.4$ V.

Fig.11 Temperature coefficient of drain-source on-state resistance.



$T_{amb} = 25$ °C.

Fig.12 Thermal resistance from junction to ambient as a function of pulse time; typical values.

Data sheet	
status	Product specification
date of issue	April 1995

BSS123
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

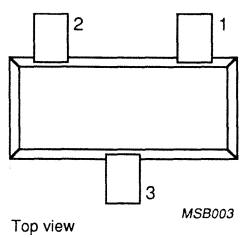
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
i_D	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION



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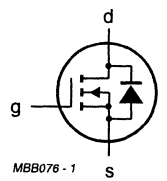


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS123

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	150	mA
I_{DM}	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on a FR4 printboard.

N-channel enhancement mode vertical D-MOS transistor

BSS123

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	40	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	25	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSS123

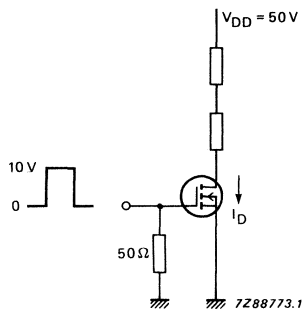


Fig.2 Switching time test circuit.

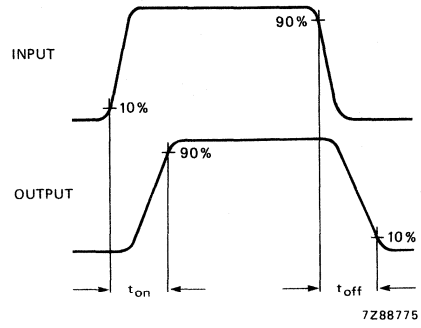


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS131

DESCRIPTION

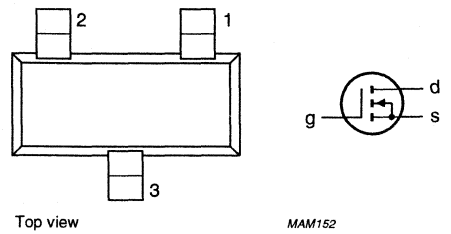
N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	240	V
V_{GSth}	gate-source threshold voltage	2.8	V
I_D	drain current (DC)	100	mA
R_{DSon}	drain-source on-state resistance	16	Ω



Top view MAM152

Marking code: SR.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS FET

BSS131

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
V_{GSO}	gate-source voltage	open drain $I_D = 0$	-	20	V
I_D	drain current	average value	-	100	mA
I_{DM}	drain current	peak value	-	400	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

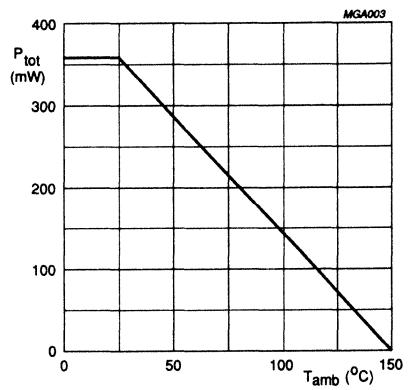


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel enhancement mode vertical D-MOS FET

BSS131

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 250 µA	240	-	-	V
I_{DSS}	drain-source leakage current	V_{GS} = 0 V_{DS} = 130 V	-	-	30	nA
		V_{GS} = 0 V_{DS} = 240 V	-	-	15	µA
		V_{GS} = 0 V_{DS} = 240 V T_j = 125 °C	-	-	60	µA
I_{GSS}	gate-source leakage current	V_{DS} = 0 V_{GS} = 20 V	-	-	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 10 V I_D = 100 mA	-	-	16	Ω
$\|Y_{fs}\|$	transfer admittance	V_{DS} = 25 V I_D = 100 mA f = 1 kHz	60	100	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	6	-	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	2.5	-	pF
t_{on}	turn-on time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0-5 V	-	20	-	ns
t_{off}	turn-off time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0-5 V	-	40	-	ns

N-channel enhancement mode vertical D-MOS transistor

BSS138

FEATURES

- Low threshold voltage
- CMOS compatible
- Low on-resistance.

DESCRIPTION

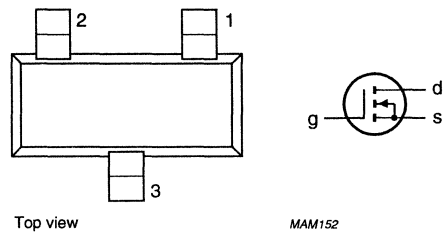
N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	50	V
V_{GSth}	gate-source threshold voltage	1.5	V
I_D	drain current (DC)	200	mA
R_{DSon}	drain-source on-state resistance	3.5	Ω



Marking code: SS.

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS FET

BSS138

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	50	V
V_{GSO}	gate-source voltage	open drain $I_D = 0$	-	20	V
I_D	drain current	average value	-	200	mA
I_{DM}	drain current	peak value	-	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

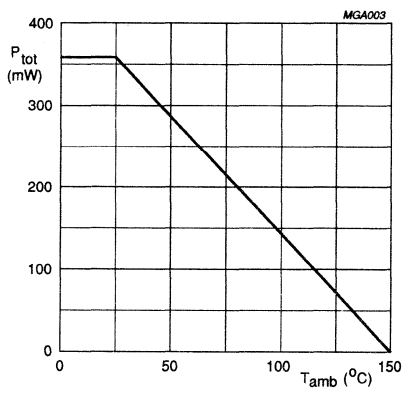


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel enhancement mode vertical D-MOS FET

BSS138

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 250 μA	50	-	-	V
I_{DSS}	drain-source leakage current	V_{GS} = 0 V_{DS} = 25 V	-	-	0.1	μA
		V_{GS} = 0 V_{DS} = 50 V	-	-	0.5	μA
		V_{GS} = 0 V_{DS} = 50 V T_j = 125 °C	-	-	5	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0 V_{GS} = 20 V	-	-	0.1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.5	-	1.5	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 5 V I_D = 200 mA	-	2	3.5	Ω
$\|Y_{fs}\|$	transfer admittance	V_{DS} = 25 V I_D = 200 mA f = 1 kHz	100	200	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	40	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	12	-	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	-	pF
t_{on}	turn-on time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0/5 V	-	16	-	ns
t_{off}	turn-off time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0/5 V	-	40	-	ns

Data sheet	
status	Product specification
date of issue	July 1993

BSS192
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 envelope, intended for use in relay, high-speed and line transformer drivers, and as a line current interruptor in telephony applications.

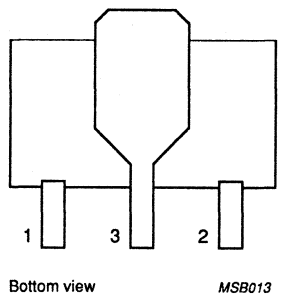
PINNING - SOT89

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 100 mA $-V_{GS}$ = 10 V	20	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION



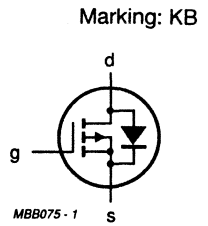


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSS192

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	150	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Transistor mounted on a ceramic substrate, area 2.5 cm², thickness 0.7 mm.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on a ceramic substrate, area 2.5 cm², thickness 0.7 mm.

P-channel enhancement mode vertical D-MOS transistor

BSS192

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 60 V V_{GS} = 0	–	–	0.2	μA
		$-V_{DS}$ = 200 V $-V_{GS}$ = 0.2 V	–	0.1	60	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 100 mA $-V_{GS}$ = 10 V	–	10	20	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	60	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	55	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSS192

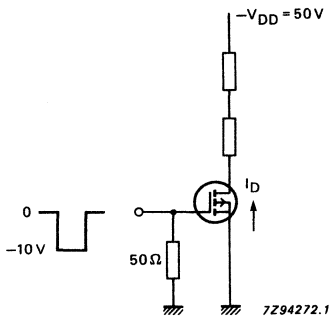


Fig.2 Switching time test circuit.

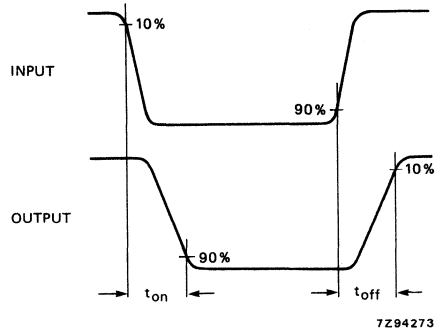


Fig.3 Input and output waveforms.

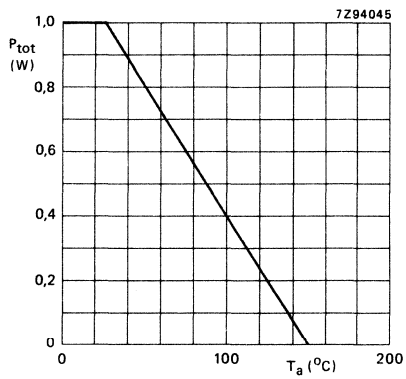


Fig.4 Power derating curve.

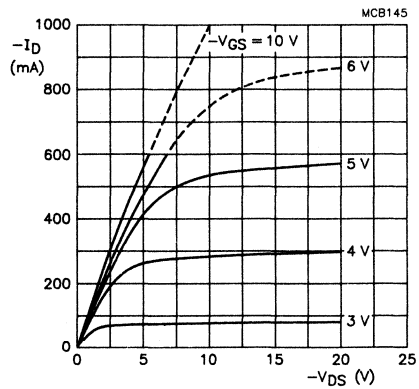


Fig.5 Typical output characteristics; $T_j = 25\,°C$.

P-channel enhancement mode vertical D-MOS transistor

BSS192

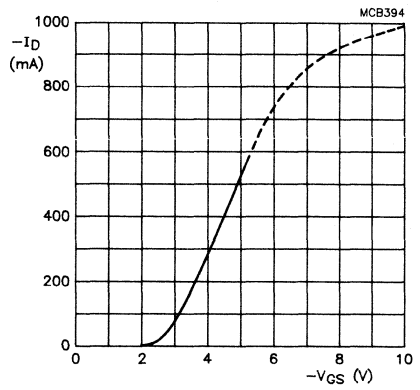


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

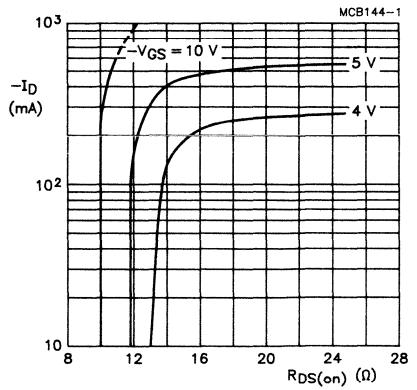


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

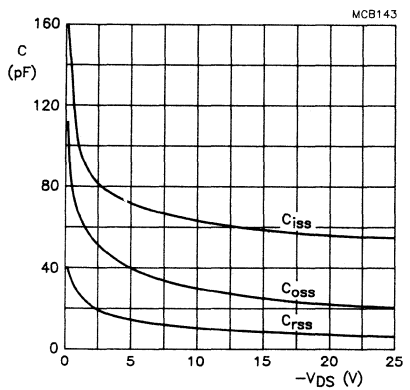


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

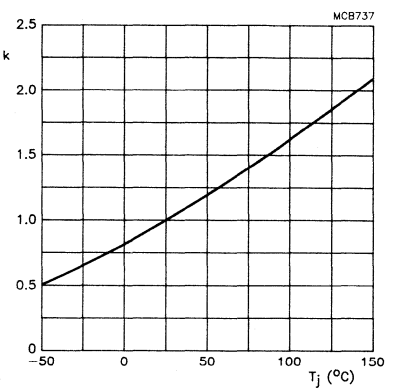


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

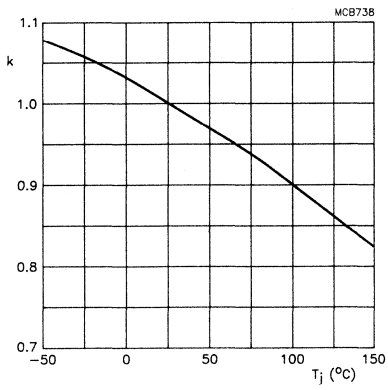


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS(th)}\ at\ 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2 Ω 4 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\|y_{fs}\|$	typ.	300 mS

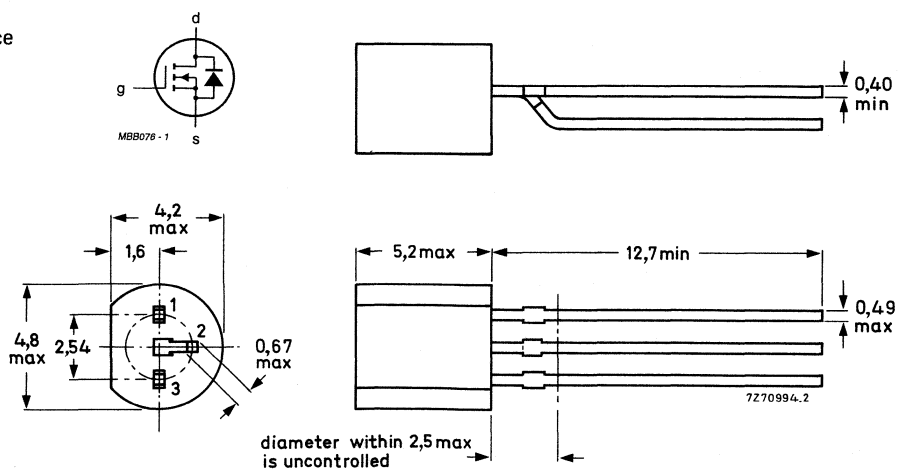
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance (see Fig. 4) I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

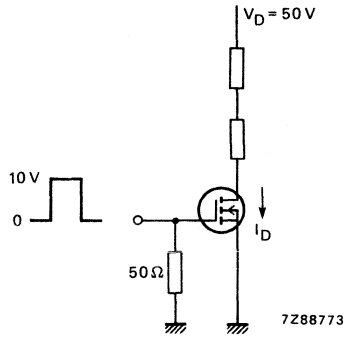


Fig. 2 Switching times test circuit.

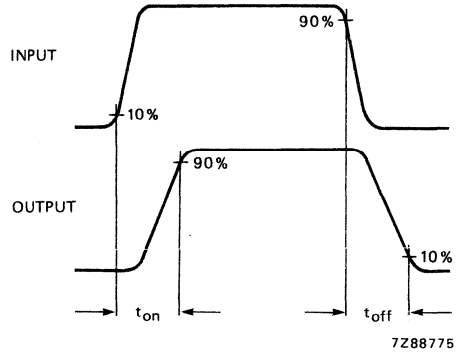


Fig. 3 Input and output waveforms.

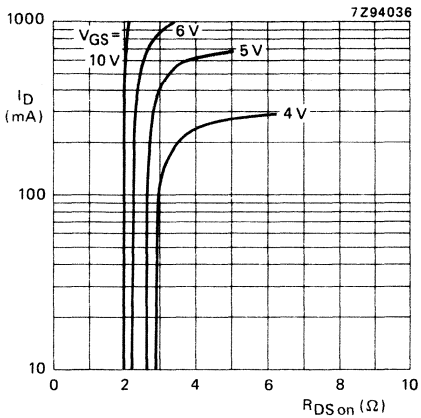


Fig. 4 T_j = 25 °C; typical values.

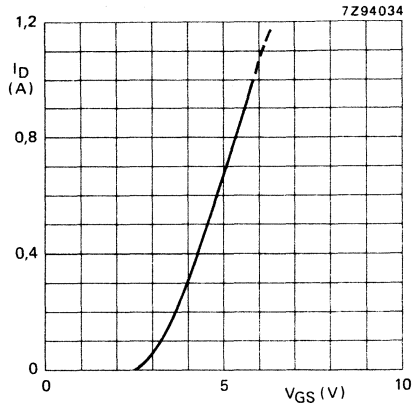


Fig. 5 T_j = 25 °C; typical values at V_{DS} = 10 V.

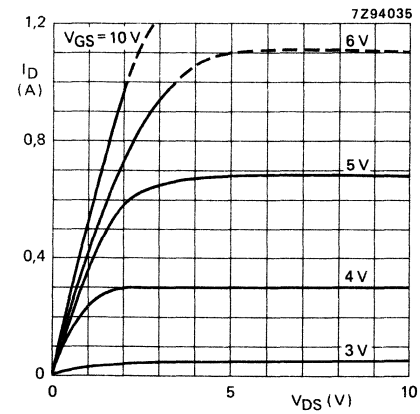


Fig. 6 T_j = 25 °C; typical values.

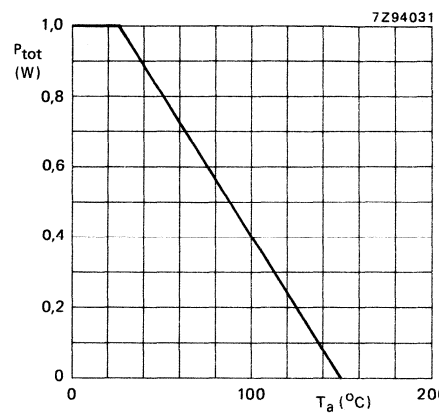


Fig. 7 Power derating curve.

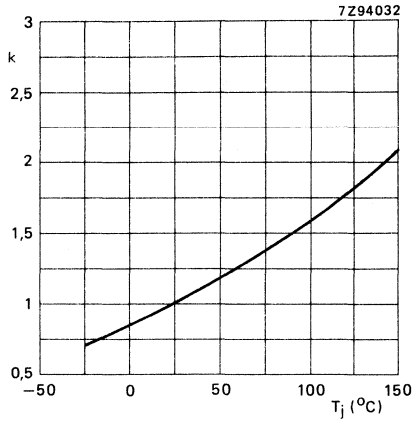


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typ. values at 500 mA/10 V.

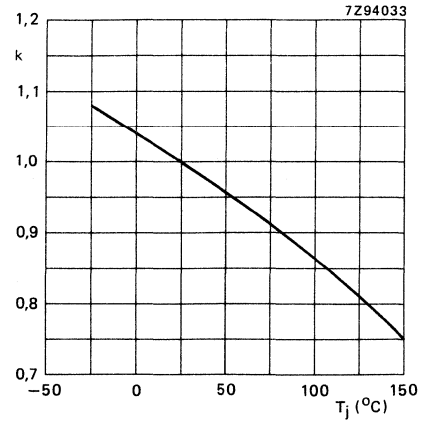


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

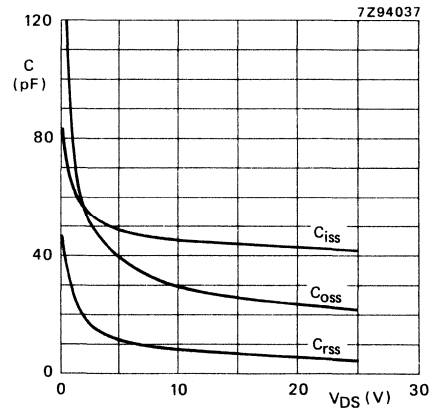


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	0.83 W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V	$\|y_{fs}\|$	typ.	150 mS

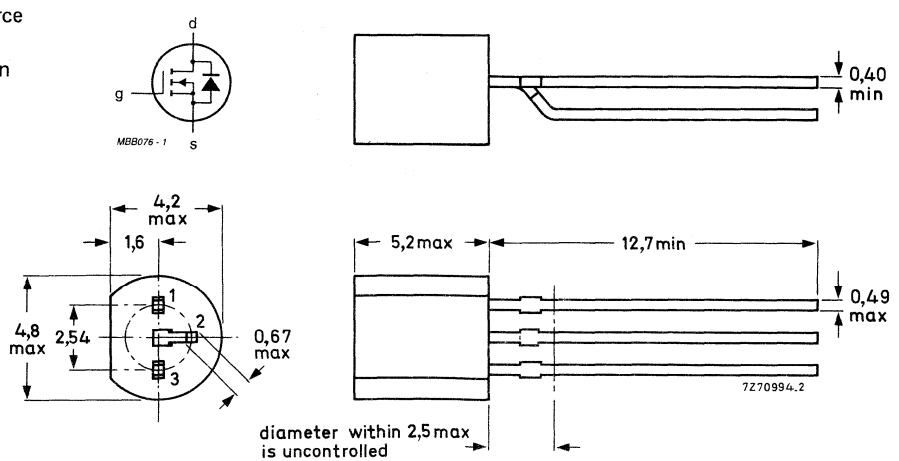
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance (see Fig. 4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	13 pF 20 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	3 pF 6 pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	4 ns 10 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

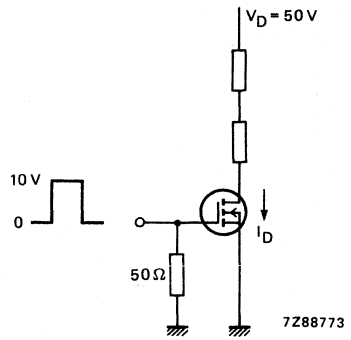


Fig. 2 Switching times test circuit.

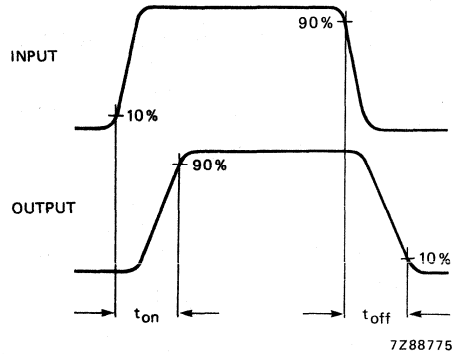


Fig. 3 Input and output waveforms.

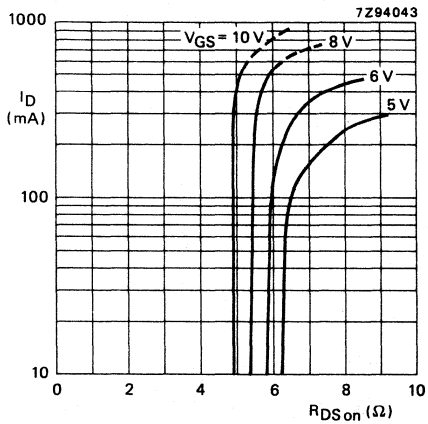


Fig. 4 T_j = 25 °C; typical values.

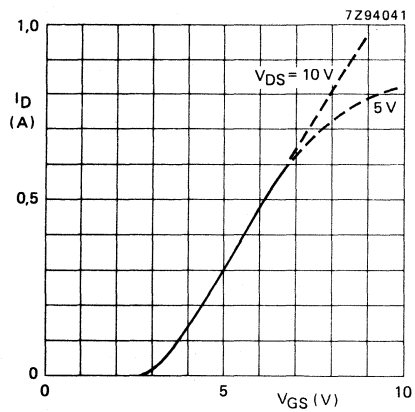


Fig. 5 T_j = 25 °C; typical values.

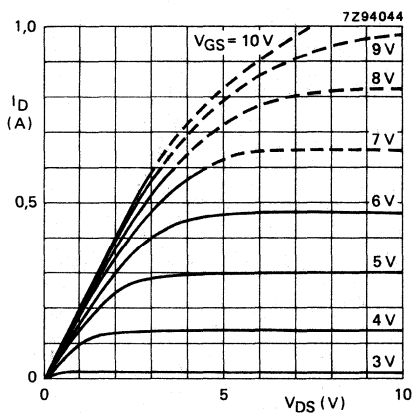


Fig. 6 T_j = 25 °C; typical values.

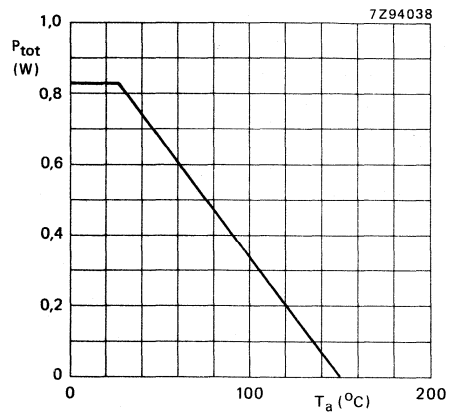


Fig. 7 Power derating curve.

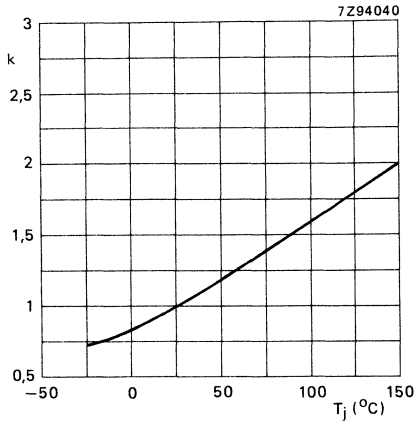


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ °C}}$; typ. values at 150 mA/5 V.

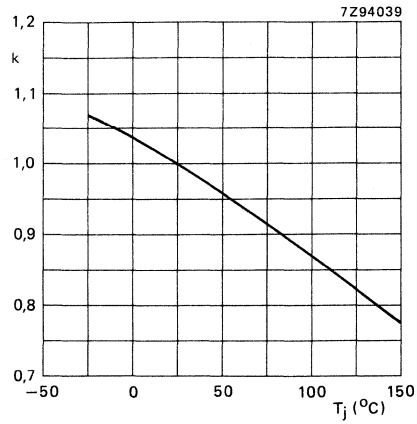


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ °C}}$; $V_{GS(th)}$ at 1 mA; typical values.

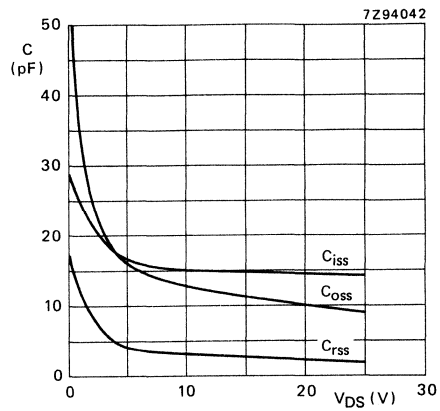


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

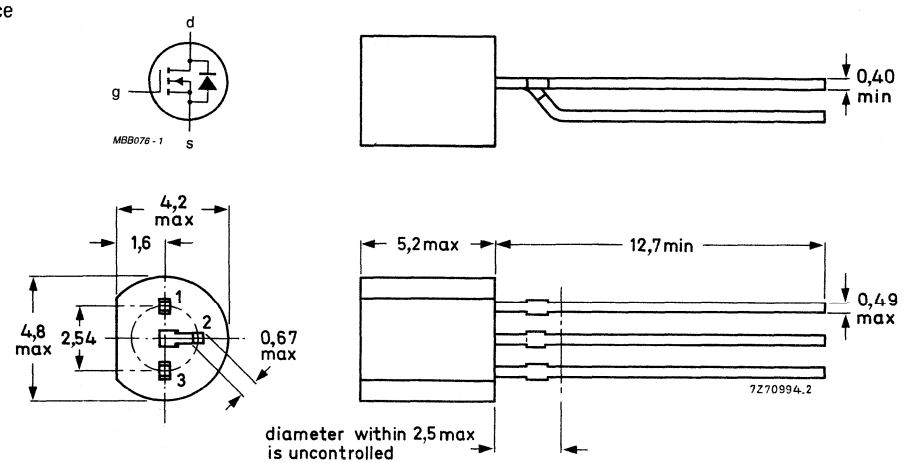
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig. 4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	70 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4 ns
		max.	10 ns
	t_{off}	typ.	15 ns
		max.	25 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

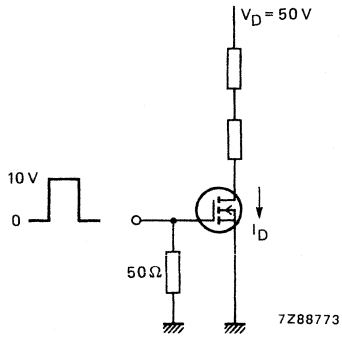


Fig. 2 Switching times test circuit.

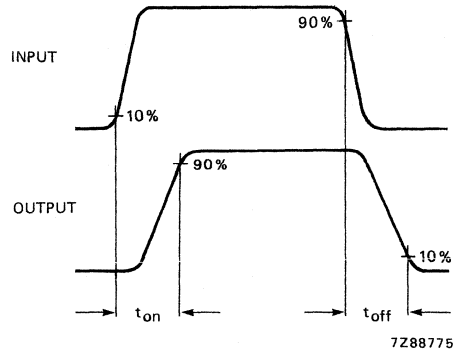


Fig. 3 Input and output waveforms.

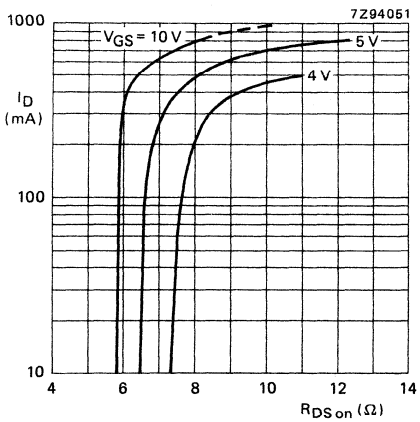


Fig. 4 T_j = 25 °C; typical values.

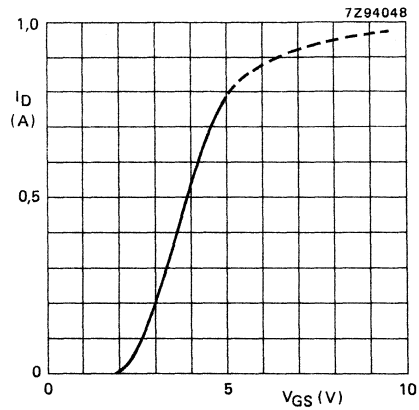


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

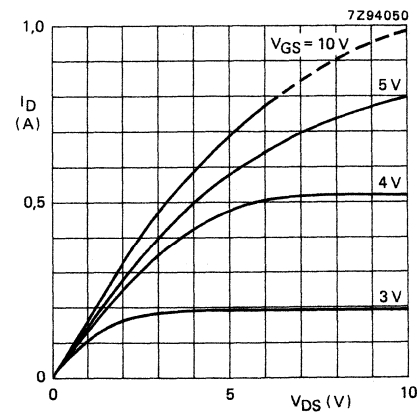


Fig. 6 T_j = 25 °C; typical values.

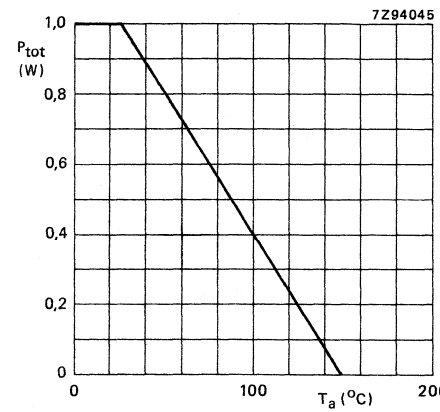


Fig. 7 Power derating curve.

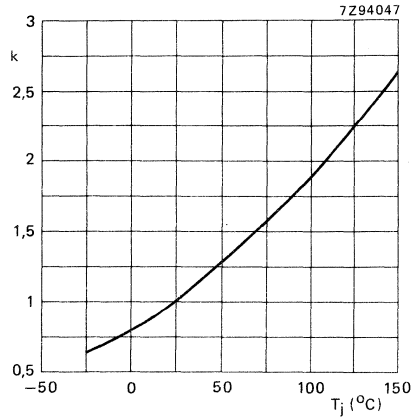


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; at 400 mA/10 V; typical values.

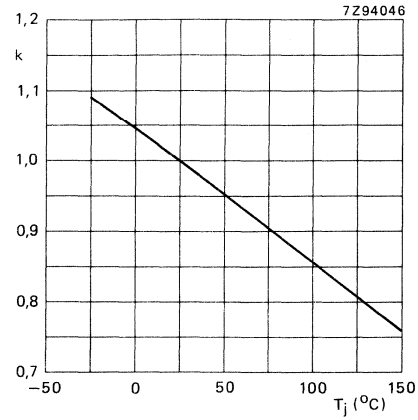


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 1 mA; typical values.

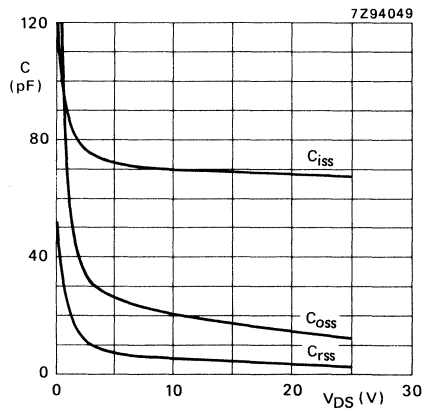


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

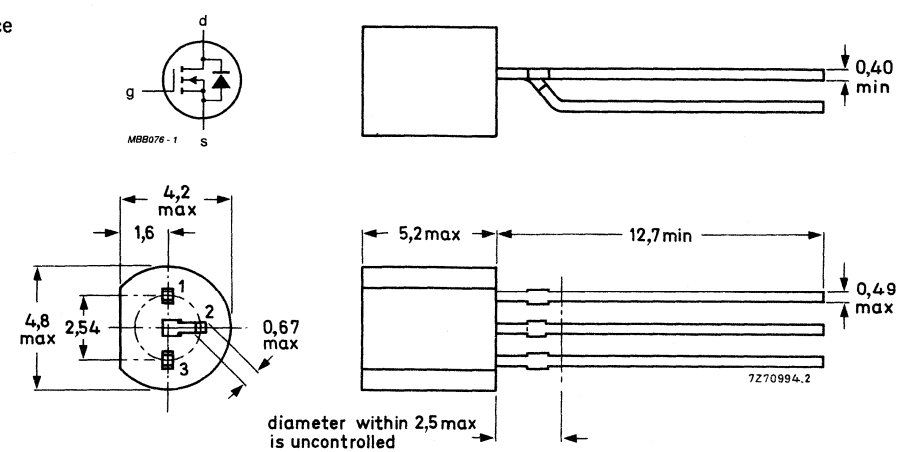
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	180	V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.7 2.4	V V
Drain-source ON-resistance (see Fig. 4) I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 10	Ω Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{is}	typ. max.	50 65	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{os}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ. max.	6 10	pF pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 15	ns ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

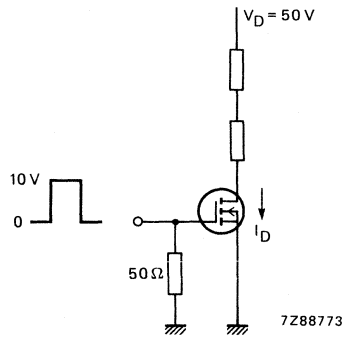


Fig. 2 Switching times test circuit.

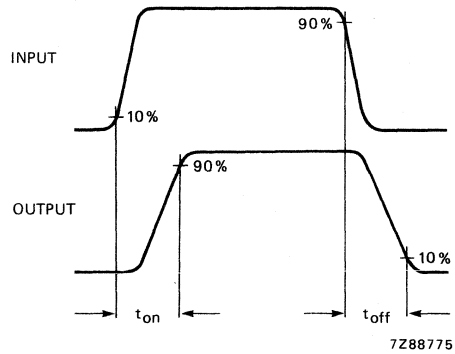


Fig. 3 Input and output waveforms.

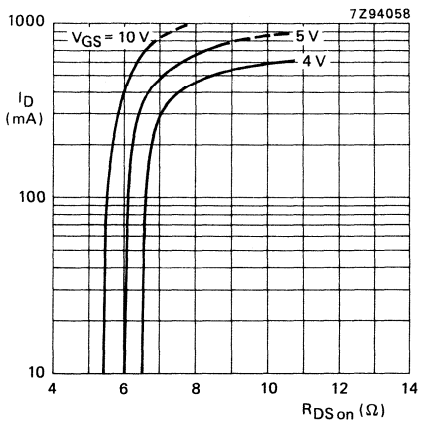


Fig. 4 T_j = 25 °C; typical values.

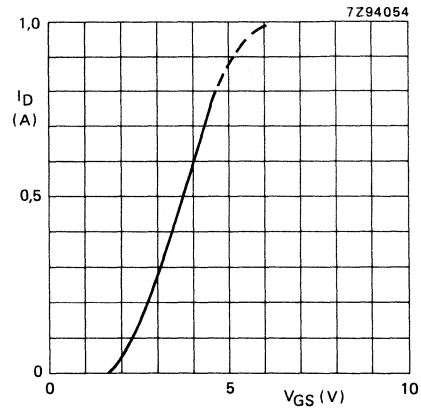


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

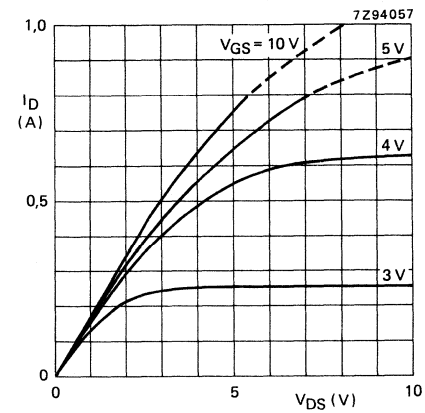


Fig. 6 T_j = 25 °C; typical values.

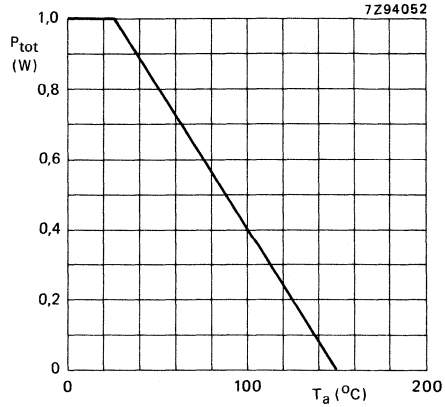


Fig. 7 Power derating curve.

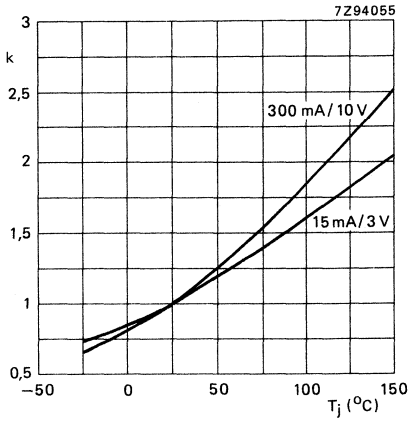


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; typical values.

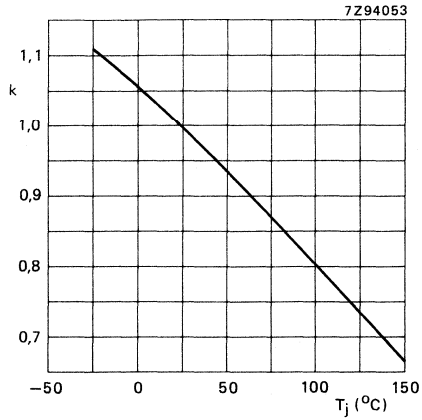


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 0,1 mA; typical values.

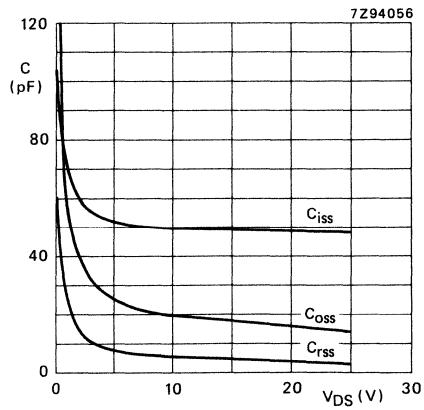


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

HIGH-VOLTAGE N-CHANNEL VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Drain-source ON-resistance $I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15 Ω
Transfer admittance $I_D = 250$ mA; $V_{DS} = 20$ V	$\lvert y_{fs} \rvert$	typ.	400 mS

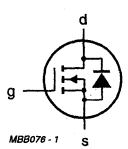
MECHANICAL DATA

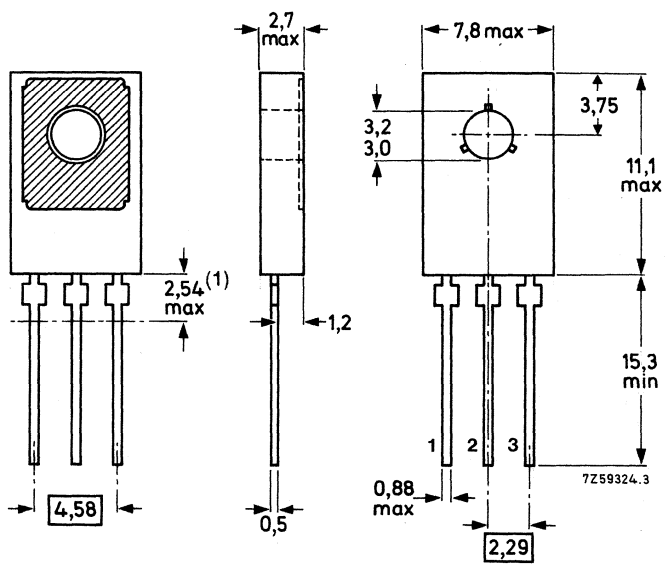
Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.

Pinning;
1 = source
2 = drain
3 = gate





(1) Lead dimensions uncontrolled under this zone

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Drain current (peak)	I_{DM}	max.	1,5 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Storage temperature	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$		100 K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$		5 K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A; V_{GS} = 0$	$V_{(BR)DS}$	>	450 V
Drain-source leakage current $V_{DS} = 350\ V; V_{GS} = 0$	I_{DSS}	<	25 μA
Gate-source leakage current $V_{GS} = 20\ V; V_{DS} = 0$	I_{GSS}	<	100 nA
Gate-source cut-off voltage $I_D = 1\ mA; V_{DS} = V_{GS}$	$V_{(P)GS}$	>	2,0 V
		<	4,0 V
Drain-source ON-resistance (see Fig. 4) $I_D = 100\ mA; V_{GS} = 10\ V$	R_{DSon}	typ.	10 Ω
		<	14 Ω
$I_D = 500\ mA; V_{GS} = 10\ V$	R_{DSon}	typ.	15 Ω
Transfer admittance $I_D = 250\ mA; V_{DS} = 20\ V$	$\lvert y_{fs} \rvert$	typ.	400 mS
Input capacitance at f = 1 MHz $V_{DS} = 10\ V; V_{GS} = 0$	C_{is}	typ.	75 pF
		<	100 pF
Output capacitance at f = 1 MHz $V_{DS} = 10\ V; V_{GS} = 0$	C_{os}	typ.	25 pF
		<	35 pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10\ V; V_{GS} = 0$	C_{rs}	typ.	3 pF
		<	5 pF
Switching times (see Figs 2 and 3) $I_D = 100\ mA; V_{DS} = 200\ V; V_{GS} = 0$ to 10 V	t_{on}	<	10 ns
	t_{off}	<	100 ns

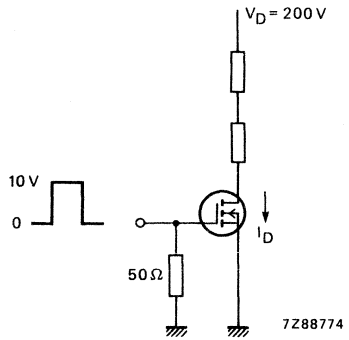


Fig. 2 Switching times test circuit.

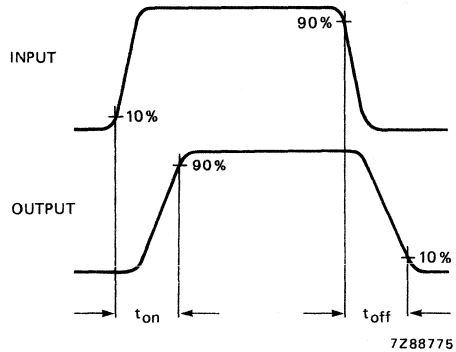


Fig. 3 Input and output waveforms.

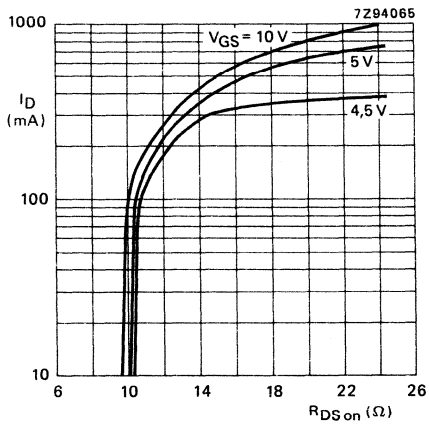


Fig. 4 T_j = 25 °C; typical values.

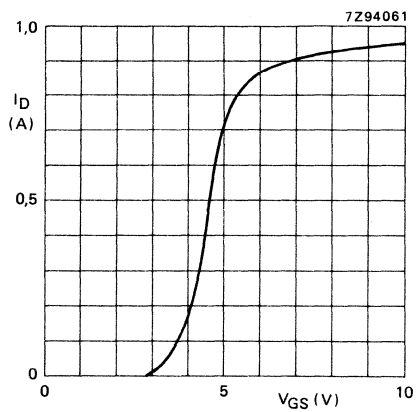


Fig. 5 T_j = 25 °C; V_{DS} = 20 V; typical values.

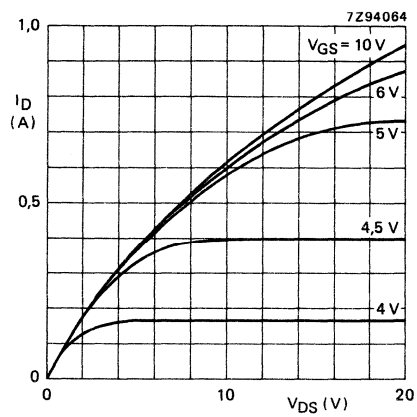


Fig. 6 T_j = 25 °C; typical values.

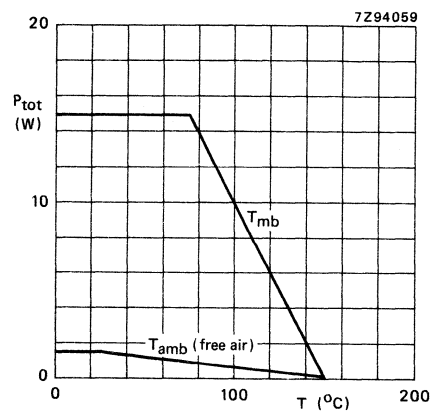


Fig. 7 Power derating curve.

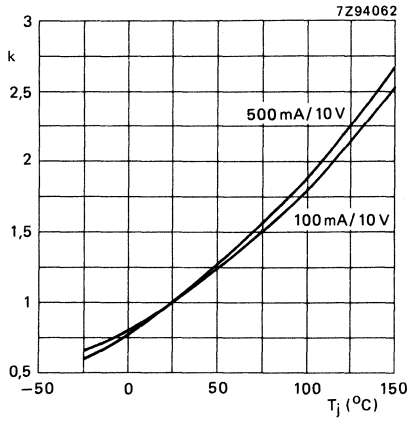


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; typical values.

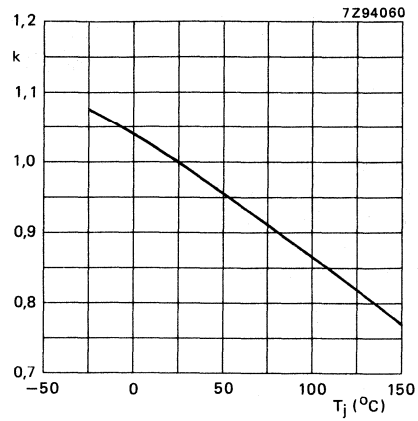


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 1 mA; typical values.

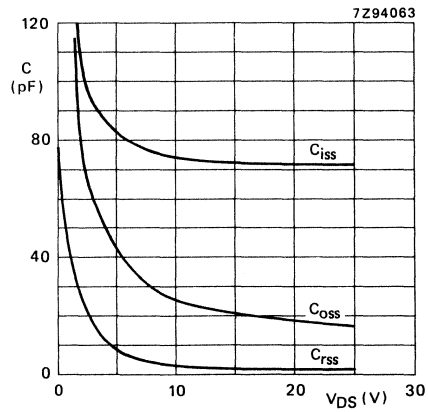


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Low $R_{DS\ on}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 4.0	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300	mS

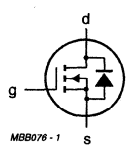
MECHANICAL DATA

Dimensions in mm

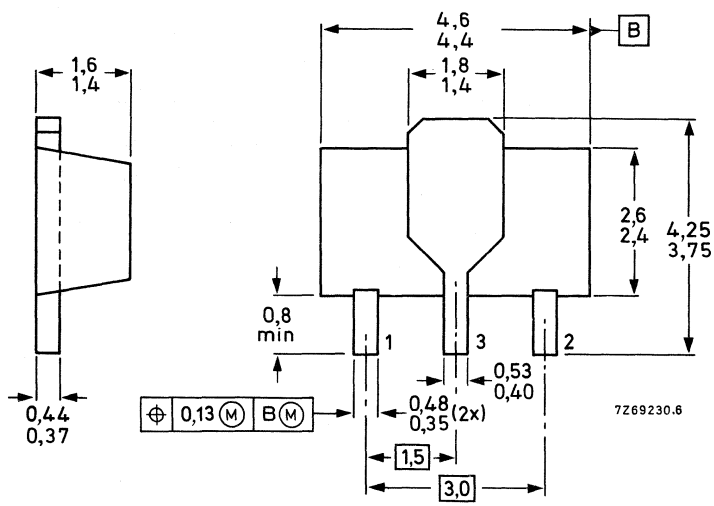
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: KM



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 3.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistors mounted on a substrate with surface area of 2.5 cm^2 and thickness of 0.7 mm.

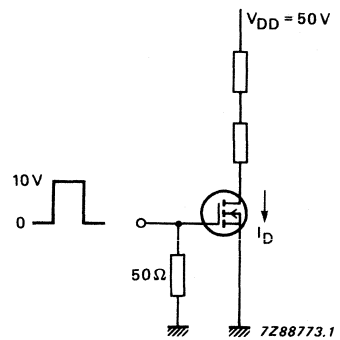


Fig.2 Switching times test circuit.

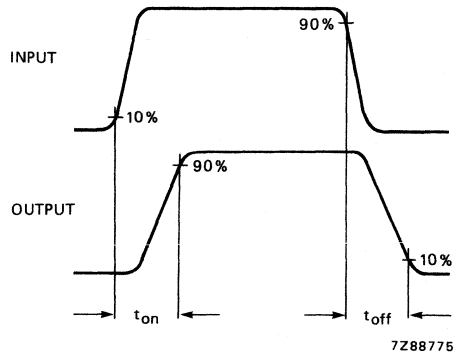


Fig.3 Input and output waveforms.

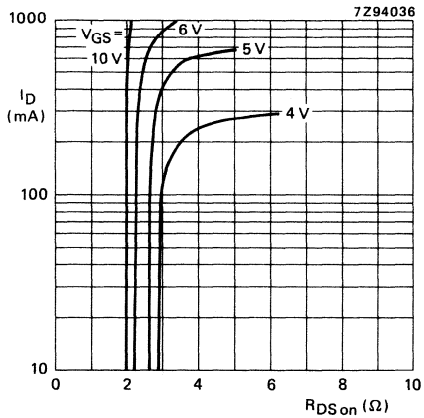


Fig.4 T_j = 25 °C; typical values.

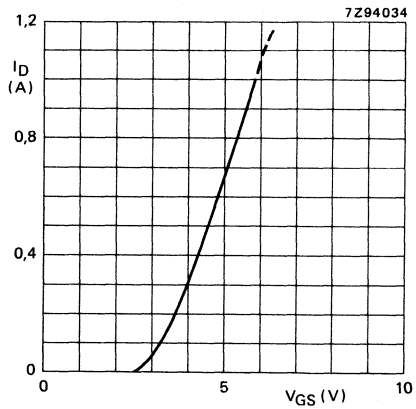


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

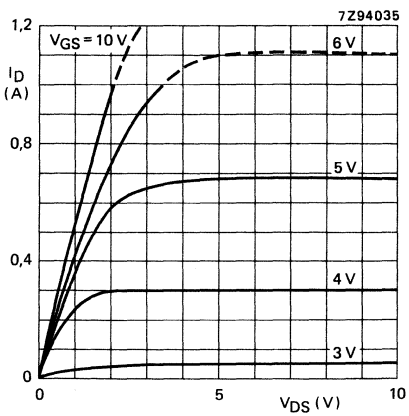


Fig.6 T_j = 25 °C; typical values.

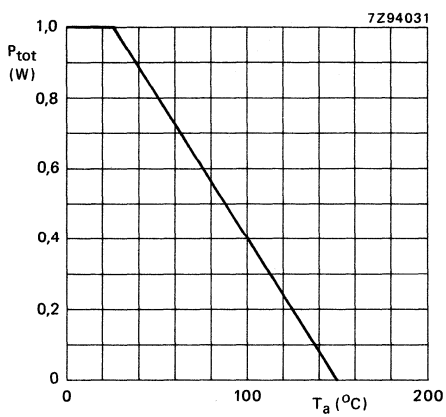


Fig.7 Power derating curve.

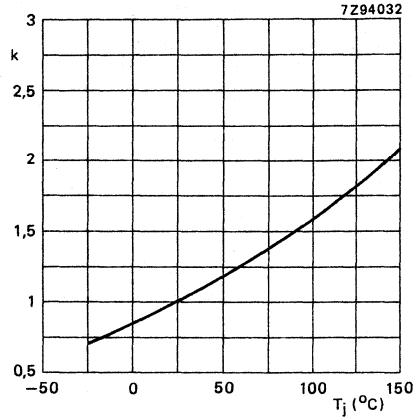


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\ ^oC}$; typ. values. at 500 mA/10 V.

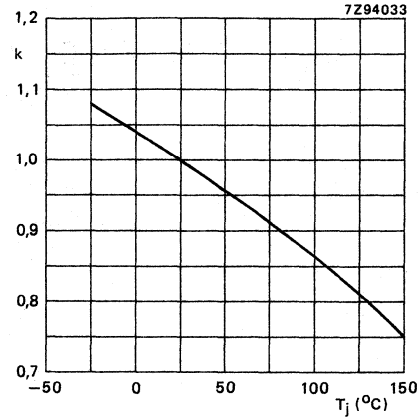


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

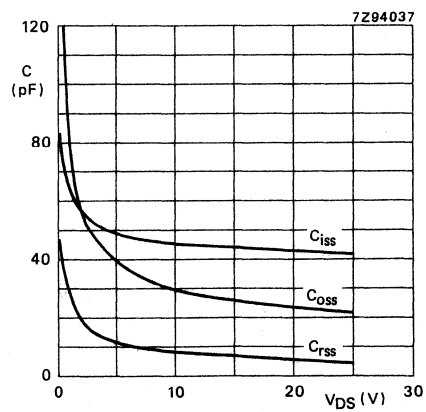


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300	mW
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance $I_D = 175$ mA; $V_{DS} = 5$ V	$\lvert y_{fs} \rvert$	typ.	150	mS

MECHANICAL DATA

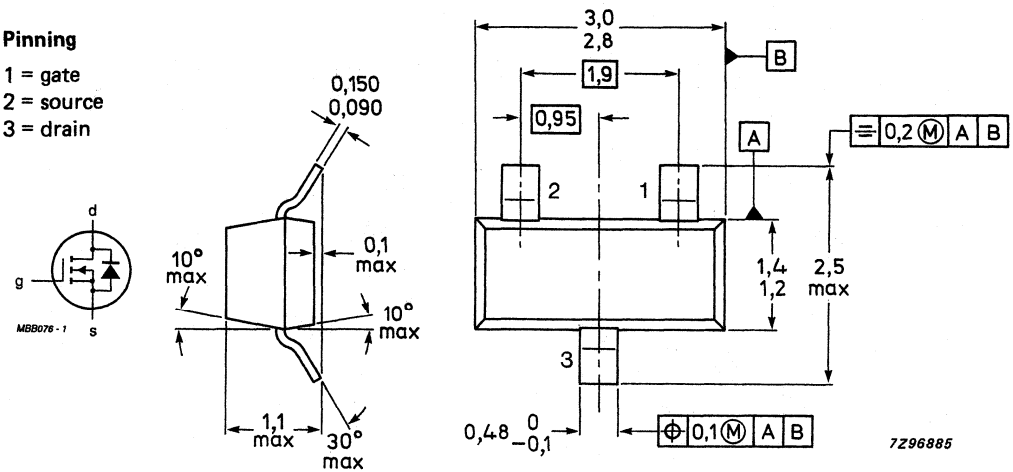
Dimensions in mm

Fig.1 SOT23.

Marking: 02p

Pinning

1 = gate
2 = source
3 = drain



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 pF 20 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 pF 6 pF
Switching times (see Figs 2 and 3) I_D = 175 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	4 ns 10 ns

Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

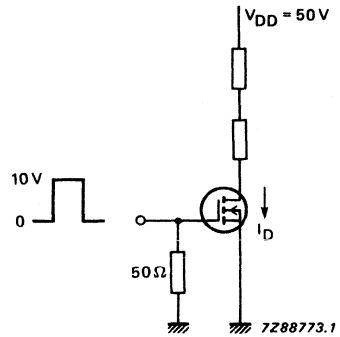


Fig.2 Switching times test circuit.

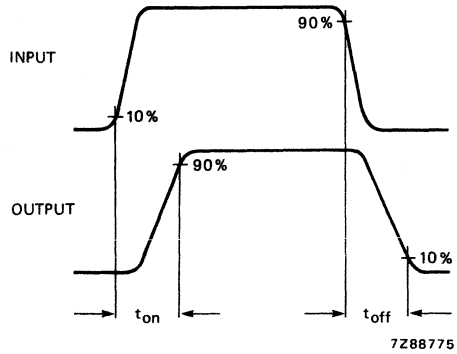


Fig.3 Input and output waveforms.

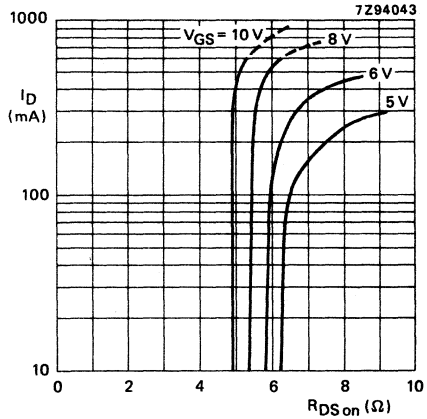


Fig.4 T_j = 25 °C; typical values.

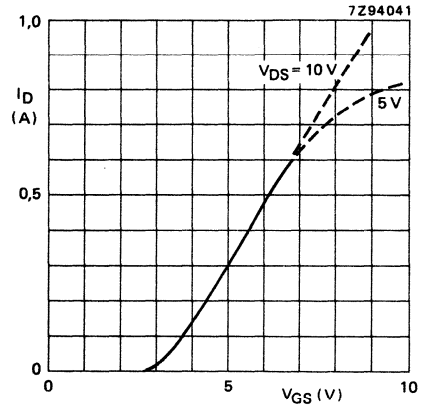


Fig.5 T_j = 25 °C; typical values.

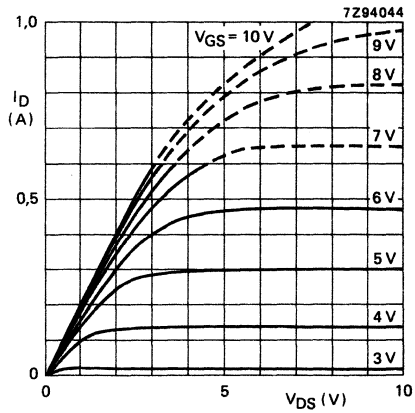


Fig.6 T_j = 25 °C; typical values.

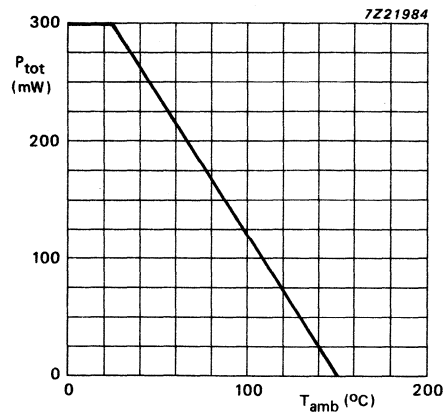


Fig.7 Power derating curve.

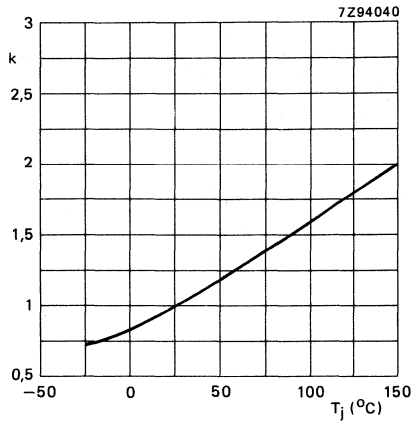


Fig.8 $k = \frac{R_{DS\,on}\ \text{at}\ T_j}{R_{DS\,on}\ \text{at}\ 25\,^{o}C}$; typ. values at 150 mA/5 V.

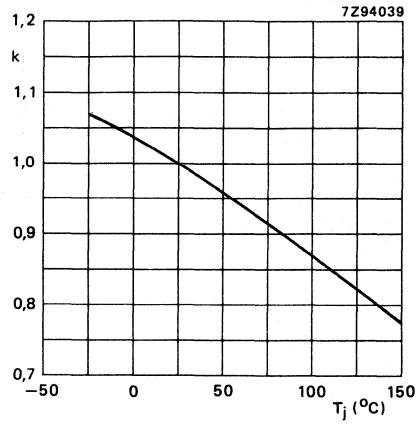


Fig.9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

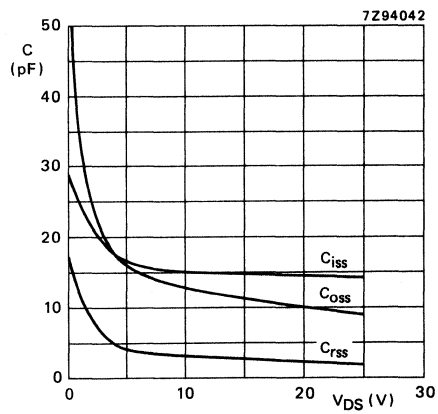


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

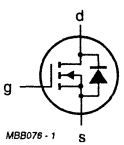
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

MECHANICAL DATA

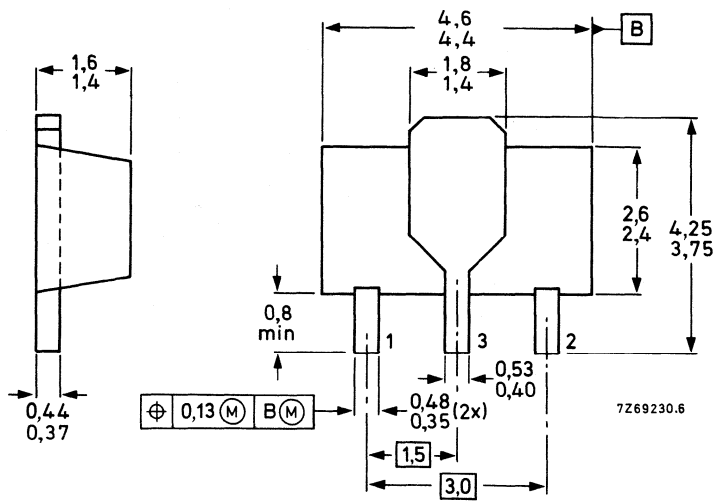
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



Marking: KN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	70 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	15 ns 25 ns

Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

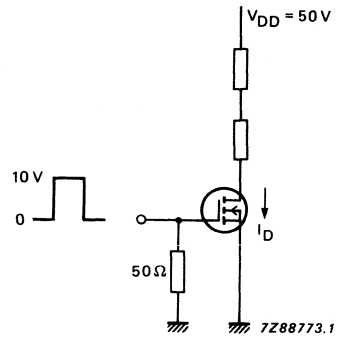


Fig. 2 Switching times test circuit.

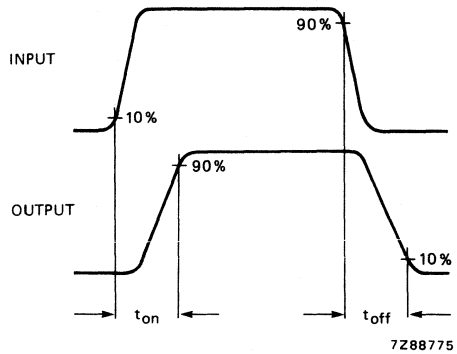


Fig. 3 Input and output waveforms.

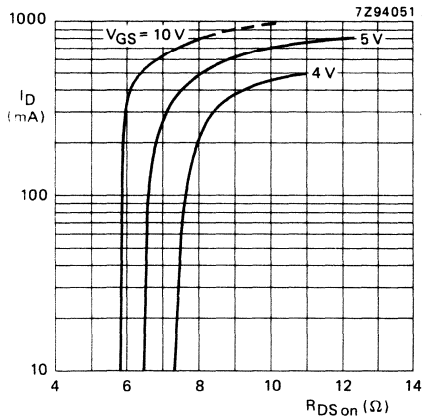


Fig. 4 T_j = 25 °C; typical values.

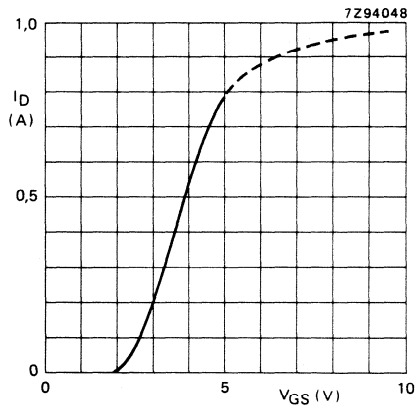


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

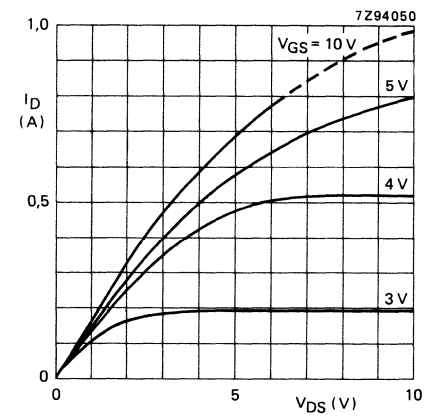


Fig. 6 T_j = 25 °C; typical values.

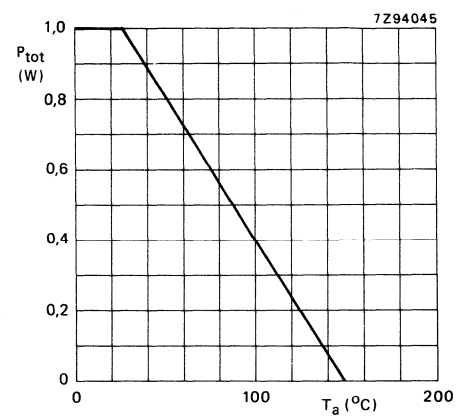


Fig. 7 Power derating curve.

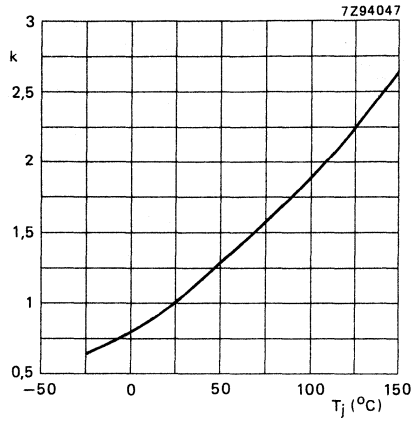


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; at 400 mA/10 V; typical values.

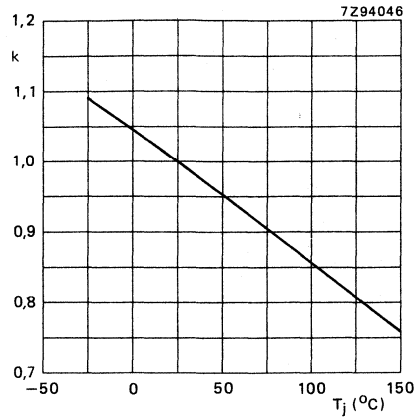


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 1 mA; typical values.

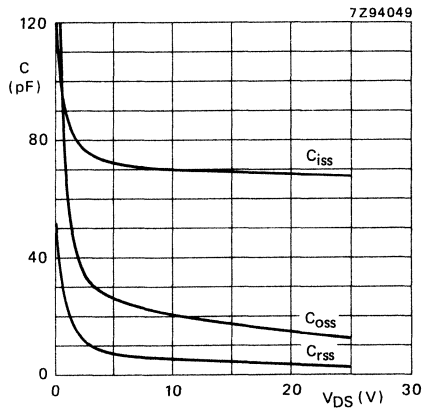


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1	W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V	$\lvert y_{fs} \rvert$	typ.	250	mS

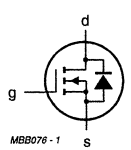
MECHANICAL DATA

Dimensions in mm

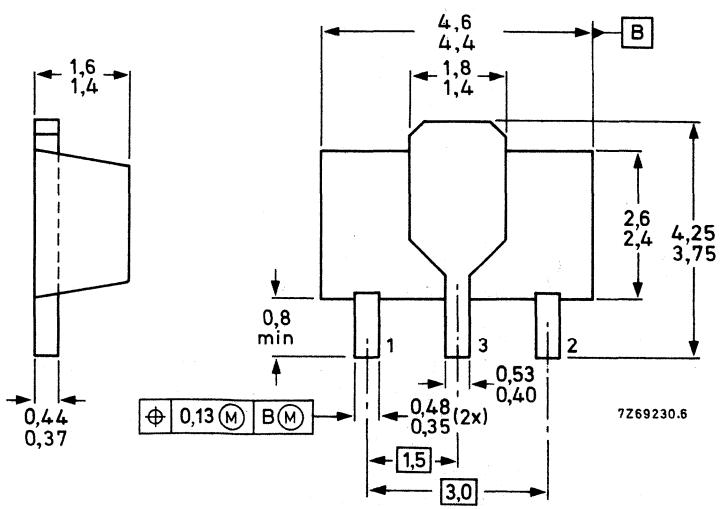
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: K0



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180 V
Drain-source leakage current			
V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage			
I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.7 V
		max.	2.7 V
Drain-source ON-resistance			
I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ.	7 Ω
		max.	10 Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6 Ω
Transfer admittance			
I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	50 pF
		max.	65 pF
Output capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20 pF
		max.	30 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	6 pF
		max.	10 pF
Switching times (see Figs 2 and 3)			
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	max.	10 ns
	t_{off}	max.	15 ns

1. Transistors mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

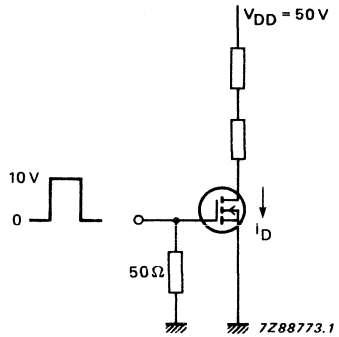


Fig.2 Switching times test circuit.

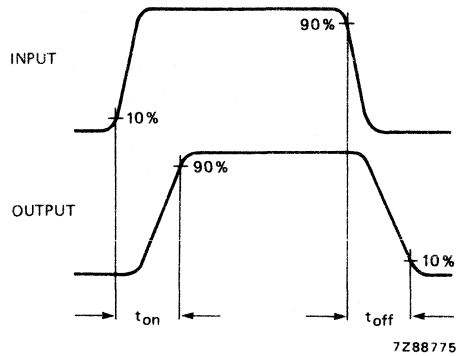


Fig.3 Input and output waveforms.

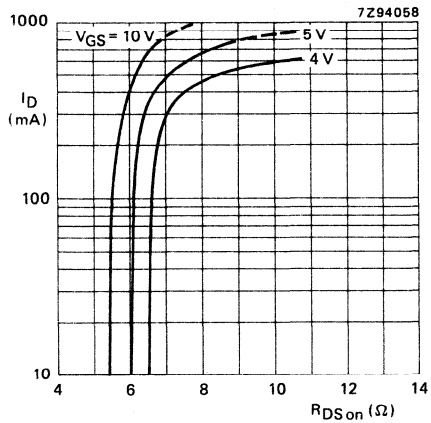


Fig.4 T_j = 25 °C; typical values.

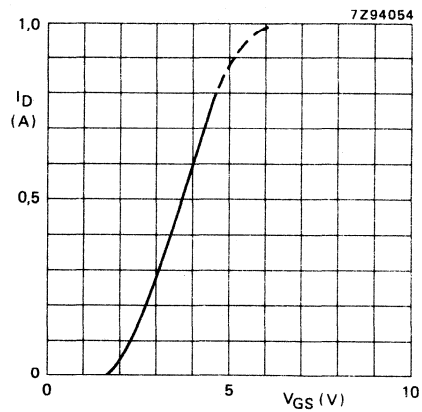


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

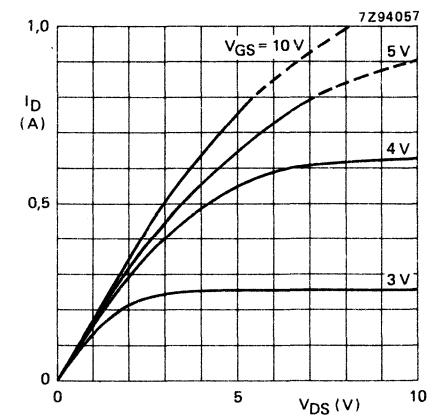


Fig.6 T_j = 25 °C; typical values.

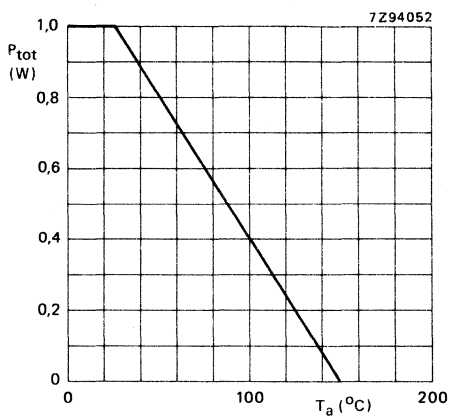


Fig.7 Power derating curve.

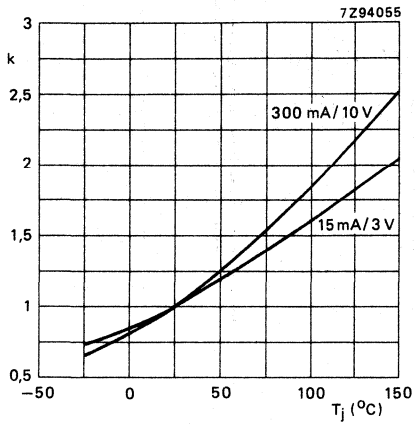


Fig.8 $k = \frac{R_{DS\,on} \text{ at } T_j}{R_{DS\,on} \text{ at } 25\ ^oC}$; typical values.

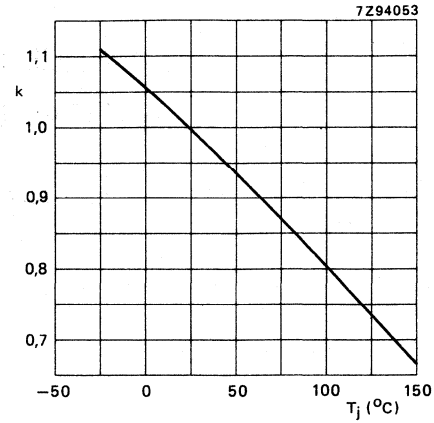


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 0.1 mA; typical values.

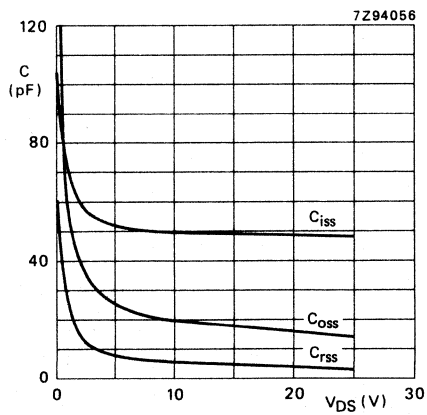


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS

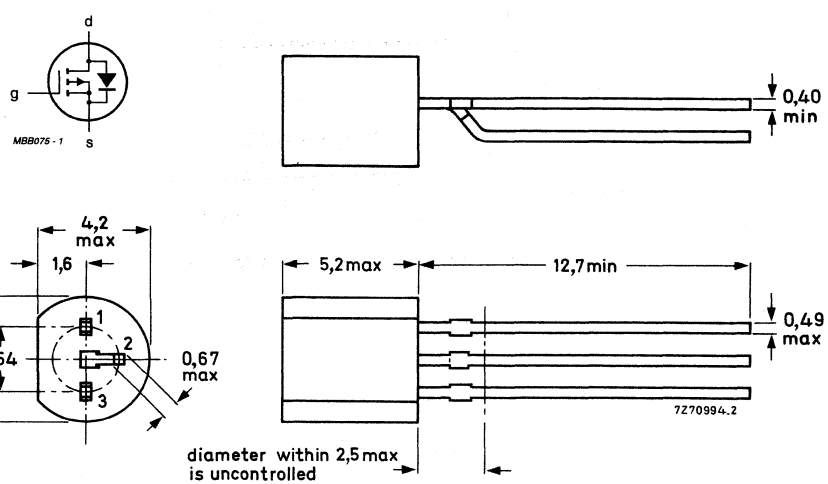
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

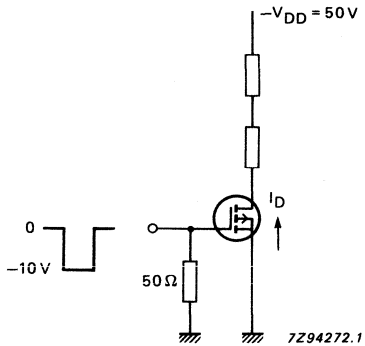


Fig.2 Switching times test circuit.

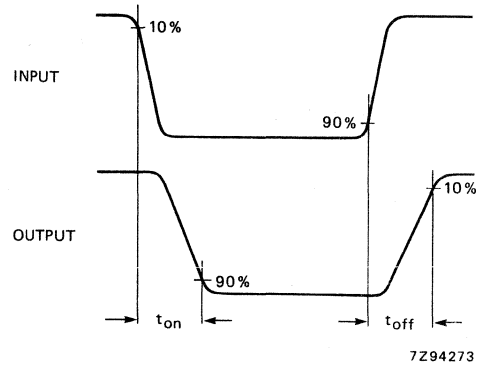


Fig.3 Input and output waveforms.

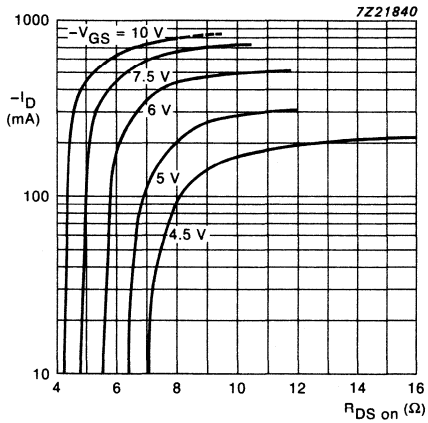


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

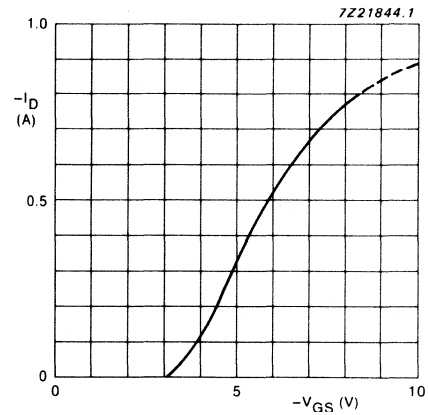


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

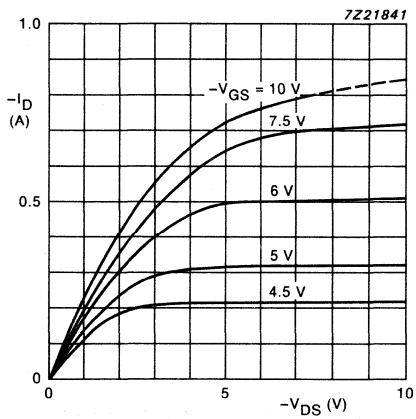


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENCHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 Ω 10 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS

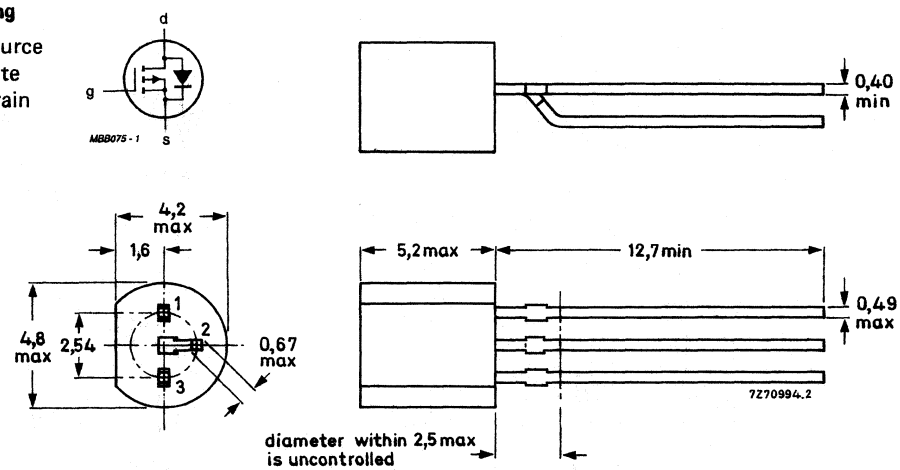
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 Ω 10 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

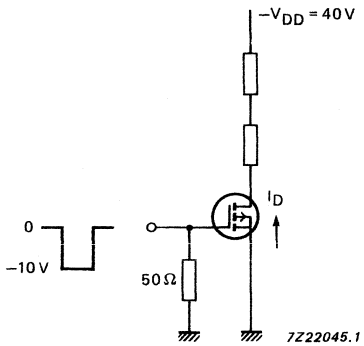


Fig.2 Switching times test circuit.

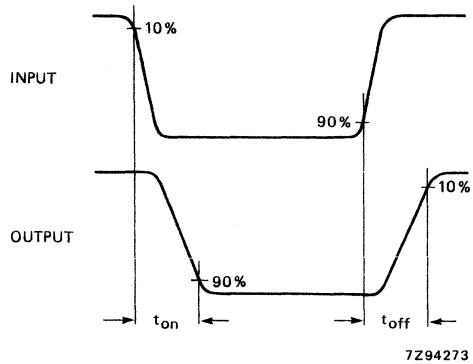


Fig.3 Input and output waveforms.

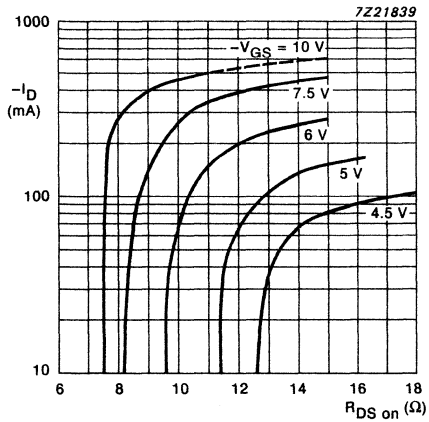


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

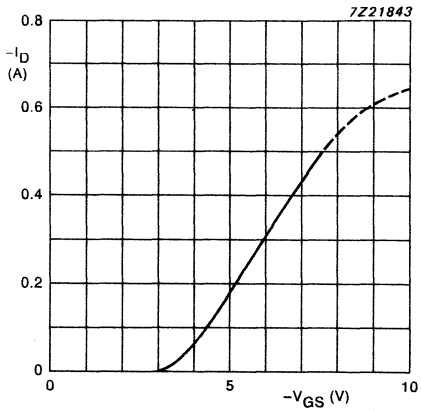


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

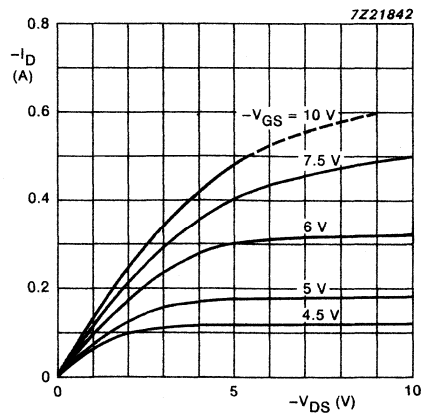


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

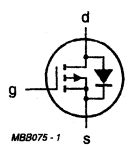
Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0,3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS

MECHANICAL DATA

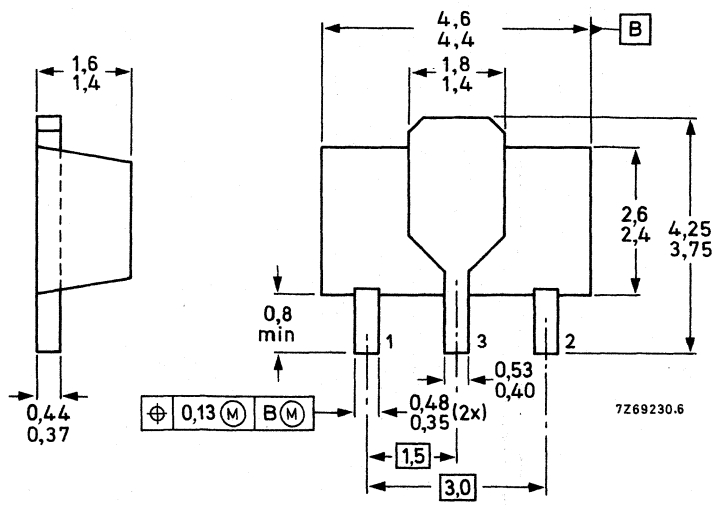
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



marking: LM



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2 and thickness = 0,7 mm.

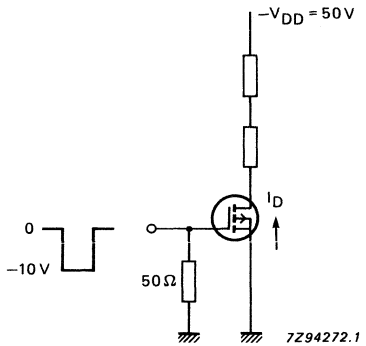


Fig.2 Switching times test circuit.

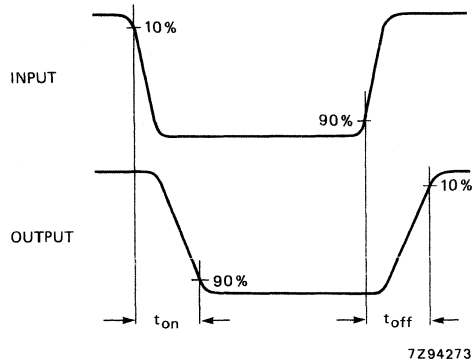


Fig.3 Input and output waveforms.

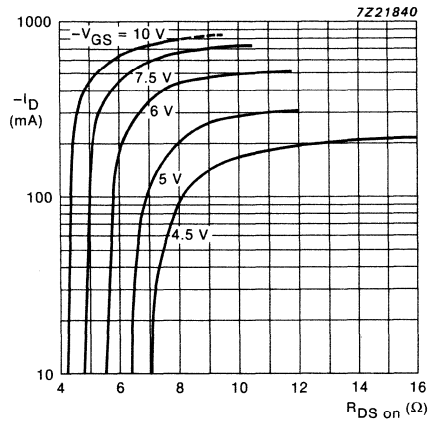


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

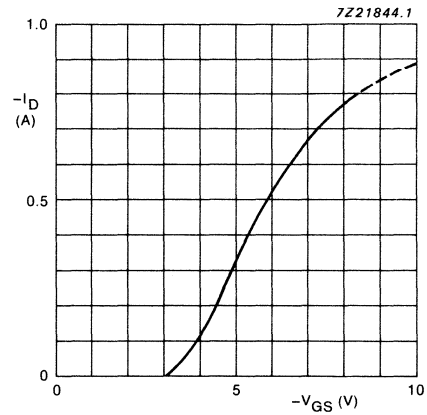


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

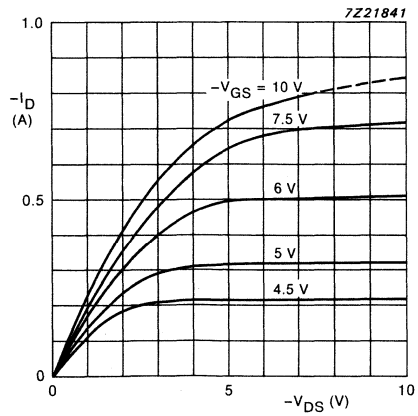


Fig.6 Output characteristics; T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0,25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ.	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS

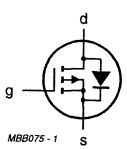
MECHANICAL DATA

Dimensions in mm

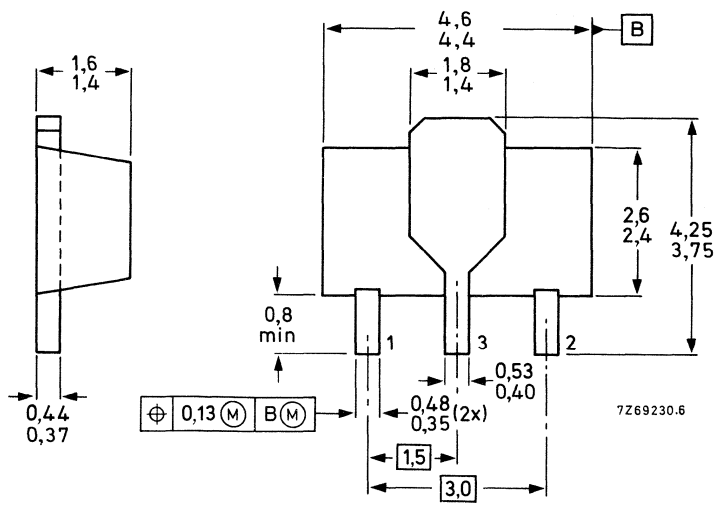
Fig. 1 SOT89.

Pinning:

1 = source
2 = gate
3 = drain



Marking: LN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ..	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2; thickness = 0,7 mm.

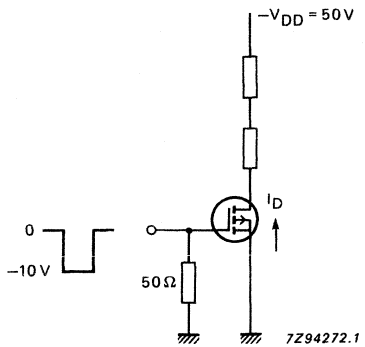


Fig. 2 Switching times test circuit.

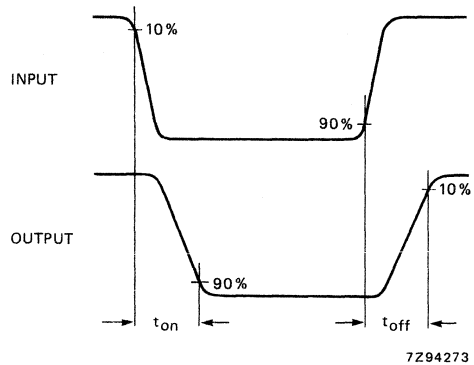


Fig. 3 Input and output waveforms.

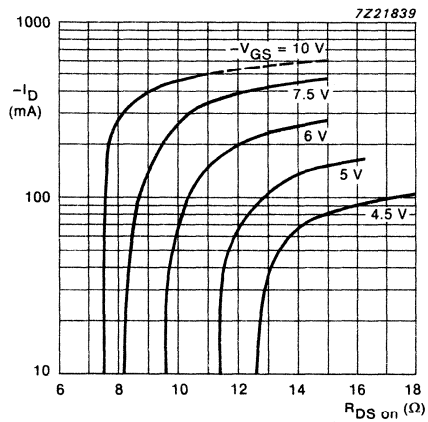


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

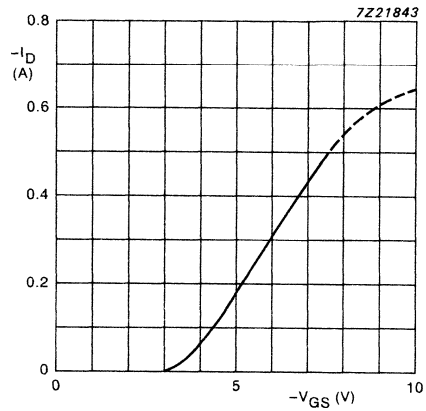


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

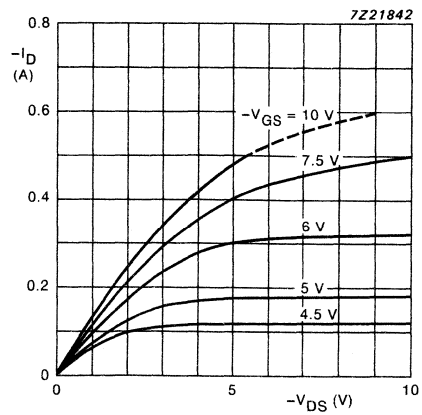


Fig.6 Output characteristics; T_j = 25 °C; typical values.

N-channel depletion mode vertical D-MOS transistors

BST124

FEATURES

- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel depletion mode vertical D-MOS transistor in a TO-126 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
I_D	DC drain current		–	450	mA
P_{tot}	total power dissipation	up to T_h = 120 °C	–	6	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	–1.65	–0.75	V

PINNING - TO-126

PIN	DESCRIPTION
1	source
2	drain
3	gate

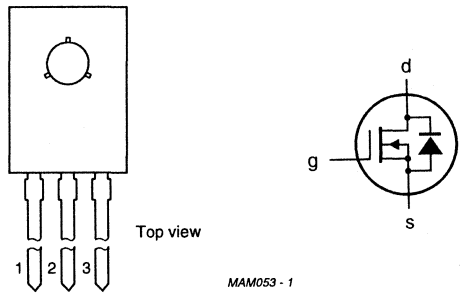


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	450	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	up to T_h = 120 °C	–	6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

N-channel depletion mode vertical D-MOS transistors

BST124

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}h}$	from junction to heatsink	5 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = −3 V	250	–	V
I_{DSX}	drain-source cut-off leakage current	V_{DS} = 200 V; V_{GS} = −3 V	–	100	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	100	nA
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 100 μA; V_{DS} = 60 V	−1.65	−0.75	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = 3 V	−1.4	−0.6	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 0	–	20	Ω
		I_D = 250 mA; V_{GS} = 5 V	–	12	Ω
I_{DSS}	drain saturation current	V_{DS} = 25 V; V_{GS} = 0	70	–	mA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = −3 V; f = 1 MHz	–	15	pF
Switching times (see Figs 2 and 3)					
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = −3 to +5 V	–	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = +5 to −3 V	–	30	ns

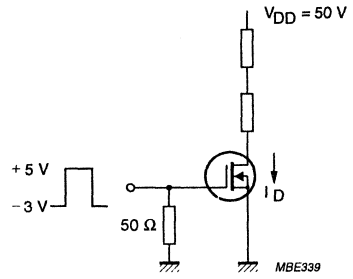


Fig.2 Switching times test circuit.

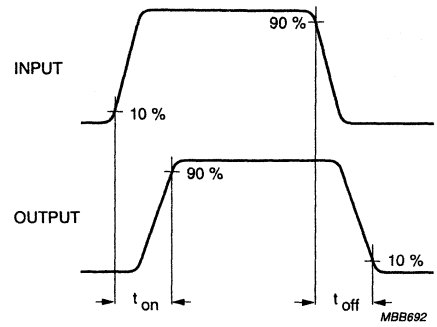


Fig.3 Input and output waveforms.

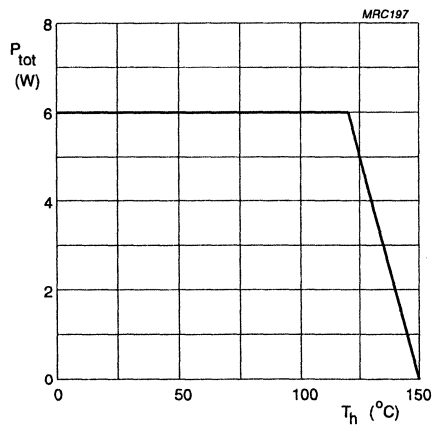
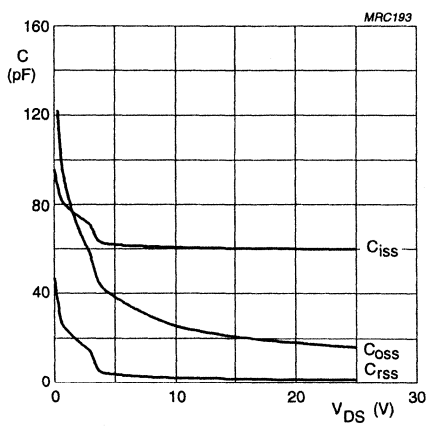


Fig.4 Power derating curve.

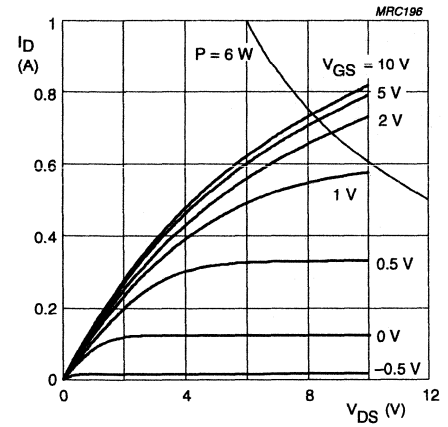


V_{GS} = −3 V; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.

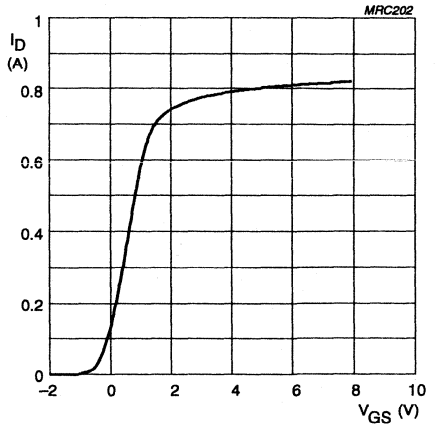
N-channel depletion mode vertical D-MOS transistors

BST124



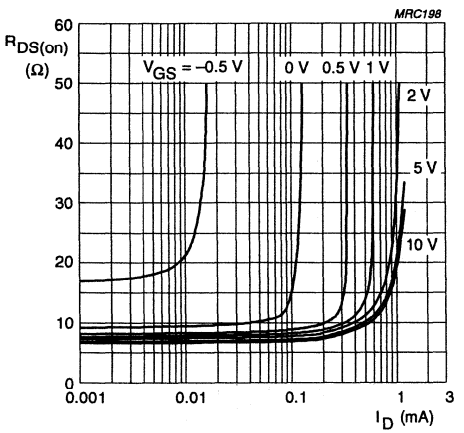
T_j = 25 °C.

Fig.6 Typical output characteristics.



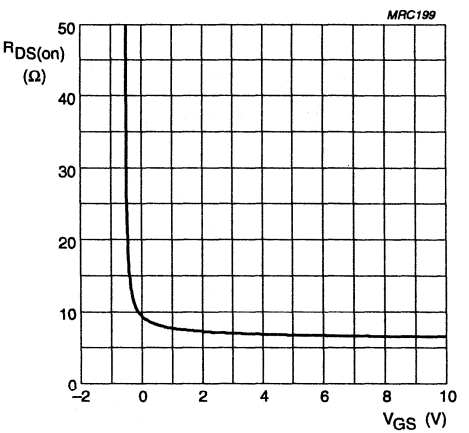
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



I_D = 10 mA; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

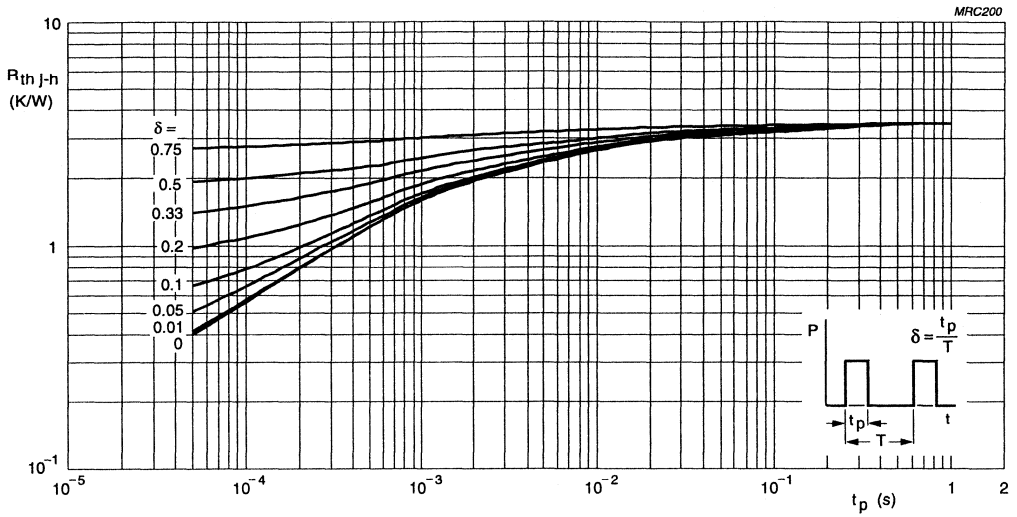
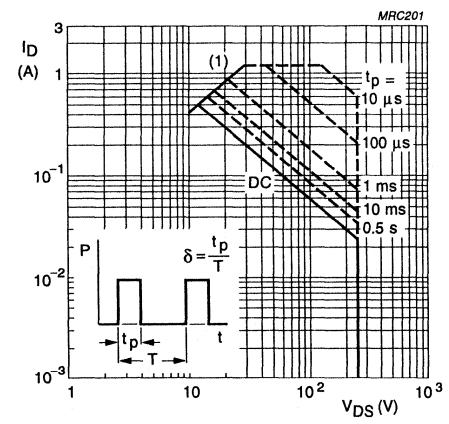


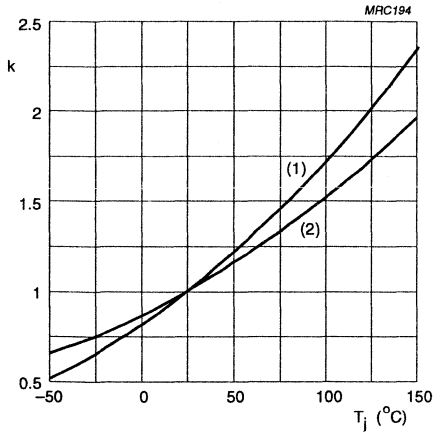
Fig.10 Transient thermal resistance from junction to heatsink as a function of pulse time; typical values.



δ = 0.01; T_{amb} = 25 °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.



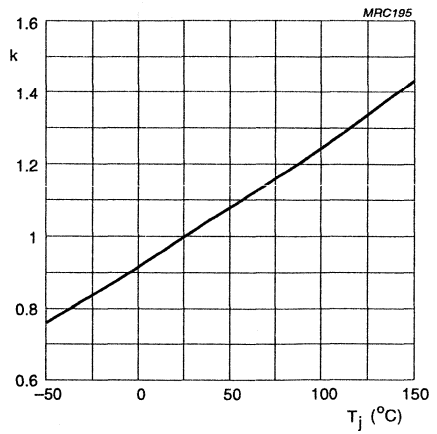
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

Typical $R_{DS(on)}$:

(1) I_D = 250 mA; V_{GS} = 5 V.

(2) I_D = 20 mA; V_{GS} = 0.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

Typical $V_{GS(th)}$ at I_D = 1 mA; V_{DS} = 3 V.

Fig.13 Temperature coefficient gate-source threshold voltage.

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		350		mW
			BSV78	**BSV79**	**BSV80**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage I_D = 1 nA; V_{GS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

MECHANICAL DATA

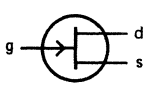
Dimensions in mm

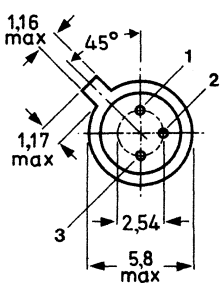
Fig. 1 TO-18.

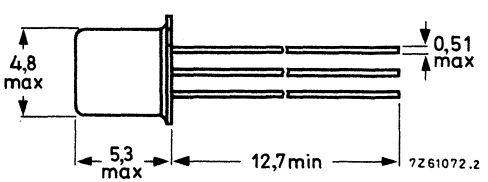
Gate connected to case

Pinning

1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (open source)	V_{DGO}	max.	40 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40 V
Forward gate current	I_G	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350 mW
Storage temperature range	T_{stg}	−65 to +	175 °C
Operating junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSV78	BSV79	BSV80	
Gate cut-off currents						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<		0.25		nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<		0.5		μA
Drain cut-off current						
V_{DS} = 15 V; $-V_{GS}$ = 12 V	I_{DSX}	<		0.25		nA
V_{DS} = 15 V; $-V_{GS}$ = 12 V; T_j = 150 °C	I_{DSX}	<		0.5		μA
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
I_D = 1.5 μA; V_{DS} = 15 V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	500			mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<		400		mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<			325	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS}$ = 10 V; V_{DS} = 0						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	C_{rs}	<	5	5	5	pF

Switching times (see Fig. 2)

Turn-on time when switched from
$-V_{GSoff}$ = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V (**BSV78**)
$-V_{GSoff}$ = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V (**BSV79**)
$-V_{GSoff}$ = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V (**BSV80**)

Turn-off time when switched from
I_{Don} = 20 mA to $-V_{GSMoff}$ = 11 V; V_{DD} = 10 V (**BSV78**)
I_{Don} = 10 mA to $-V_{GSMoff}$ = 7 V; V_{DD} = 10 V (**BSV79**)
I_{Don} = 5 mA to $-V_{GSMoff}$ = 5 V; V_{DD} = 10 V (**BSV80**)

		BSV78	BSV79	BSV80	
delay time	t_d <	5	10	10	ns
rise time	t_r <	5	8	20	ns
turn-on time	t_{on} <	10	18	30	ns
fall time	t_f <	6	11	24	ns
storage time	t_s <	4	5	8	ns
turn-off time	t_{off} <	10	16	32	ns

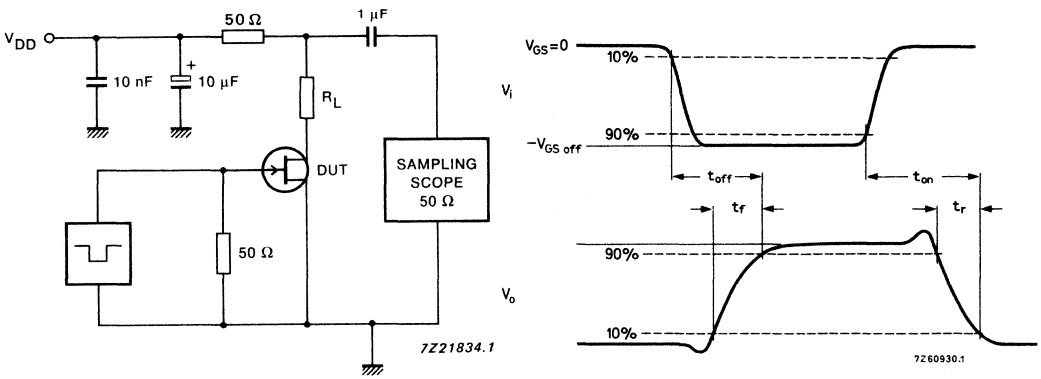
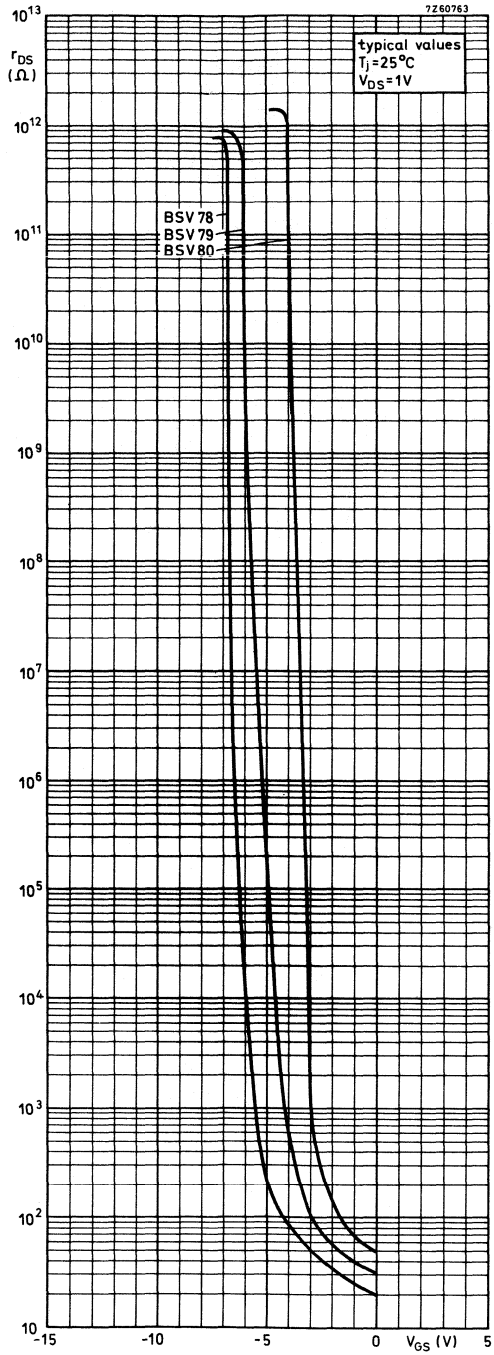


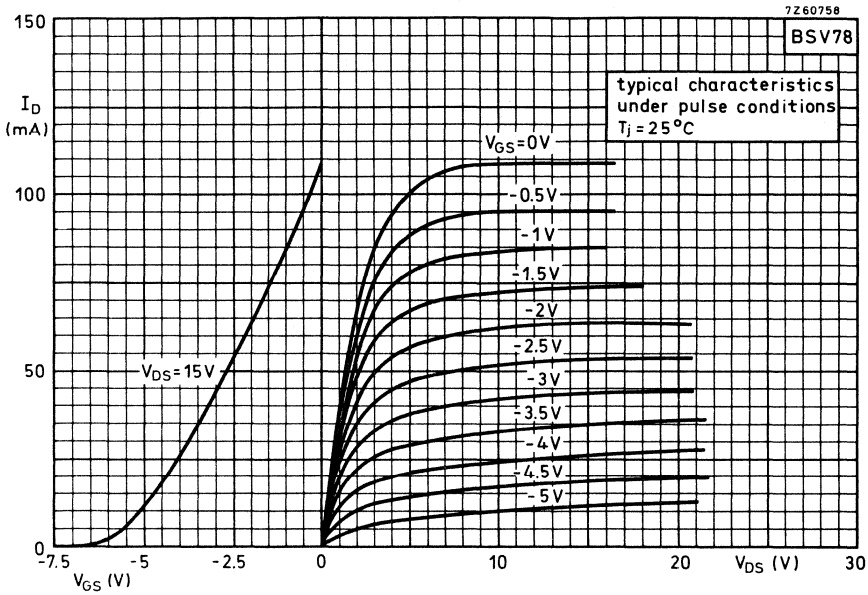
Fig. 2 Switching times test circuit and input and output waveforms.

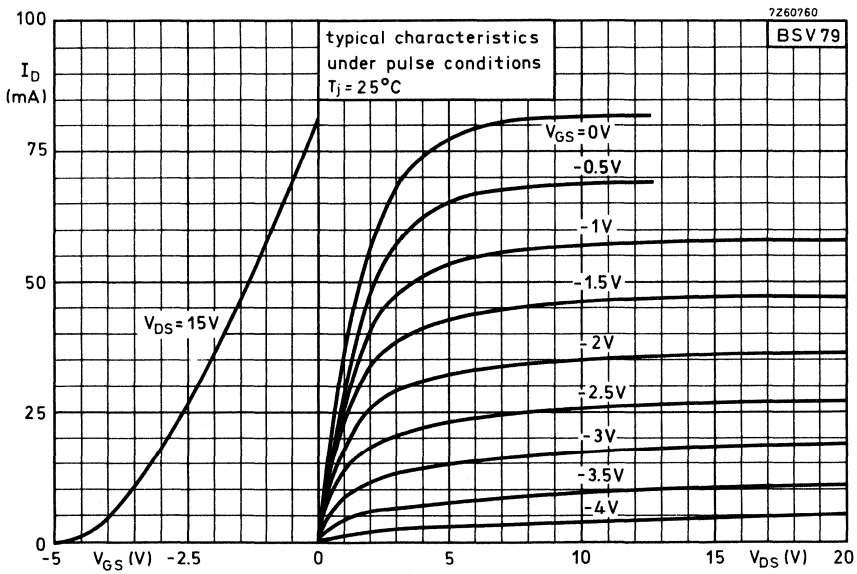
	BSV78	BSV79	BSV80	
R_L =	424	909	1885	Ω

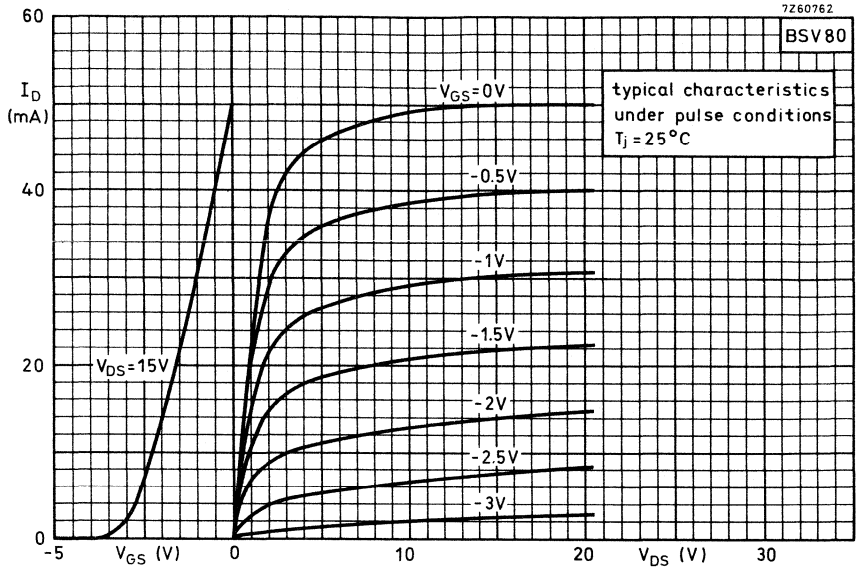
Pulse generator:
R_i = 50 Ω
t_r < 0.5 ns
t_f < 5 ns

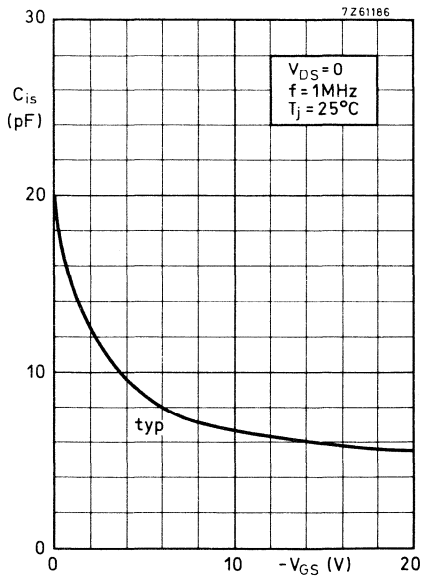
Oscilloscope:
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns

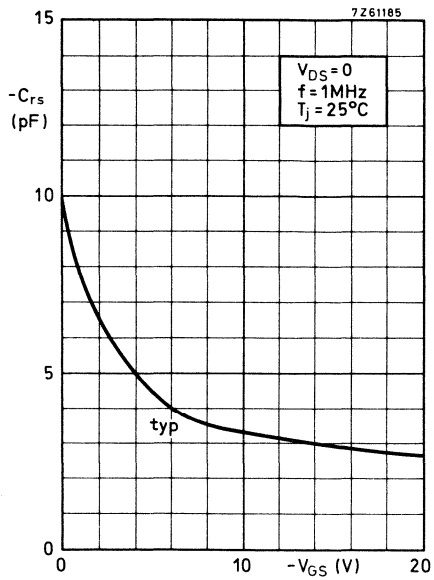

7Z60763
typical values
T_j=25°C
V_{DS}=1V
r_{DS} (Ω)
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
BSV 78
BSV 79
BSV 80
-15
-10
-5
0
V_{GS} (V)
5

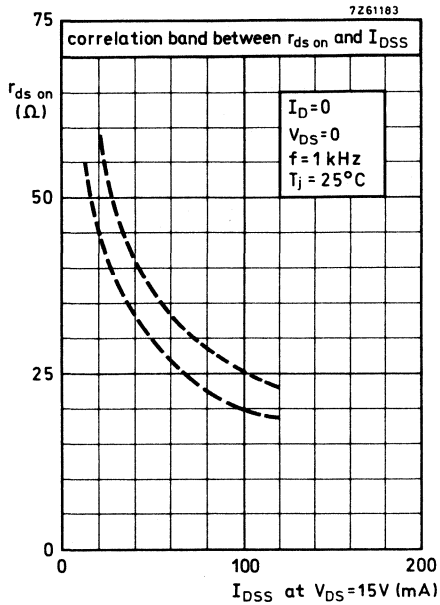

7Z60758
BSV78
typical characteristics
under pulse conditions
$T_j = 25°C$
I_D (mA)
150
100
50
0
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
-4.5V
-5V
V_{DS}=15V
-7.5
-5
-2.5
0
10
20
30
V_{GS} (V)
V_{DS} (V)

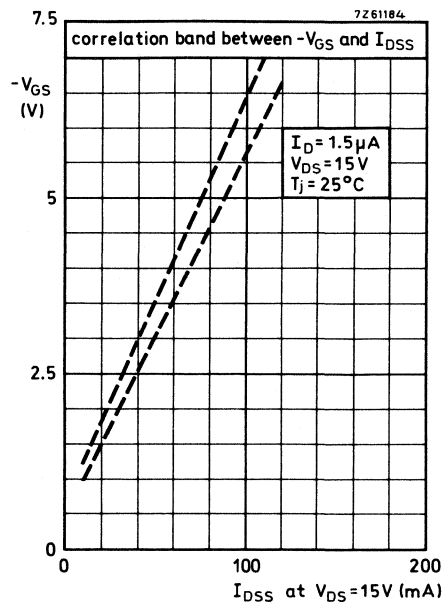

7Z60760
BSV79
typical characteristics
under pulse conditions
$T_j = 25°C$
I_D (mA)
100
75
50
25
0
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
V_{DS}=15V
-5
-2.5
0
5
10
15
20
V_{GS} (V)
V_{DS} (V)


7Z60762
BSV80
typical characteristics
under pulse conditions
T_j = 25 °C
I_D (mA)
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
V_{DS}=15V
60
40
20
0
-5
V_{GS} (V)
0
10
20
V_{DS} (V)
30


7Z61186
V_{DS} = 0
f = 1MHz
T_j = 25°C
C_{is} (pF)
30
20
10
0
typ
0
10
$-V_{GS}$ (V)
20


7Z61185
V_{DS} = 0
f = 1MHz
T_j = 25°C
$-C_{rs}$ (pF)
15
10
5
0
typ
0
10
$-V_{GS}$ (V)
20


7Z61183
correlation band between $r_{ds\ on}$ and I_{DSS}
$r_{ds\ on}$ (Ω)
75
50
25
0
I_D=0
V_{DS}=0
f=1 kHz
T_j=25°C
0
100
200
I_{DSS} at V_{DS}=15V (mA)


7Z61184
correlation band between $-V_{GS}$ and I_{DSS}
$-V_{GS}$ (V)
7.5
5
2.5
0
I_D=1.5μA
V_{DS}=15V
T_j=25°C
0
100
200
I_{DSS} at V_{DS}=15V (mA)

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

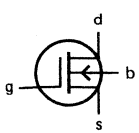
Drain-source resistance (on) at f = 1 kHz			
V_{DS} = 0; V_{GS} = 5 V; V_{BS} = 0	$R_{ds\ on}$	max.	50 Ω
Drain-source resistance (off)			
V_{DS} = 10 V; $-V_{GS}$ = 5 V; V_{BS} = 0	$R_{DS\ off}$	min.	10 GΩ
Feedback capacitance at f = 1 MHz			
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	typ.	0.5 pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	typ.	0.5 pF

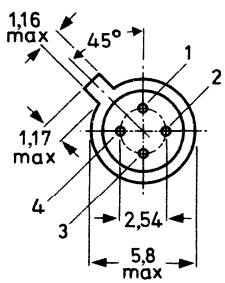
MECHANICAL DATA

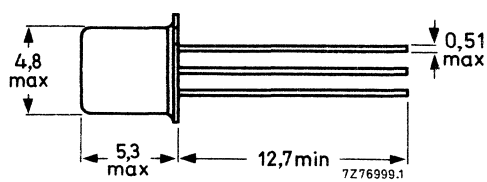
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	V_{GB}	max. min.	10 V −10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 V −15 V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	V_{G-N}	max. min.	50 V −50 V
Drain current (DC)	I_D	max.	25 mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0.1$	I_{DM}	max.	50 mA
Source current (peak value) $t_p = 20$ ms; $\delta = 0.1$	I_{SM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 125 °C
Junction temperature	T_j	max.	125 °C

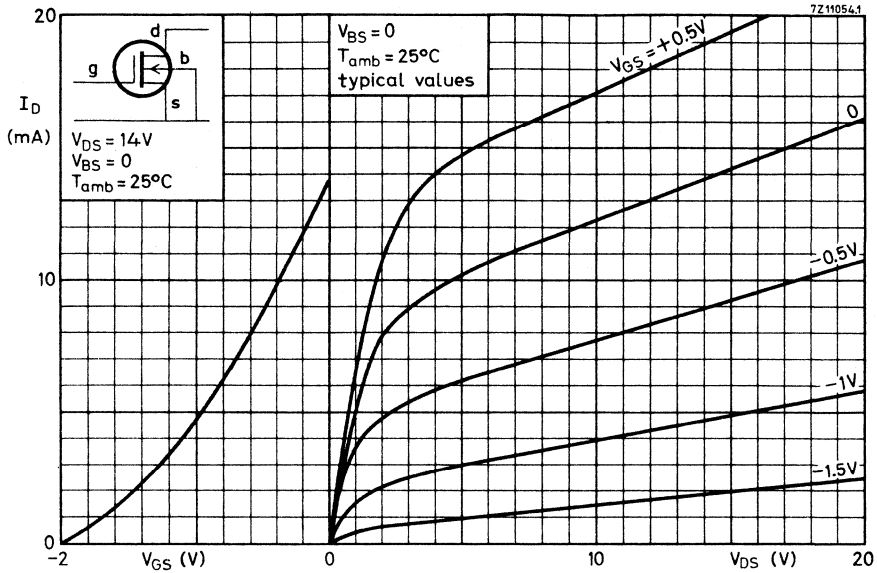
THERMAL RESISTANCE

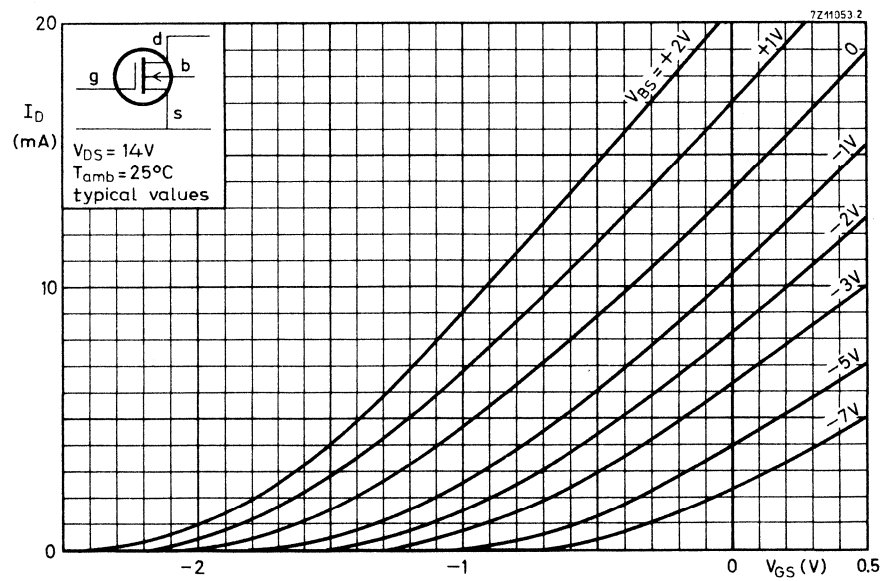
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500 K/W

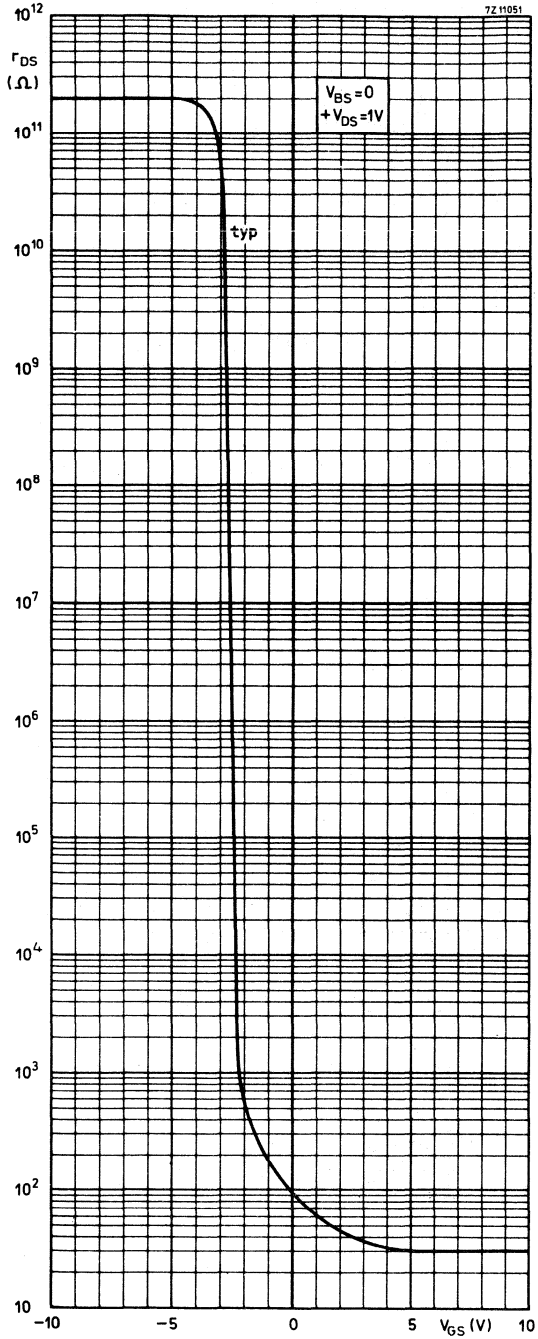
CHARACTERISTICS

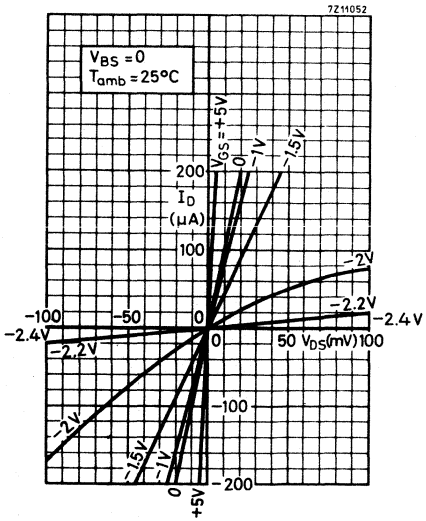
T_j = 25 °C unless otherwise specified

Drain cut-off currents; V_{BS} = 0				
V_{DS} = 10 V; $-V_{GS}$ = 5 V	I_{DSX}	<	1	nA
V_{DS} = 10 V; $-V_{GS}$ = 5 V; T_j = 125 °C	I_{DSX}	<	1	µA
Source cut-off currents; V_{BD} = 0				
V_{SD} = 10 V; $-V_{GD}$ = 5 V	I_{SDX}	<	1	nA
V_{SD} = 10 V; $-V_{GD}$ = 5 V; T_j = 125 °C	I_{SDX}	<	1	µA
Gate currents; V_{BS} = 0				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	10	pA
V_{GS} = 10 V; V_{DS} = 0	I_{GSS}	<	10	pA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	<	200	pA
V_{GS} = 10 V; V_{DS} = 0; T_j = 125 °C	I_{GSS}	<	200	pA
Bulk currents; V_{GB} = 0				
$-V_{BD}$ = 30 V; I_S = 0	$-I_{BDO}$	<	10	µA
$-V_{BS}$ = 30 V; I_D = 0	$-I_{BSO}$	<	10	µA
Drain-source resistance (on) at f = 1 kHz; V_{BS} = 0				
V_{GS} = 0 ; V_{DS} = 0	$R_{ds\ on}$	<	100	Ω
V_{GS} = 0 ; V_{DS} = 0; T_j = 125 °C	$R_{ds\ on}$	<	150	Ω
$+V_{GS}$ = 5 V; V_{DS} = 0	$R_{ds\ on}$	<	50	Ω
Drain-source resistance (off)				
$-V_{GS}$ = 5 V; V_{DS} = 10 V; V_{BS} = 0	$R_{DS\ off}$	>	10	GΩ
Feedback capacitances at f = 1 MHz				
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	typ.	0.5	pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	typ.	0.5	pF
Gate to all other terminals capacitance at f = 1 MHz				
$-V_{GB}$ = 5 V; V_{SB} = V_{DB} = 0	$C_{g\text{-}n}$	<	6	pF


7Z11054.1
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
V_{BS} = 0
T_{amb} = 25°C
V_{BS} = 0
T_{amb} = 25°C
typical values
V_{GS} = +0.5V
0
−0.5V
−1V
−1.5V
−2
V_{GS} (V)
0
10
V_{DS} (V)
20


7Z11053.2
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
T_{amb} = 25°C
typical values
V_{BS} = +2V
+1V
0
−1V
−2V
−3V
−5V
−7V
−2
−1
0
V_{GS} (V)
0.5


7Z11051
10^{12}
r_{DS} (Ω)
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
$V_{BS}=0$
$+V_{DS}=1V$
typ
−10
−5
0
5
V_{GS} (V)
10


7Z11052
$V_{BS}=0$
$T_{amb}=25°C$
$V_{GS}=+5V$
0
−1V
−1.5V
200
I_D (μA)
100
−2V
−2.2V
−2.4V
−100
−50
0
50
V_{DS}(mV)100
−2.4V
−2.2V
−2V
−1.5V
−1V
0
+5V
−100
−200

N-channel junction FETs J108; J109; J110

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (<8 Ω for J108).

DESCRIPTION

Silicon symmetrical N-channel junction FETs in a TO-92 envelope. Intended for use in applications such as analog switches, choppers and commutators.

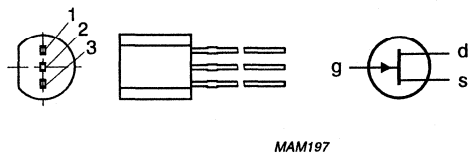


Fig.1 Simplified outline and symbol.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C	-	400	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	250	K/W

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS} = 10$ V $V_{DS} = 5$ V		-	3	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	J108 J109 J110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ μA $V_{DS} = 0$		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ μA $V_{DS} = 5$ V	J108 J109 J110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	J108 J109 J110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (J108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (J109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (J110).

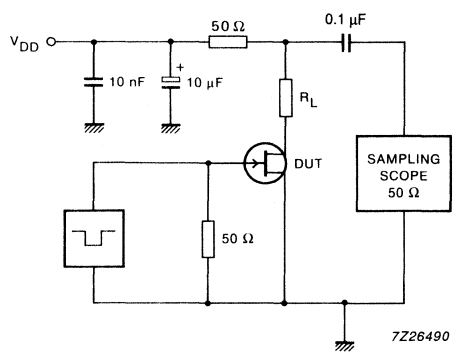


Fig.2 Switching circuit.

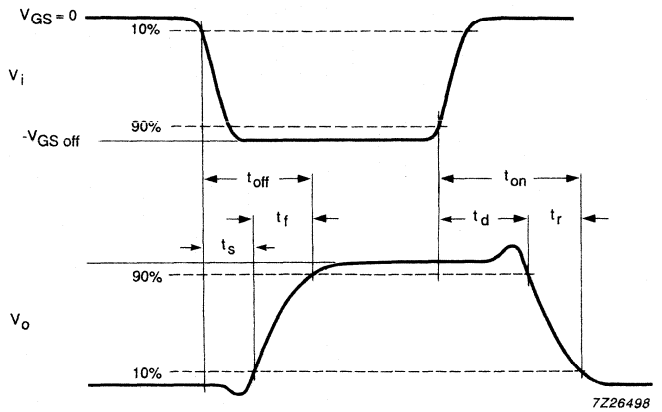


Fig.3 Input and output waveforms.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

Features

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS\ on}$ at zero gate voltage

QUICK REFERENCE DATA

			J111	J112	J113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	400	400	mW
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min. max.	3 10	1 5	0.5 3	V V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

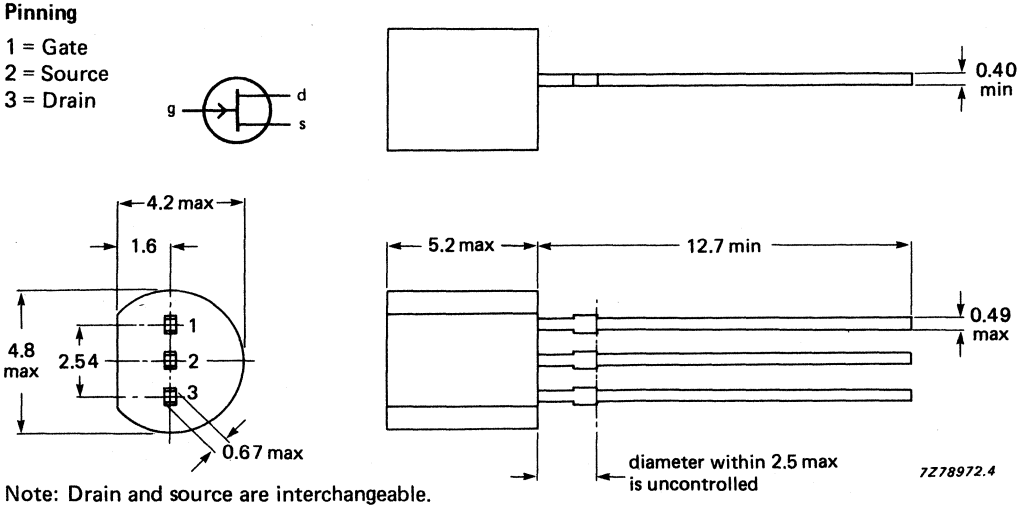
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92.

Pinning

1 = Gate
2 = Source
3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Gate forward current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J111	J112	J113	
Gate reverse current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	1	1	1	nA
Drain cut-off current V_{DS} = 5 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	max.	1	1	1	nA
Drain saturation current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{is}	typ.	6 pF
V_{DS} = $-V_{GS}$ = 0; f = 1 MHz	C_{is}	typ.	22 pF
		max.	28 pF
Feedback capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{rs}	typ.	3 pF
Switching times			
test conditions			
V_{DD} = 10 V; V_{GS} = 0 to V_{GSoff}			
$-V_{GS\ off}$ = 12 V; R_L = 750 Ω for J111			
$-V_{GS\ off}$ = 7 V; R_L = 1550 Ω for J112			
$-V_{GS\ off}$ = 5 V; R_L = 3150 Ω for J113			
Rise time	t_r	typ.	6 ns
Turn-on time	t_{on}	typ.	13 ns
Fall time	t_f	typ.	15 ns
Turn-off time	t_{off}	typ.	35 ns

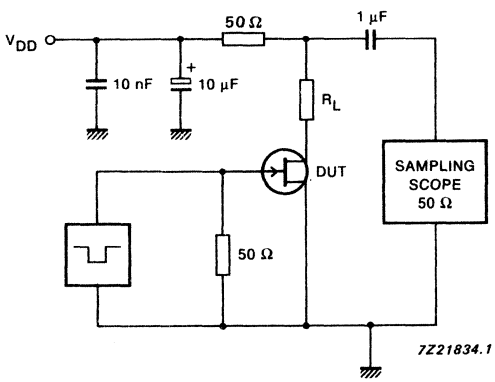


Fig.2 Switching times test circuit.

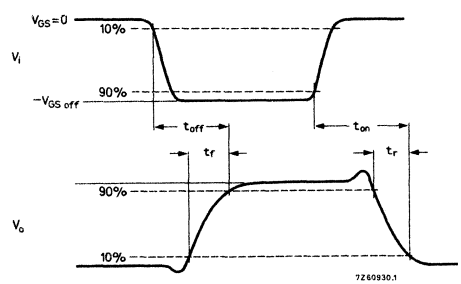


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

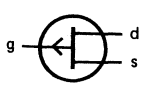
Drain-source voltage	$\pm V_{DS}$	max.		30			V
Gate-source voltage	V_{GSO}	max.		30			V
Gate current	$-I_G$	max.		50			mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.		400			mW
			J174	**J175**	**J176**	**J177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	max.	85	125	250	300	Ω

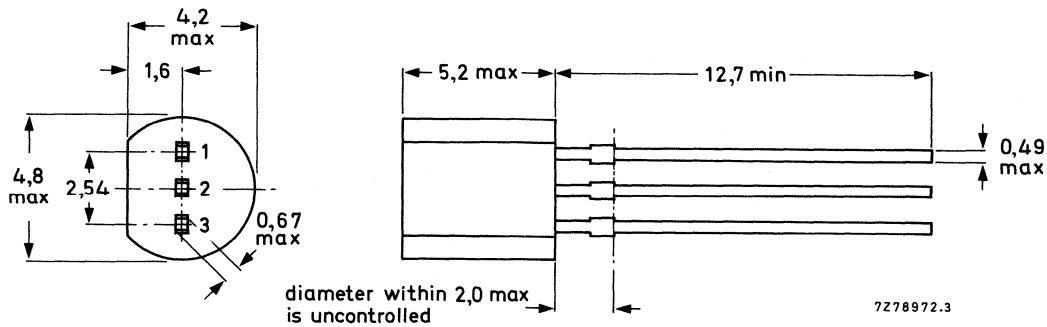
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:
1 = Source
2 = Gate
3 = Drain





Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J174	J175	J176	J177	
Gate cut-off current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSX}$	max.	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	min.	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\,off}$	min.	5	3	1	0.8	V
		max.	10	6	4	2.25	V
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	R_{DSon}	max.	85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
V_{GS} = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
V_{GS} = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
V_{GS} = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)			J174	J175	J176	J177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

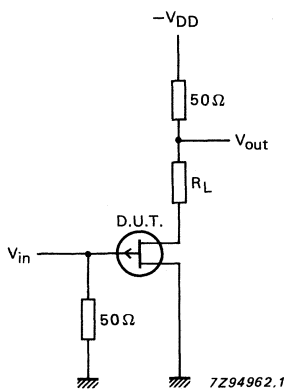


Fig. 2 Switching times test circuit.

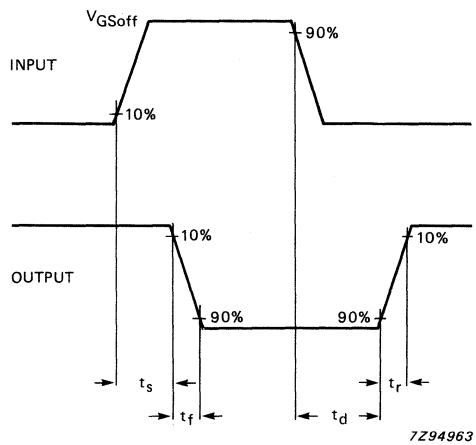


Fig. 3 Input and output waveforms;
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$.

N-channel silicon field-effect transistors

J308/309/310

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-92 envelope. They are intended for use in the AM input stage in car radios and in UHF/VHF amplifiers, oscillators and mixers.

PIN CONFIGURATION

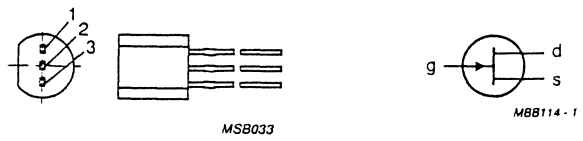


Fig.1 Simplified outline and symbol.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	J308		12	60	mA
	J309		12	30	mA
	J310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 µA			
	J308		1	6.5	V
	J309		1	4	V
	J310		2	6.5	V
Y_{fs}	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	250	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead minimum 10 x 10 mm

STATIC CHARACTERISTICS

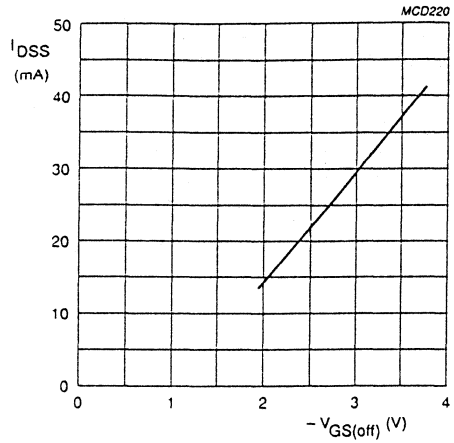
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	25	–		V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	J308		12	–	60	mA
	J309		12	–	30	mA
	J310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	J308		1	–	6.5	V
	J309		1	–	4	V
	J310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\lvert Y_{fs} \rvert$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\lvert Y_{os} \rvert$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

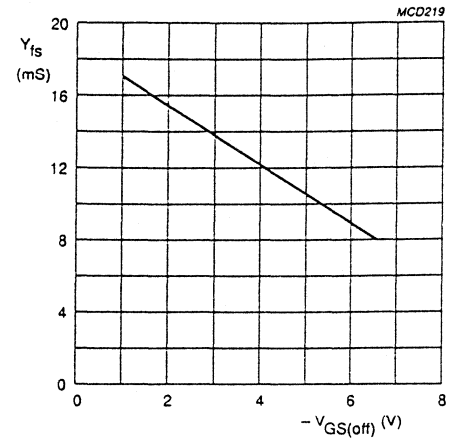
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\bar{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

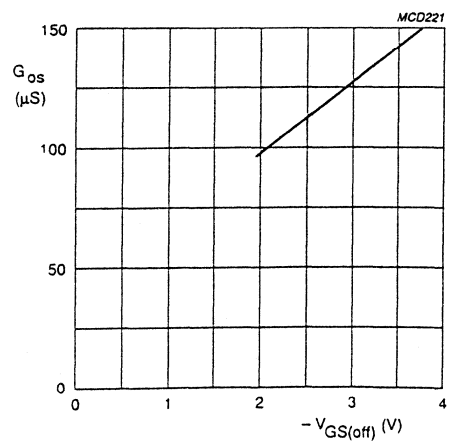
Fig.2 Drain current as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

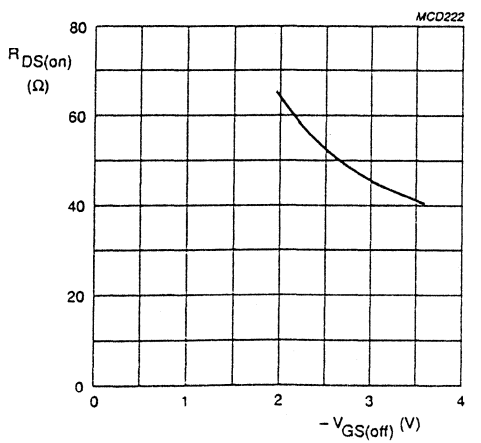
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

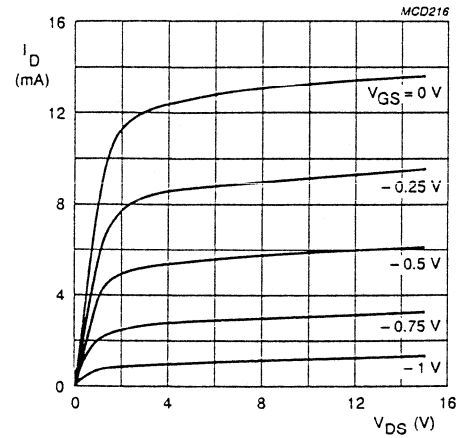
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

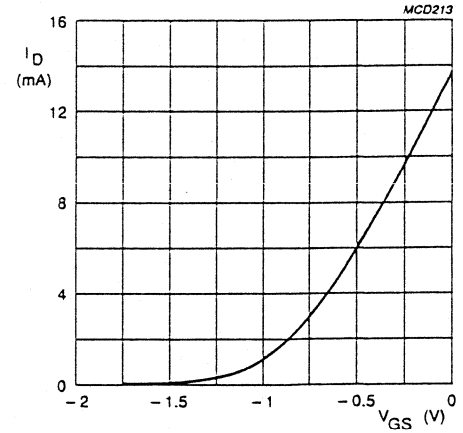
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



J308.

T_j = 25 °C.

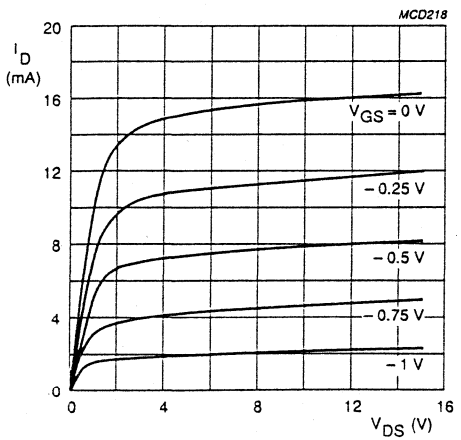
Fig.6 Output characteristics, typical values.



J308.

V_{DS} = 10 V; T_j = 25 °C.

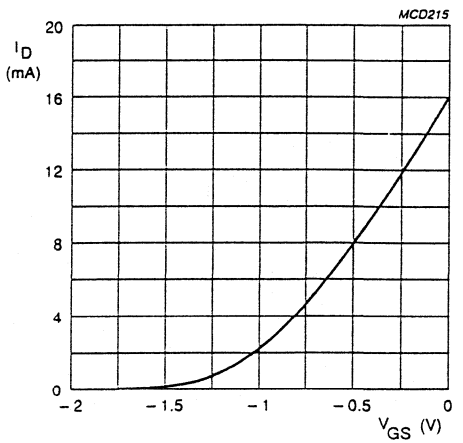
Fig.7 Input characteristics, typical values.



J309.

T_j = 25 °C.

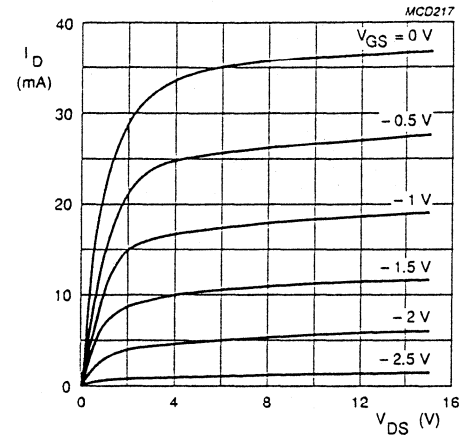
Fig.8 Output characteristics, typical values.



J309.

V_{DS} = 10 V; T_j = 25 °C.

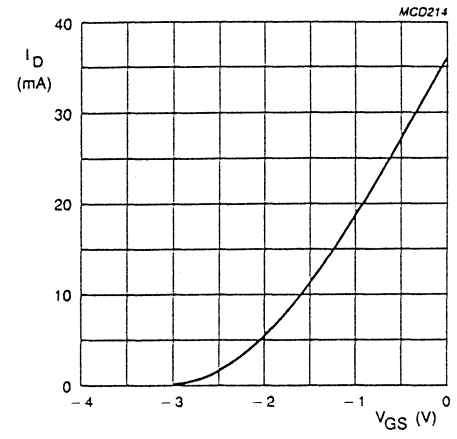
Fig.9 Input characteristics, typical values.



J310.

T_j = 25 °C.

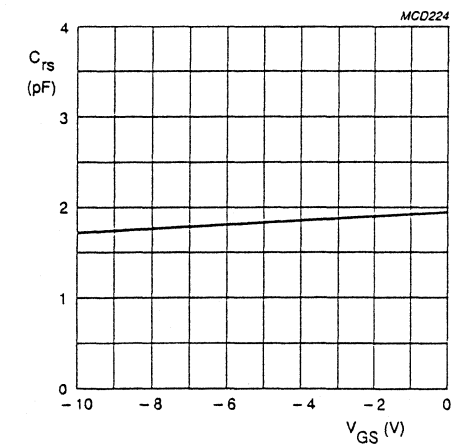
Fig.10 Output characteristics, typical values.



J310.

V_{DS} = 10 V; T_j = 25 °C.

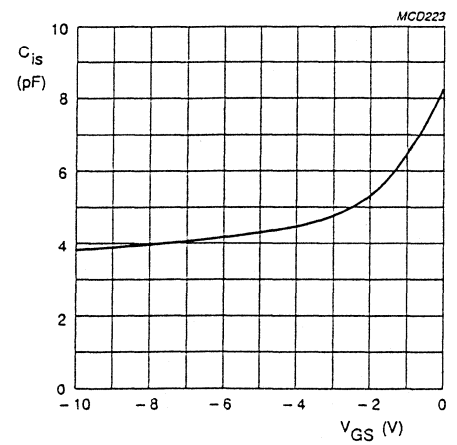
Fig.11 Input characteristics, typical values.



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

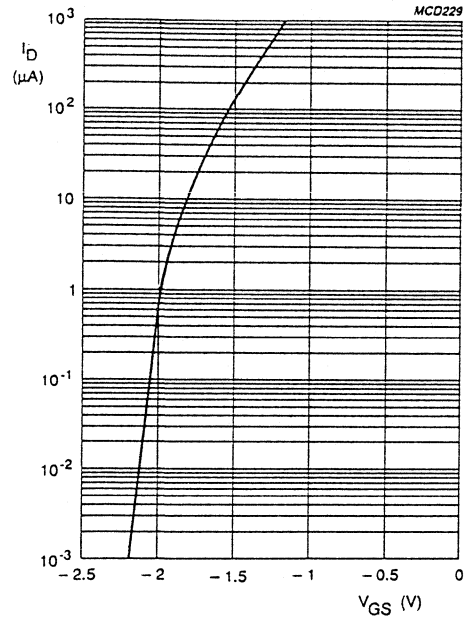
Fig.12 Feedback capacitance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

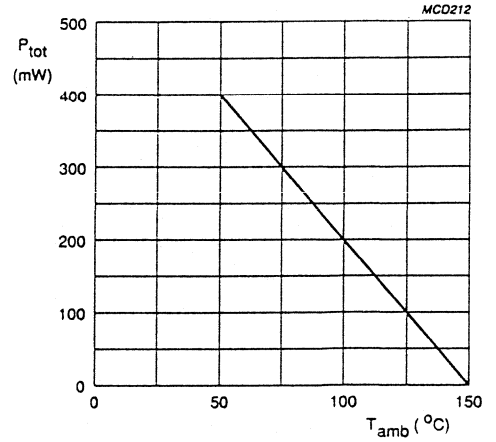
Fig.13 Input capacitance, typical values.



J308, 309 & 310.

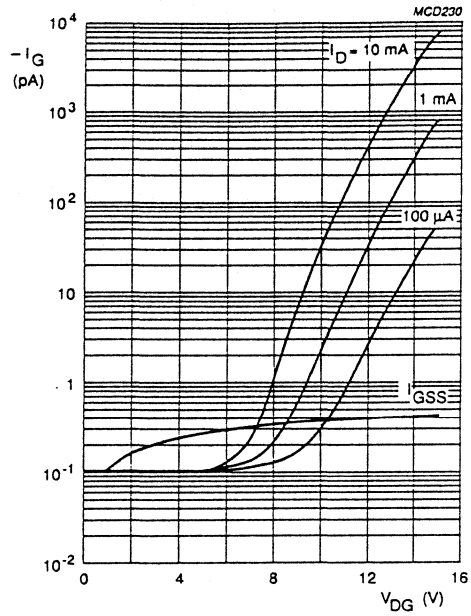
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



J308, 309 & 310.

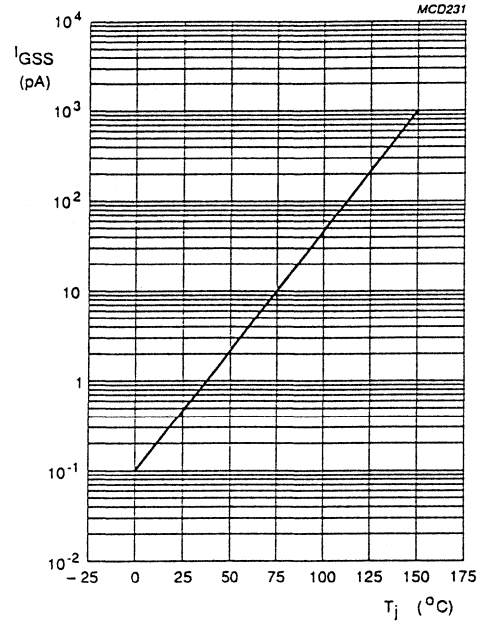
Fig.15 Power derating curve.



J308, 309 & 310.

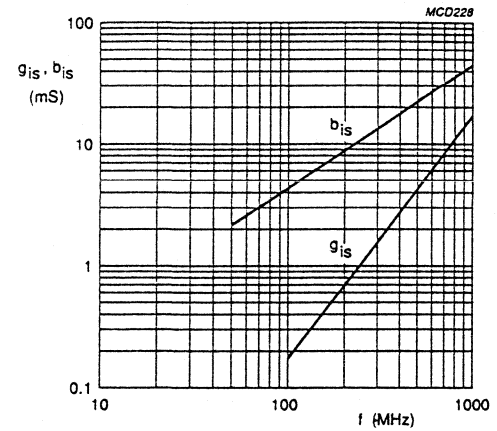
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



J308, 309 & 310.

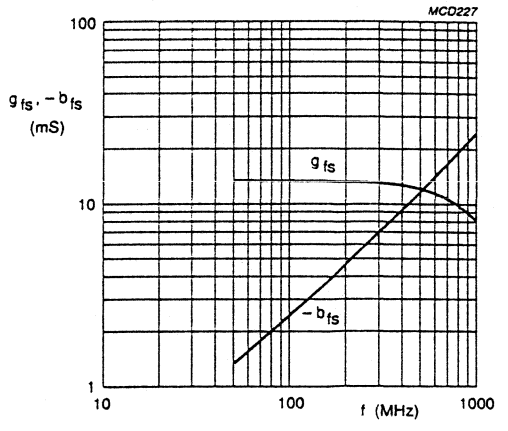
Fig.17 Gate current as a function of junction temperature, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

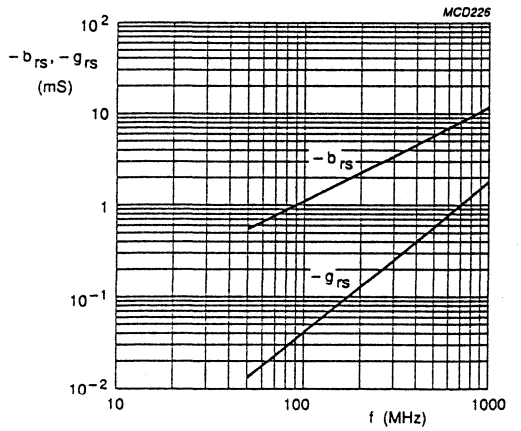
Fig.18 Input admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

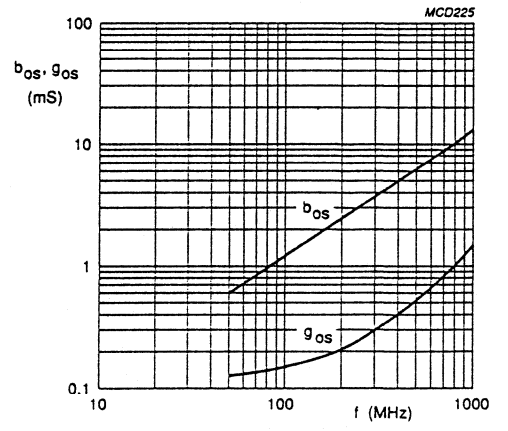
Fig.19 Forward admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

Complementary enhancement mode MOS transistors

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FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying etc.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

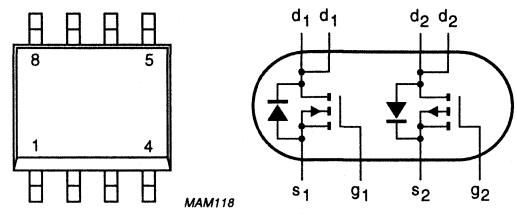


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	I_S = 1.25 A	–	1.2	V
	P-channel	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–1	–2.8	V
I_D	drain current (DC)				
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 2.2 A	–	0.1	Ω
	P-channel	V_{GS} = –10 V; I_D = –1 A	–	0.25	Ω
P_{tot}	total power dissipation	up to T_s = 80 °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80°C$			
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
I_{DM}	peak drain current	note 1			
	N-channel		–	14	A
	P-channel		–	–10	A
P_{tot}	total power dissipation	up to T_s = 80 °C; note 2	–	2	W
		up to T_{amb} = 25 °C; note 3	–	2	W
		up to T_{amb} = 25 °C; note 4	–	1	W
		up to T_{amb} = 25 °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80°C$			
	N-channel		–	1.5	A
	P-channel		–	–1.25	A
I_{SM}	peak pulsed source current	note 1			
	N-channel		–	6	A
	P-channel		–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 2 W at the same time).
3. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

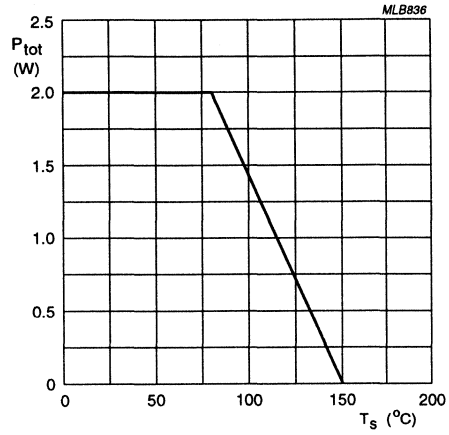
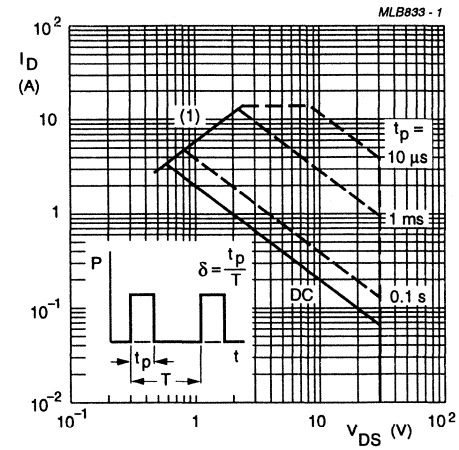
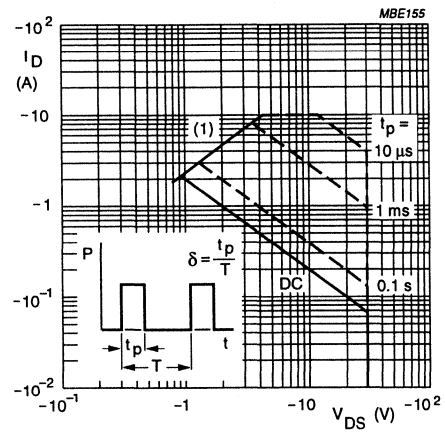


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR; N-channel.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.4 DC SOAR; P-channel.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = –10 μA	–30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
	P-channel	V_{GS} = V_{DS}; I_D = –1 mA	–1	–	–2.8	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = –24 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
I_{Don}	on-state drain current					
	N-channel	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
	P-channel	V_{GS} = –10 V; V_{DS} = –1 V	–2.3	–	–	A
		V_{GS} = –4.5 V; V_{DS} = –5 V	–1	–	–	A
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
	P-channel	V_{GS} = –4.5 V; I_D = – 0.5 A	–	0.33	0.4	Ω
		V_{GS} = –10 V; I_D = –1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance					
	N-channel	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
	P-channel	V_{DS} = –20 V; I_D = –1 A	1	2	–	S
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	140	–	pF

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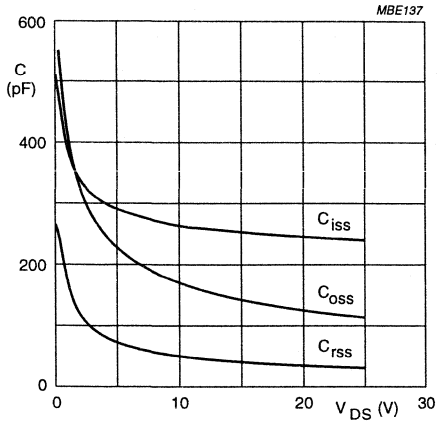
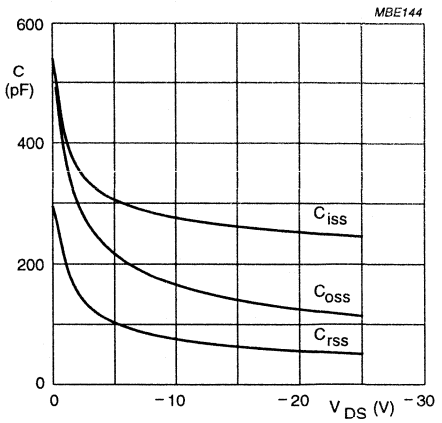
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	10	25	nC
Q_{gs}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	3	–	nC
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
	P-channel	V_{GS} = 0 to –10 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
	P-channel	V_{GS} = –10 to 0 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GS} = 0; I_S = 1.25 A	–	–	1.2	V
	P-channel	V_{GS} = 0; I_S = –1.25 A	–	–	–1.6	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = 100 A/µs	–	35	100	ns
	P-channel	I_S = –1.25 A; di/dt = 100 A/µs	–	150	200	ns



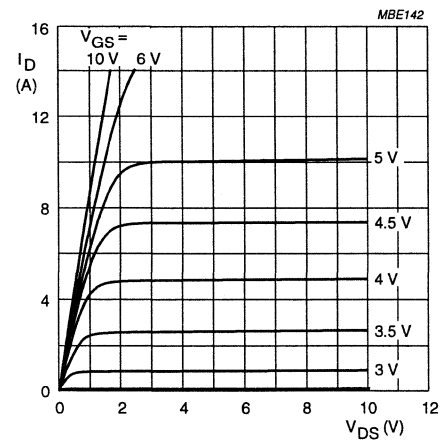
V_{GS} = 0.
T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage; N-channel; typical values.



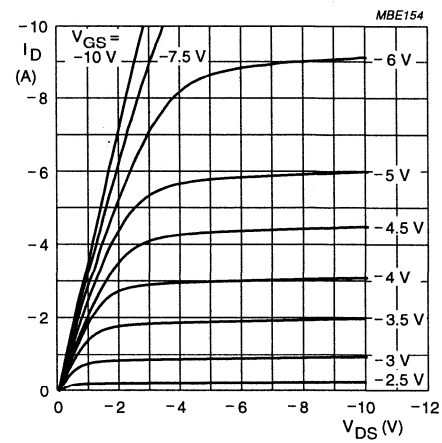
V_{GS} = 0.
T_j = 25 °C.

Fig.6 Capacitance as a function of drain source voltage; P-channel; typical values.



T_j = 25 °C.

Fig.7 Typical output characteristics; N-channel.



T_j = 25 °C.

Fig.8 Typical output characteristics; P-channel.

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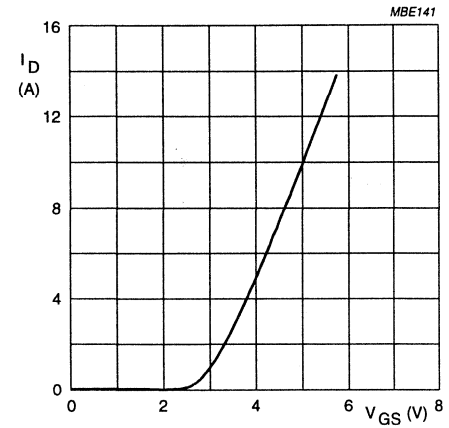
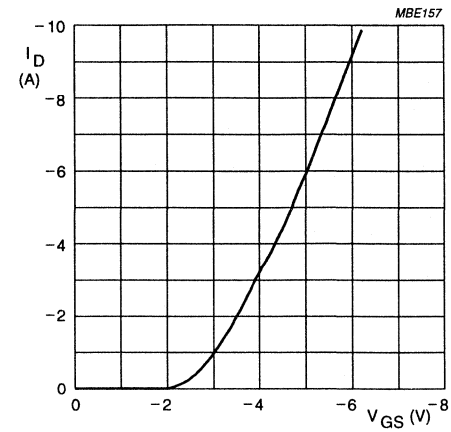


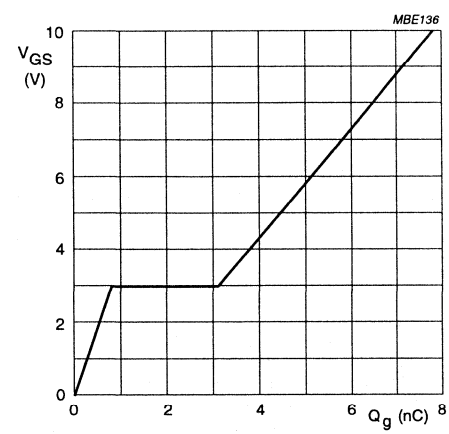
V_{DS} = 10 V.
T_j = 25 °C.

Fig.9 Typical transfer characteristics; N-channel.



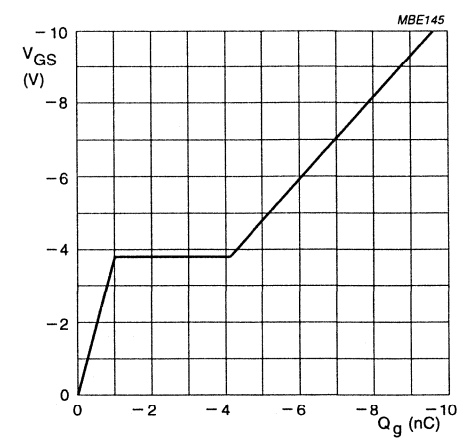
V_{DS} = −10 V.
T_j = 25 °C.

Fig.10 Typical transfer characteristics; P-channel.



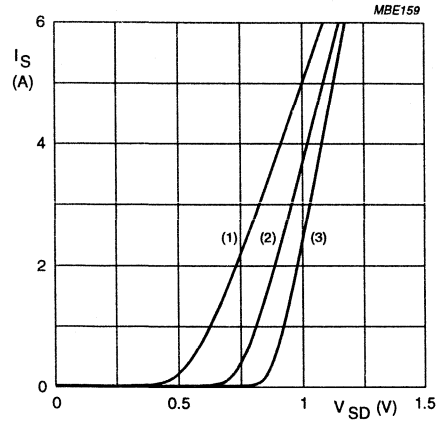
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.11 Gate-source voltage as a function of total gate charge; N-channel.



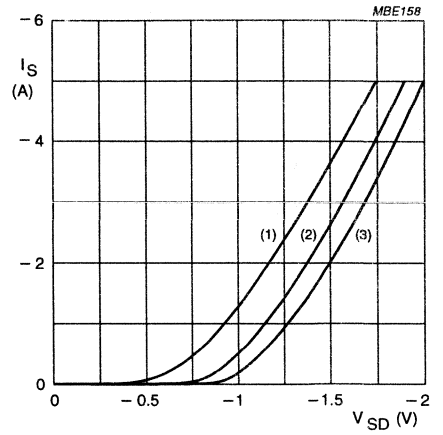
V_{DD} = −15 V.
I_D = −2.3 A.

Fig.12 Gate-source voltage as a function of total gate charge; P-channel.



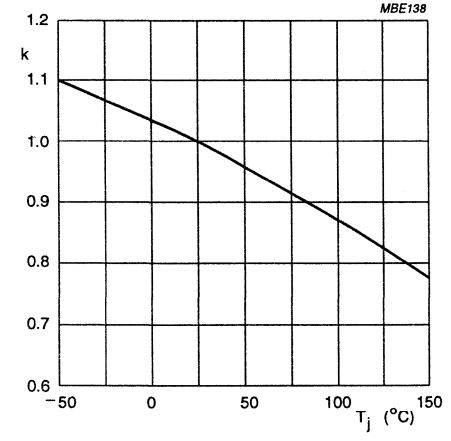
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.13 Source current as a function of source-drain diode forward voltage; N-channel.



V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

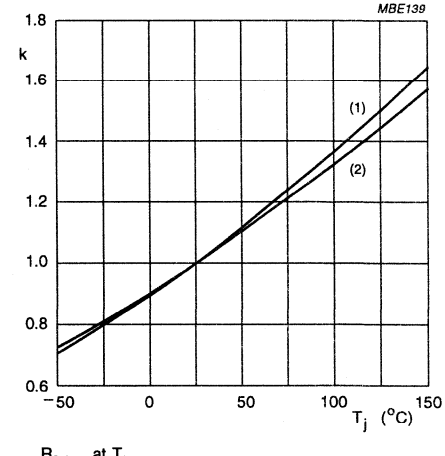
Fig.14 Source current as a function of source-drain diode forward voltage; P-channel.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = 1 mA; V_{DS} = V_{GS} = V_{th}.

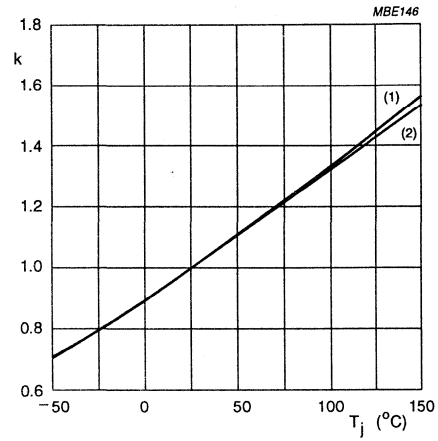
Fig.15 Temperature coefficient of gate-source threshold voltage; N and P-channels.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) I_D = 2.2 A; V_{GS} = 10 V.
(2) I_D = 1 A; V_{GS} = 4.5 V.

Fig.16 Temperature coefficient of drain-source on-resistance; N-channel.



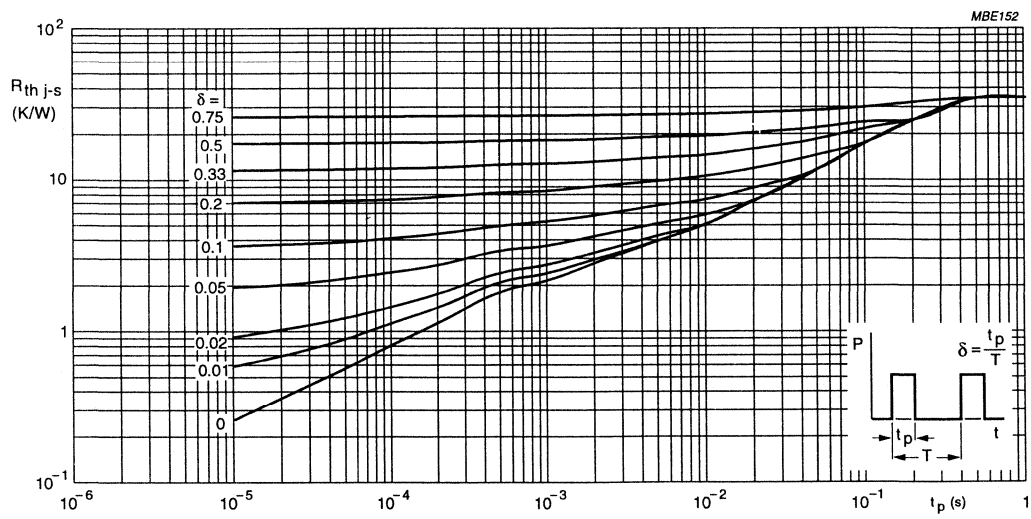
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:

(1) $I_D = -1$ A; $V_{GS} = -10$ V.

(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.17 Temperature coefficient of drain-source on-resistance; P-channel.



Solder point temperature $T_s = 80$ °C.

Fig.18 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

N-channel enhancement mode MOS transistor

PHN105

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

OBJECTIVE
See Philips Semiconductors for further information

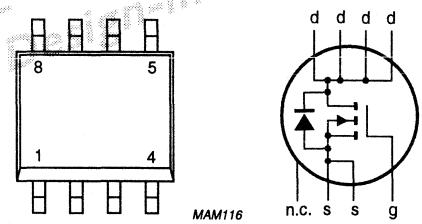


Fig.1 Simplified outline and symbol.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

CAUTION

The device is supplied in an antistatic package.
The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)		–	4.8	A
R_{DSon}	drain-source on-state resistance	I_D = 5.5 A; V_{GS} = 10 V	–	0.05	Ω
P_{tot}	total power dissipation	up to T_s = 80 °C	–	2	W

N-channel enhancement mode MOS transistor

PHN105

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	20	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	4.8	A
I_{DM}	peak drain current	note 1	–	20	A
P_{tot}	total power dissipation	up to $T_s = 80$ °C	–	2	W
		up to $T_{amb} = 25$ °C; note 2	–	2	W
		up to $T_{amb} = 25$ °C; note 3	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	1.5	A
I_{SM}	peak pulsed source current	note 1	–	12	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
3. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

N-channel enhancement mode MOS transistor

PHN105

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	20	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 15 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 5 V	7	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2 A	–	–	0.1	Ω
		V_{GS} = 10 V; I_D = 4.4 A	–	–	0.05	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = 10 V; I_D = 1 A	tbf	–	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	–	tbf	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	–	tbf	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	–	tbf	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DS} = 10 V; I_D = 1.8 A	–	–	tbf	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DS} = 10 V; I_D = 1.8 A	–	–	tbf	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 10 V; I_D = 1.8 A	–	–	tbf	nC
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 10 V; I_D = 1 A; R_L = 10 Ω	–	–	tbf	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 10 V; I_D = 1 A; R_L = 10 Ω	–	–	tbf	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GS} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	–	tbf	ns

N-channel enhancement mode MOS transistor

PHN110

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

OBJECTIVE
See Philips Semiconductors for design-in information

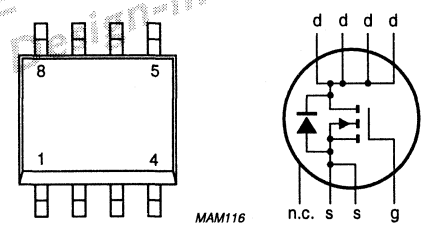


Fig.1 Simplified outline and symbol.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	up to T_s = 80 °C	–	2	W

N-channel enhancement mode MOS transistor

PHN110

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	up to $T_s = 80$ °C	–	2	W
		up to $T_{amb} = 25$ °C; note 2	–	2	W
		up to $T_{amb} = 25$ °C; note 3	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	1.5	A
I_{SM}	peak pulsed source current	note 1	–	6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
3. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

N-channel enhancement mode MOS transistor

PHN110

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GS} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns

Dual N-channel enhancement mode MOS transistor

PHN210

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SO8 (SOT96-1) package.

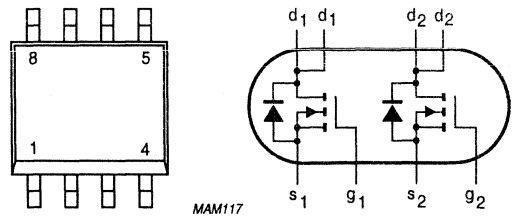


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	up to T_s = 80 °C	–	2	W

Dual N-channel enhancement mode MOS transistor

PHN210

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80°$ C	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	up to T_s = 80 °C; note 2	–	2	W
		up to T_{amb} = 25 °C; note 3	–	2	W
		up to T_{amb} = 25 °C; note 4	–	1	W
		up to T_{amb} = 25 °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	1.5	A
I_{SM}	peak pulsed source current	note 1	–	6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 2 W at the same time).
3. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

Dual N-channel enhancement mode MOS transistor

PHN210

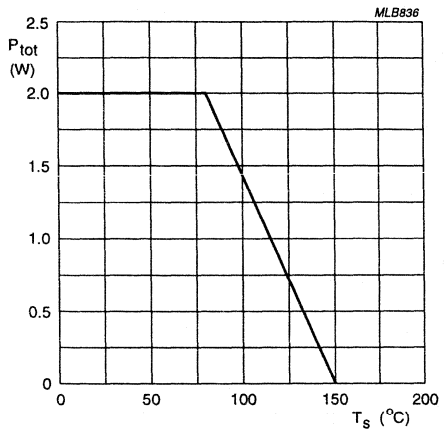
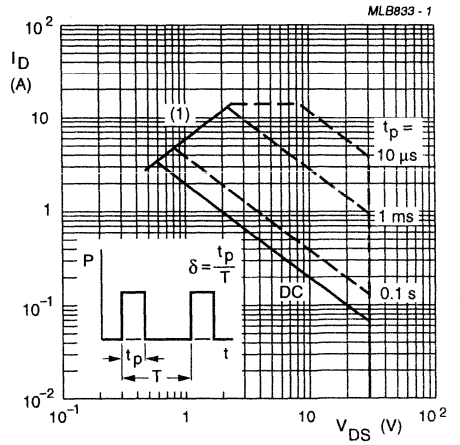


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR.

Dual N-channel enhancement mode MOS transistor

PHN210

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

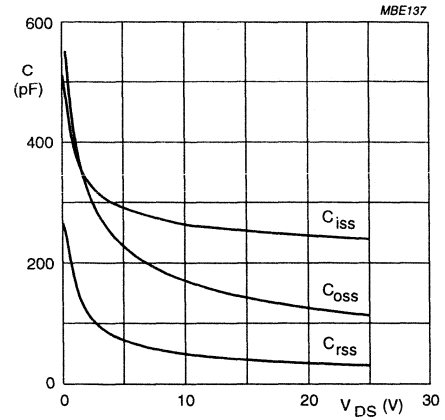
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GS} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns

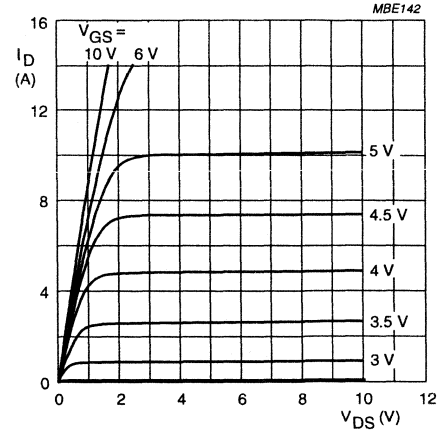
Dual N-channel enhancement mode MOS transistor

PHN210



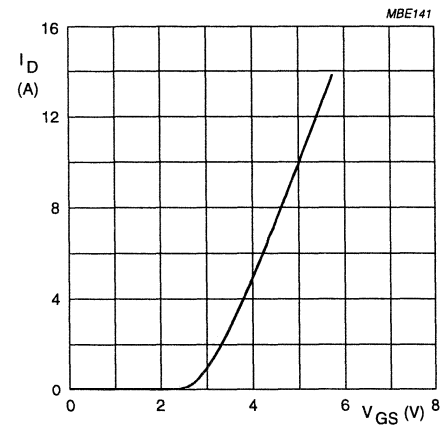
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



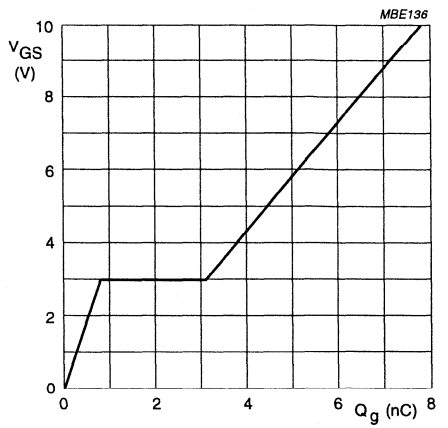
T_j = 25 °C.

Fig.5 Typical output characteristics.



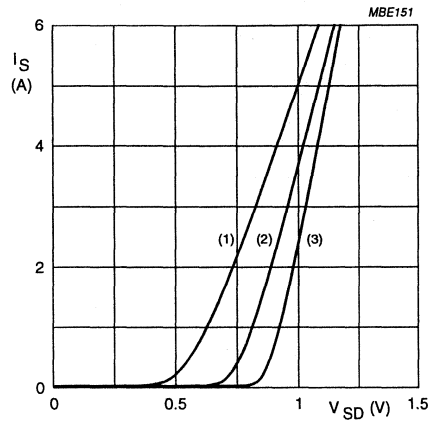
V_{DS} = 10 V.
T_j = 25 °C.

Fig.6 Typical transfer characteristics.



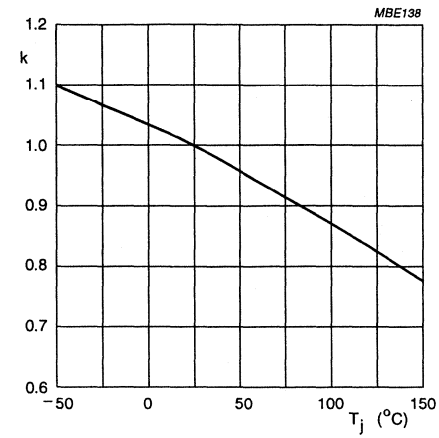
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.7 Gate-source voltage as a function of total gate charge.



$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

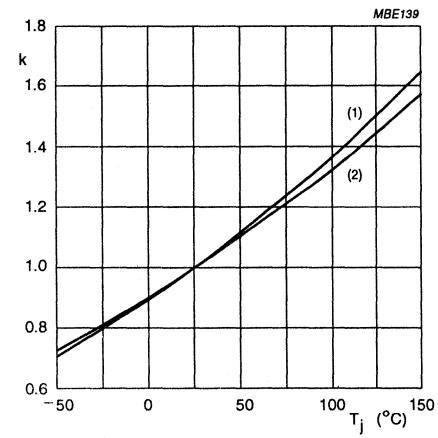
Fig.8 Source current as a function of source-drain diode forward voltage.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{th}$.

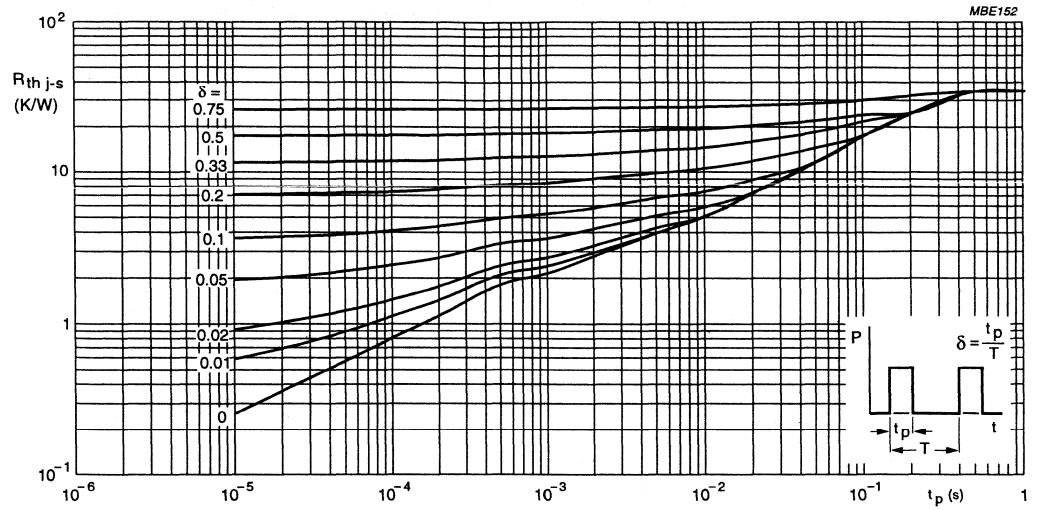
Fig.9 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) $I_D = -1$ A; $V_{GS} = -10$ V.
(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.10 Temperature coefficient of drain-source on-resistance.



Solder point temperature T_s = 80 °C.

Fig.11 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode MOS transistor

PHP112

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

OBJECTIVE
See Philips Semiconductors for preliminary information

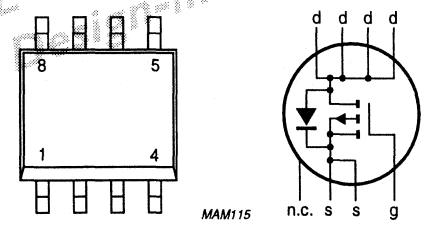


Fig.1 Simplified outline and symbol.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–20	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–3.1	A
R_{DSon}	drain-source on-state resistance	I_D = –4 A; V_{GS} = –10 V	–	0.12	Ω
P_{tot}	total power dissipation	up to T_s = 80 °C;	–	2	W

P-channel enhancement mode MOS transistor

PHP112

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–20	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	–3.1	A
I_{DM}	peak drain current	note 1	–	–14	A
P_{tot}	total power dissipation	up to $T_s = 80$ °C	–	2	W
		up to $T_{amb} = 25$ °C; note 2	–	2	W
		up to $T_{amb} = 25$ °C; note 3	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–10	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
3. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

P-channel enhancement mode MOS transistor

PHP112

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−20	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −15 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −5 V	−4.6	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1 A	–	–	0.24	Ω
		V_{GS} = −10 V; I_D = −2 A	–	–	0.12	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = −10 V; I_D = −2 A	tbf	–	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	–	tbf	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	–	tbf	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	–	tbf	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DS} = −10 V; I_D = −4 A	–	–	tbf	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DS} = −10 V; I_D = −4 A	–	–	tbf	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −10 V; I_D = −4 A	–	–	tbf	nC
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −10 V; I_D = −1 A; R_L = 10 Ω	–	–	tbf	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −10 V; I_D = −1 A; R_L = 10 Ω	–	–	tbf	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GS} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	–	tbf	ns

P-channel enhancement mode MOS transistor

PHP125

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

OBJECTIVE
See philips Semiconductors for pin-in information

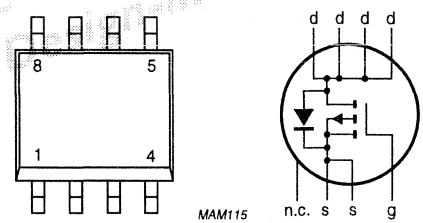


Fig.1 Simplified outline and symbol.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)		–	–2.3	A
R_{DSon}	drain-source on-state resistance	$I_D = -1$ A; $V_{GS} = -10$ V	–	0.25	Ω
P_{tot}	total power dissipation	up to $T_s = 80$ °C;	–	2	W

P-channel enhancement mode MOS transistor

PHP125

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	–2.3	A
I_{DM}	peak drain current	note 1	–	–10	A
P_{tot}	total power dissipation	up to $T_s = 80$ °C	–	2	W
		up to $T_{amb} = 25$ °C; note 2	–	2	W
		up to $T_{amb} = 25$ °C; note 3	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
3. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

P-channel enhancement mode MOS transistor

PHP125

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−2.3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GS} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns

Dual P-channel enhancement mode MOS transistor

PHP225

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectifying, etc.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SO8 (SOT96-1) package.

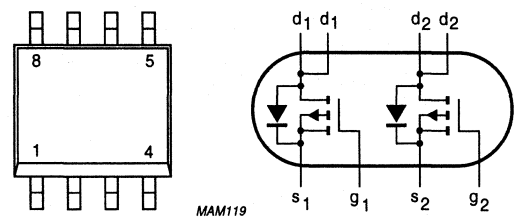


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)		–	–2.3	A
R_{DSon}	drain-source on-state resistance	$I_D = -1$ A; $V_{GS} = -10$ V	–	0.25	Ω
P_{tot}	total power dissipation	up to $T_s = 80$ °C;	–	2	W

Dual P-channel enhancement mode MOS transistor

PHP225

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	–2.3	A
I_{DM}	peak drain current	note 1	–	–10	A
P_{tot}	total power dissipation	up to $T_s = 80$ °C; note 2	–	2	W
		up to $T_{amb} = 25$ °C; note 3	–	2	W
		up to $T_{amb} = 25$ °C; note 4	–	1	W
		up to $T_{amb} = 25$ °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 2 W at the same time).
3. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on PCB with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

Dual P-channel enhancement mode MOS transistor

PHP225

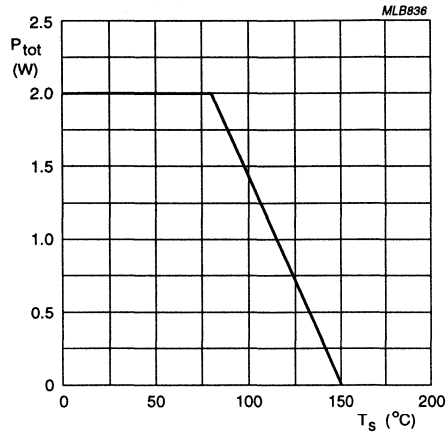
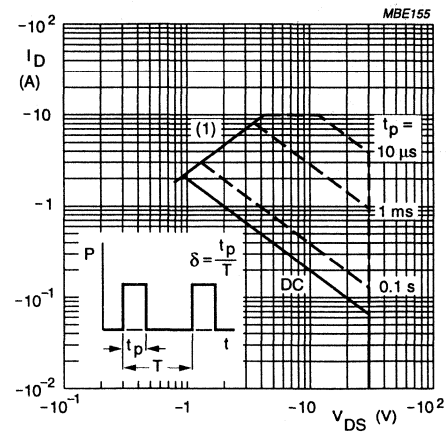


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 DC SOAR.

Dual P-channel enhancement mode MOS transistor

PHP225

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

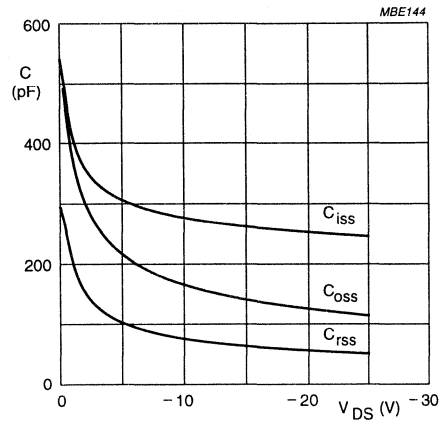
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−2.3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{DS}	source drain diode forward voltage	V_{GS} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns

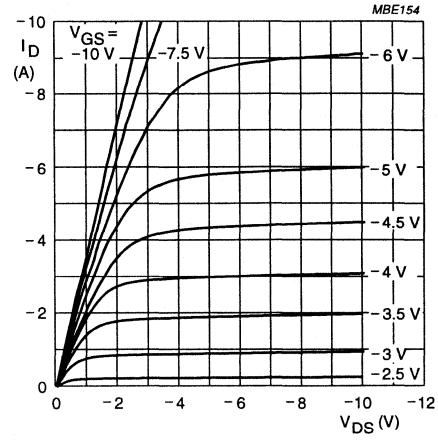
Dual P-channel enhancement mode MOS transistor

PHP225



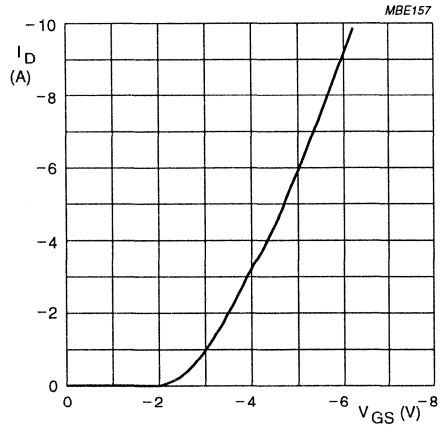
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



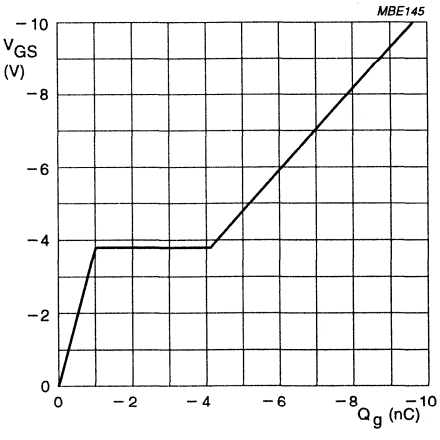
T_j = 25 °C.

Fig.5 Typical output characteristics.



V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Typical transfer characteristics.

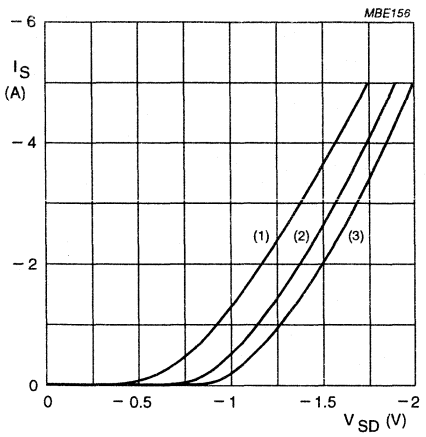


V_{DD} = −15 V.
I_D = −2.3 A.

Fig.7 Gate-source voltage as a function of total gate charge.

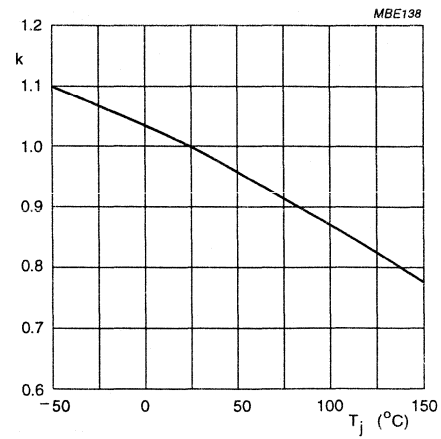
Dual P-channel enhancement mode MOS transistor

PHP225



$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

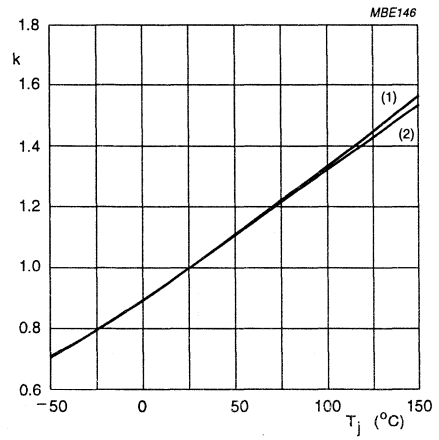
Fig.8 Source current as a function of source-drain diode forward voltage.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{th}$.

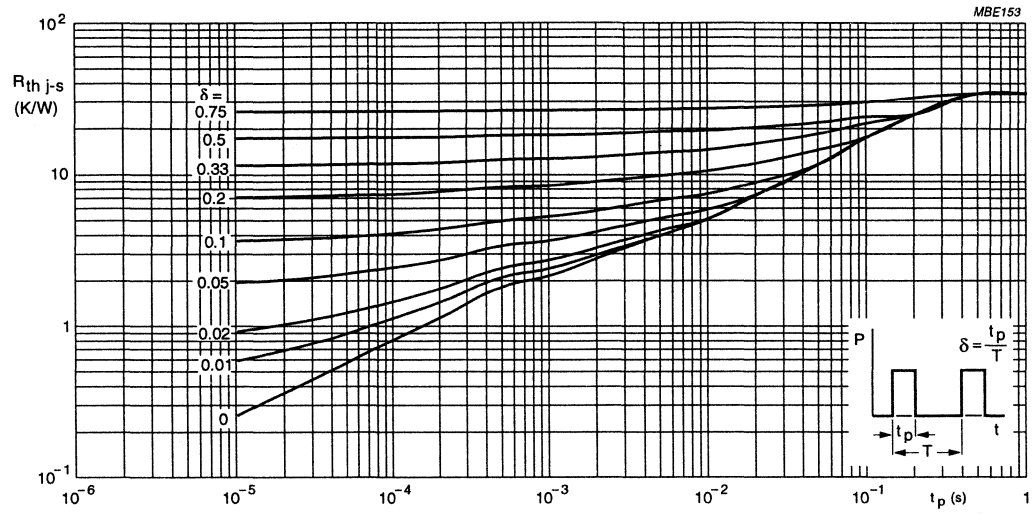
Fig.9 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) $I_D = -1$ A; $V_{GS} = -10$ V.
(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.10 Temperature coefficient of drain-source on-resistance.



Solder point temperature T_s = 80 °C.

Fig.11 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

PMBF107
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

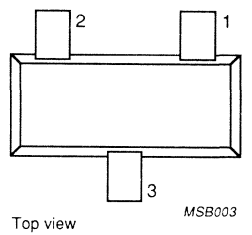
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	100	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	28	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.4	V

PIN CONFIGURATION



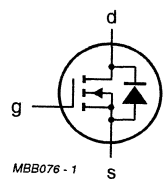


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printboard.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printboard.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain cut-off current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
		I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

PMBF107

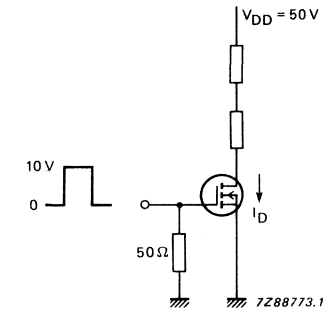


Fig.2 Switching time test circuit.

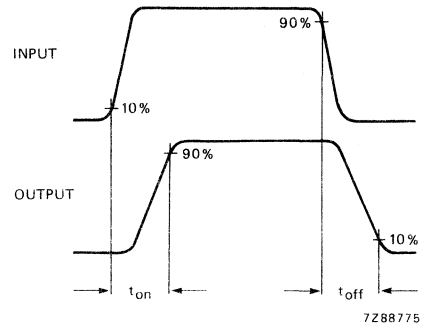


Fig.3 Input and output waveforms.

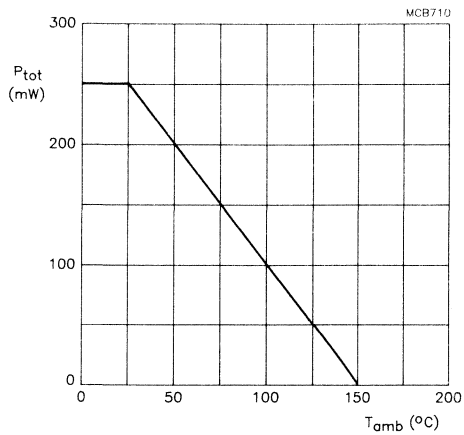


Fig.4 Power derating curve.

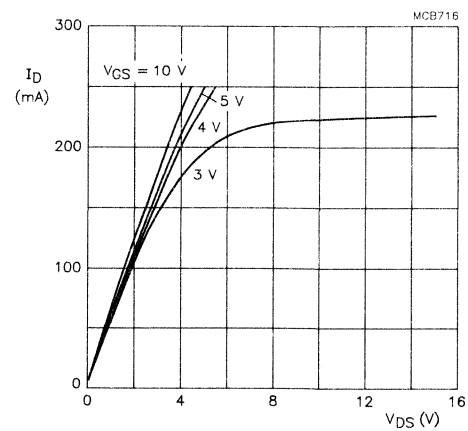


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

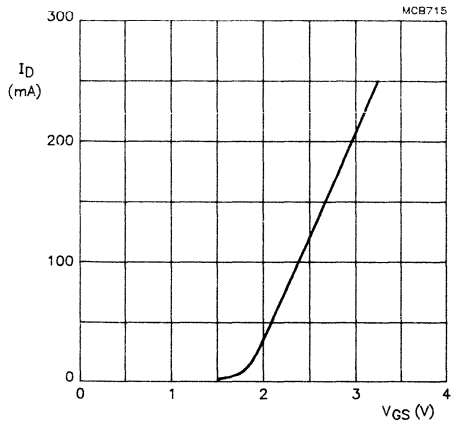


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

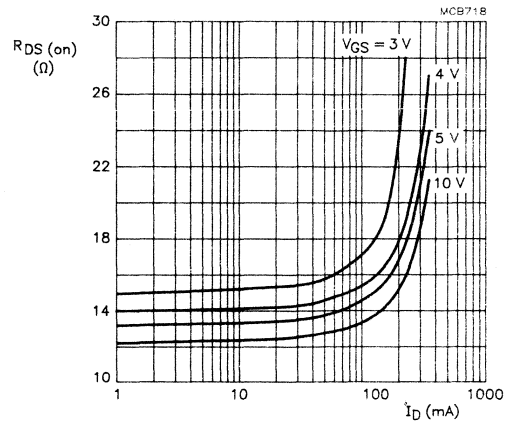


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

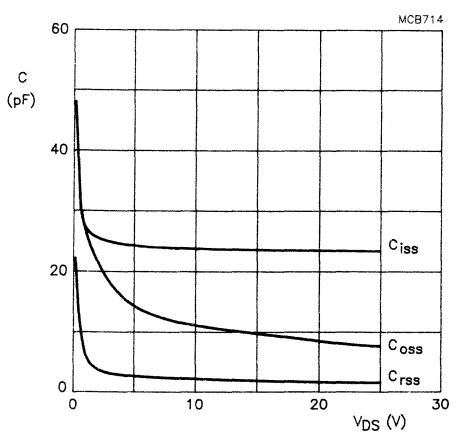


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.5 Ω 5.0 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min. typ.	100 mS 200 mS

MECHANICAL DATA

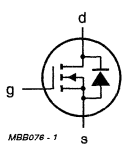
Dimensions in mm

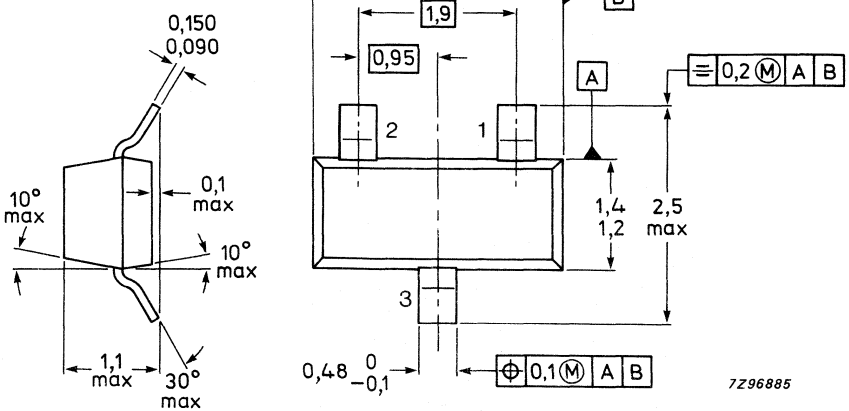
Fig.1 SOT23.

Marking code:
PMBF170 = pKX

Pinning

1 = gate
2 = source
3 = drain





TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max. max.	300 mW (note 1) 250 mW (note 2)
Storage temperature range	T_{stg}	−65 to + 150 °C	
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W
From junction to ambient (note 2)	$R_{th\ j\text{-}a}$	=	500 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min. typ.	60 V 90 V
Drain-source leakage current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	500 nA
V_{DS} = 48V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 3.0 V
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\ on}$	typ. max.	2.5 Ω 5.0 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{iss}	typ. max.	25 pF 40 pF
Output capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{oss}	typ. max.	22 pF 30 pF
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{rss}	typ. max.	6 pF 10 pF

Notes

1. Mounted on ceramic substrate measuring 10 mm x 8 mm x 0.7 mm.
2. Mounted on printed-circuit board.

Switching times

V_{GS} = 0 to 10 V; I_D = 200 mA ; V_{DD} = 50 V

t_{on}	max.	10	ns
t_{off}	max.	15	ns

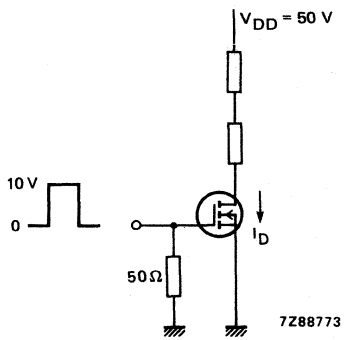


Fig.2 Switching times test circuit.

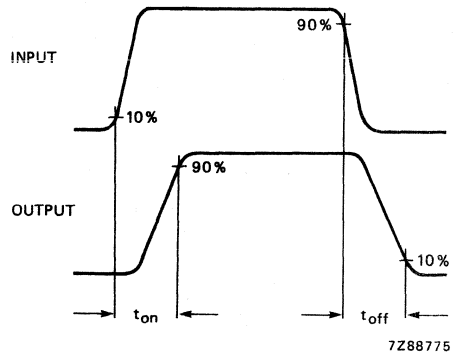


Fig.3 Input and output waveforms.

N-CHANNEL FETS

Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

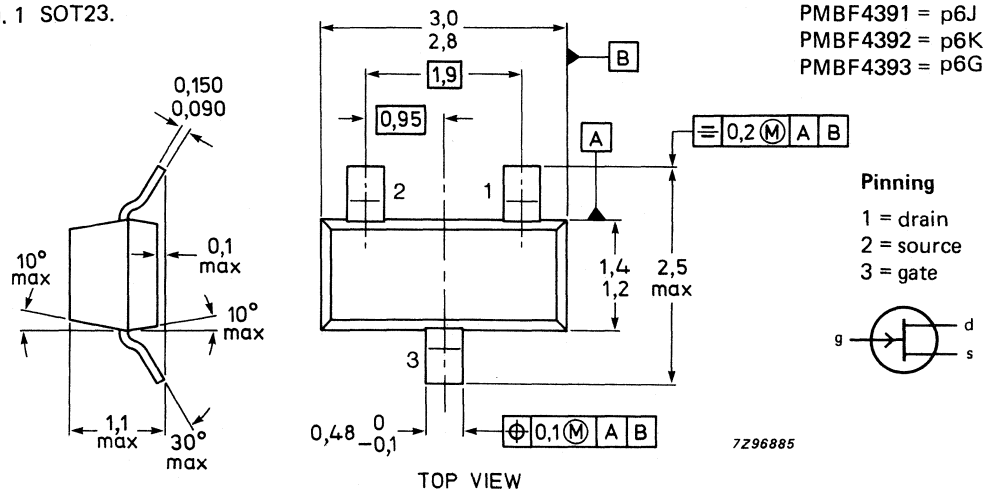
QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{(P)GS}$	> <	4 10	2 5	0.5 3	V V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$R_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz $-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	3.5	3.5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSM}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6 mA; $-V_{GSM}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3 mA; $-V_{GSM}$ = 5 V	t_{off}	<	–	–	50	ns

MECHANICAL DATA

Fig. 1 SOT23.

Dimensions in mm



Marking code

PMBF4391 = p6J
PMBF4392 = p6K
PMBF4393 = p6G

Pinning

1 = drain
2 = source
3 = gate

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBF4391	PMBF4392	PMBF4393
Gate-source voltage					
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1	1	1 V
Gate-source cut-off current					
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	<	0.1	0.1	0.1 nA
V_{DS} = 0 V; $-V_{GS}$ = 20 V; T_{amb} = 150 °C	$-I_{GSS}$	<	0.2	0.2	0.2 μA
Drain current					
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5 mA
		<	150	75	30 mA
Gate-source breakdown voltage					
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40 V
Gate-source cut-off voltage					
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4	2	0.5 V
		<	10	5	3 V
Drain-source voltage (on)					
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	– V
I_D = 6 mA; V_{GS} = 0	V_{DSon}	<		0.4	– V
I_D = 3 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4 V
Drain-source resistance (on)					
I_D = 0; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$r_{ds\ on}$	<	30	60	100 Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

			PMBF4391	PMBF4392	PMBF4393
Drain cut-off current					
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	<	0.1	–	– nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	<	–	0.1	– nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	<	–	–	0.1 nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	0.2	–	– μA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.2	– μA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.2 μA
y-parameters (common source)					
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_{amb} = 25 °C					
Input capacitance	C_{is}	<	14	14	14 pF
Feedback capacitance					
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	– pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	– pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5 pF
Switching times					
V_{DD} = 10 V; V_{GS} = 0					
Conditions I_D and $-V_{GSoff}$	I_D	=	12	6	3 mA
	$-V_{GS\,off}$	=	12	7	5 V
	R_L	=	750	1550	3150 Ω
Rise time	t_r	<	5	5	5 ns
Turn on time	t_{on}	<	15	15	15 ns
Fall time	t_f	<	15	20	30 ns
Turn off time	t_{off}	<	20	35	50 ns

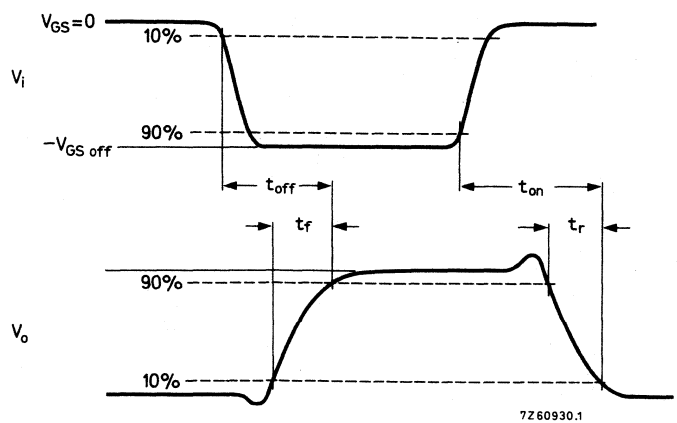
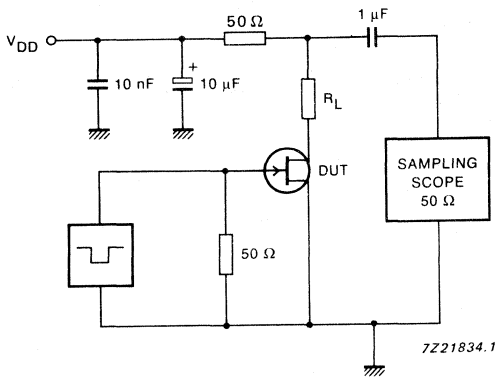


Fig.2 Switching times waveforms.



Pulse generator:

t_r	<	0.5 ns
t_f	<	0.5 ns
t_p	=	100 μs
δ	=	0.01

Oscilloscope:

R_i	=	50 Ω

Fig. 3 Test circuit.

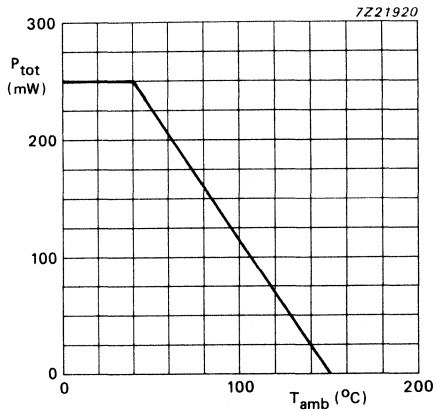


Fig.4 Power derating curve.

N-channel field-effect transistor PMBF4416; PMBF4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

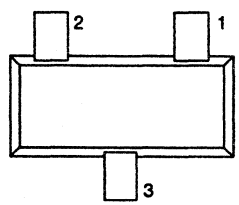
N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT23

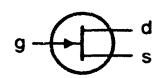
PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PMBF4416		–	30	V
	PMBF4416A		–	35	V
I_{DSS}	drain-source current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF4416		–	–6	V
	PMBF4416A		–2.5	–6	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS



Top view



MAM036

Marking codes:
PMBF4416: P6A.
PMBF4416A: M16.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PMBF4416		–	30	V
	PMBF4416A		–	35	V
V_{GSO}	gate-source voltage				
	PMBF4416		–	–30	V
	PMBF4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	PMBF4416		–	–30	V
	PMBF4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

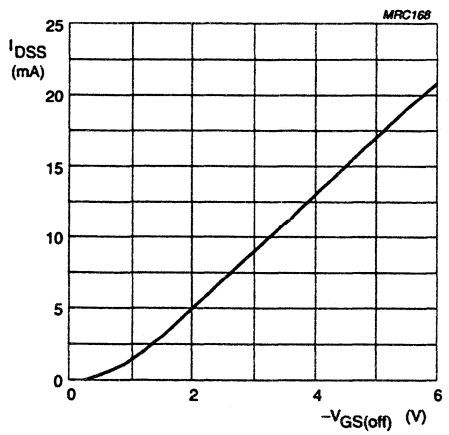
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	PMBF4416		–30	–	V
	PMBF4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF4416		–	–6	V
	PMBF4416A		–2.5	–6	V
$\lvert Y_{fs}\rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\lvert Y_{os}\rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF4416		–	50	μS
	PMBF4416A		–	50	μS

DYNAMIC CHARACTERISTICS

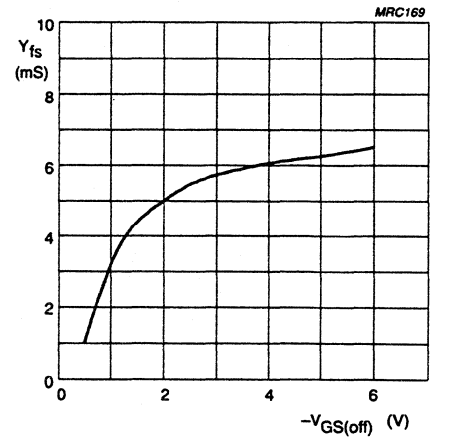
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	µS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	µS
		f = 400 MHz	–	–100	–	µS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	µS
		f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



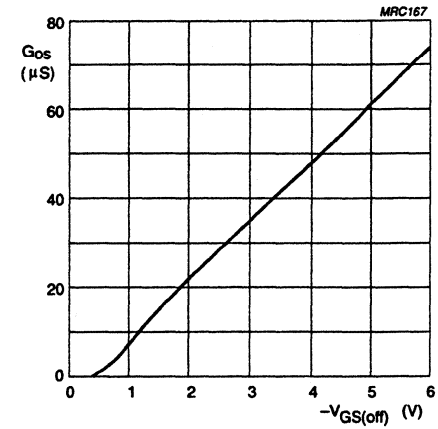
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



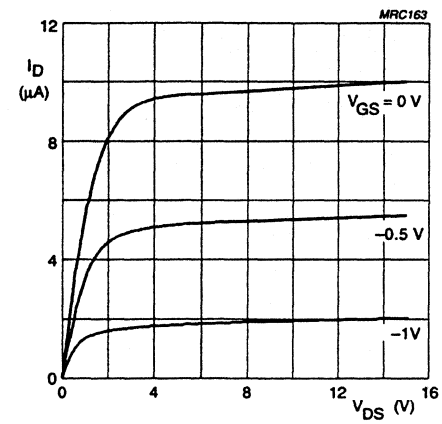
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



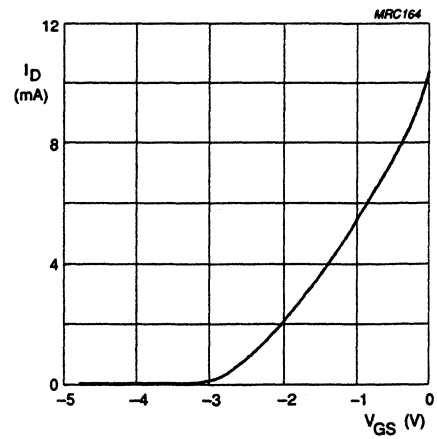
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



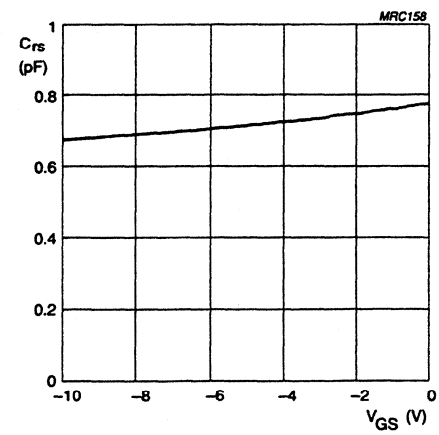
T_j = 25 °C.

Fig.5 Typical output characteristics.



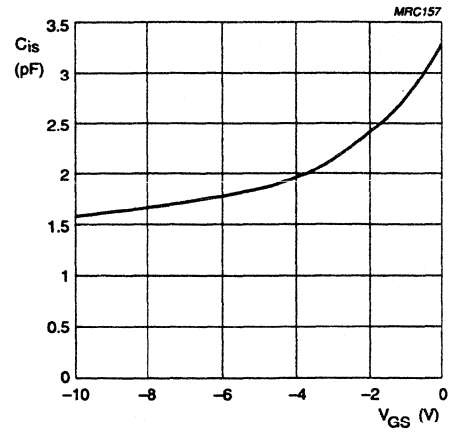
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

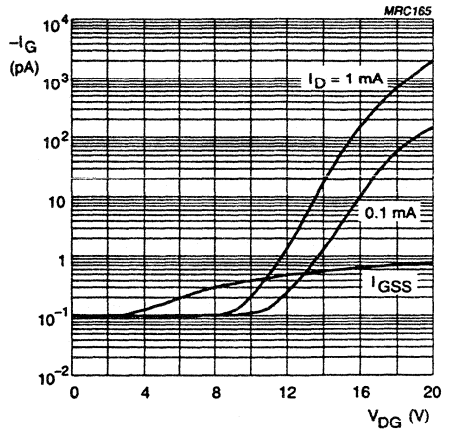


Fig.9 Gate current as a function of drain-gate voltage, typical values.

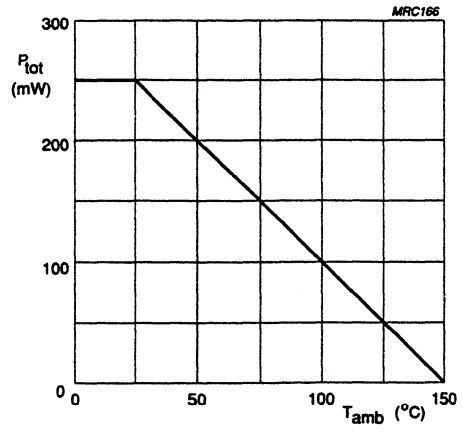
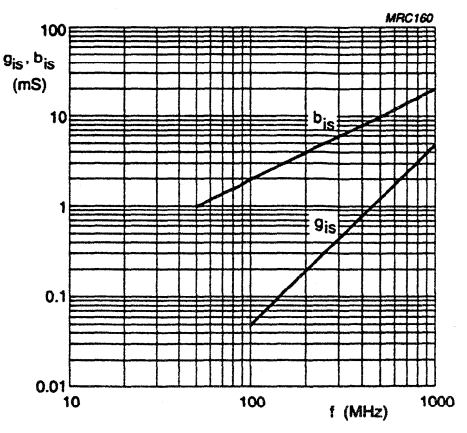
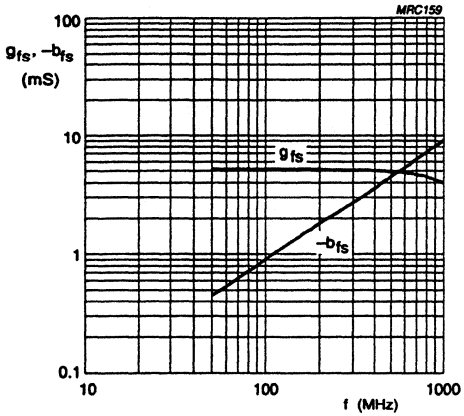


Fig.10 Power derating curve.



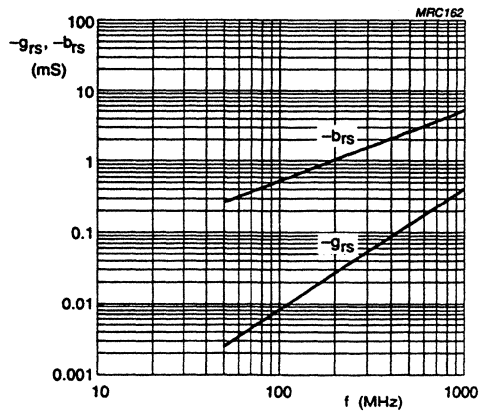
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



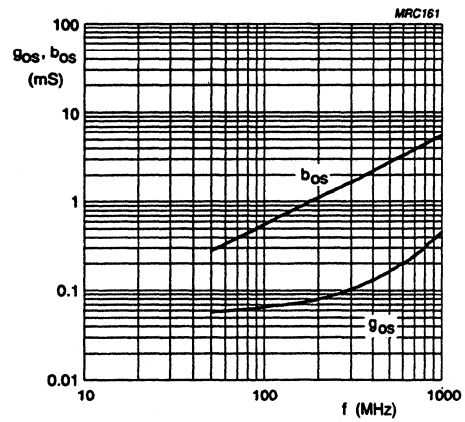
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for PMBF4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

N-channel field-effect transistors PMBF5484; PMBF5485; PMBF5486

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

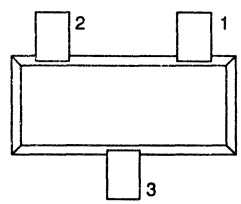
N-channel, symmetrical, silicon junction FETs in a surface-mountable SOT23 envelope. Intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT23

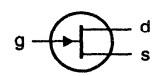
PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		1	5	mA
	PMBF5485		4	10	mA
	PMBF5486		8	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF5484		−0.3	−3	V
	PMBF5485		−0.5	−4	V
	PMBF5486		−2	−6	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz			
	PMBF5484		3	6	mS
	PMBF5485		3.5	7	mS
	PMBF5486		4	8	mS



Top view



MAM036

Marking codes:
PMBF5484: p6B
PMBF5485: p6M
PMBF5486: p6H

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	gate-drain voltage		–	–25	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

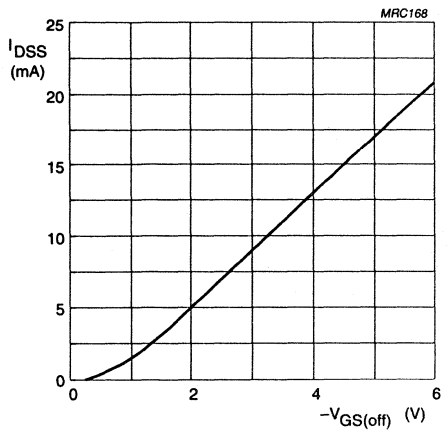
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 µA	–25	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		1	5	mA
	PMBF5485		4	10	mA
	PMBF5486		8	20	mA
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PMBF5484		–0.3	–3	V
	PMBF5485		–0.5	–4	V
	PMBF5486		–2	–6	V
$\lvert Y_{fs}\rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		3	6	mS
	PMBF5485		3.5	7	mS
	PMBF5486		4	8	mS
$\lvert Y_{os}\rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PMBF5484		–	50	µS
	PMBF5485		–	60	µS
	PMBF5486		–	75	µS

DYNAMIC CHARACTERISTICS

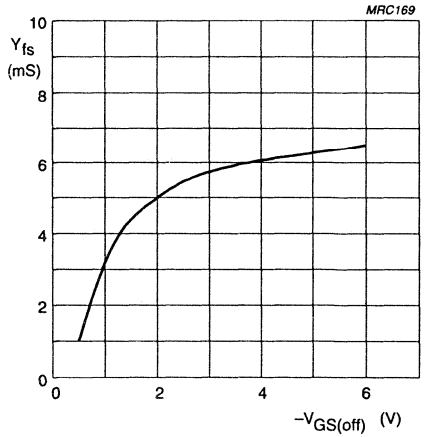
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	5	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	1	pF
g_{is}	common source input conductance					
	PMBF5484	f = 100 MHz	100	–	–	µS
	PMBF5485; PMBF5486	f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance					
	PMBF5484	f = 100 MHz	2.5	–	–	mS
	PMBF5485	f = 400 MHz	3	–	1	mS
	PMBF5486	f = 400 MHz	3.5	–	1	mS
g_{os}	common source output conductance					
	PMBF5484	f = 100 MHz	–	–	75	µS
	PMBF5485; PMBF5486	f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



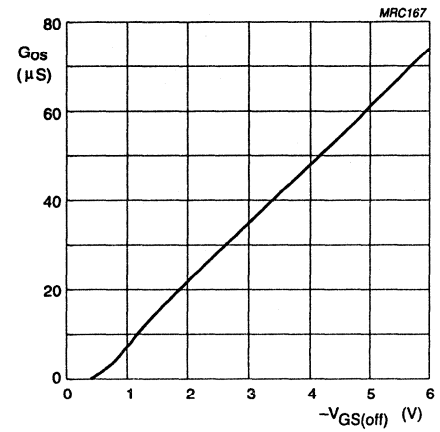
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.2 Drain current as a function of gate-source cut-off voltage.



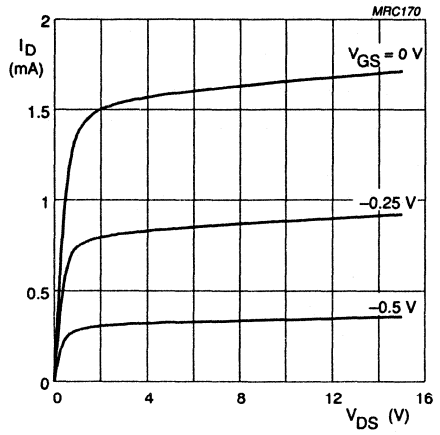
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



V_{DS} = 15 V; T_j = 25 °C; typical values.

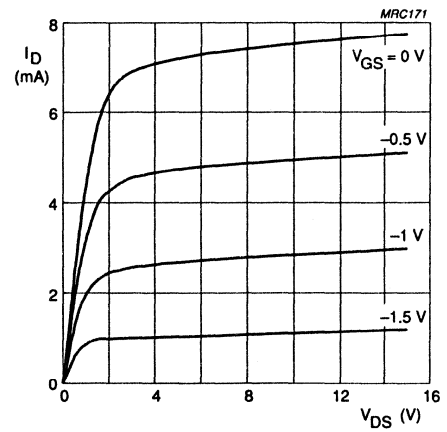
Fig.4 Common source output conductance as a function of gate-source cut-off voltage.



PMBF5484

T_j = 25 °C.

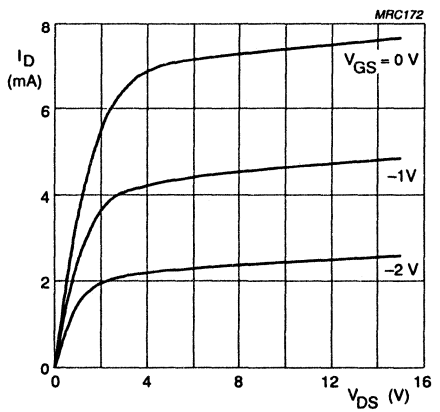
Fig.5 Typical output characteristics.



PMBF5485

T_j = 25 °C.

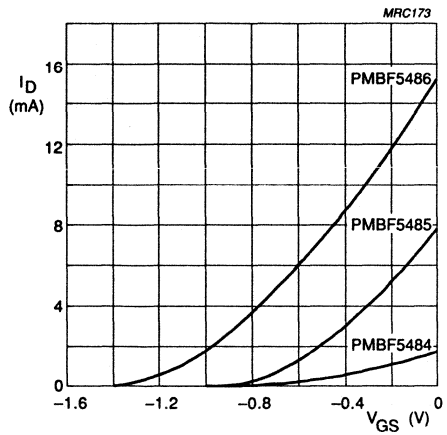
Fig.6 Typical output characteristics.



PMBF5486

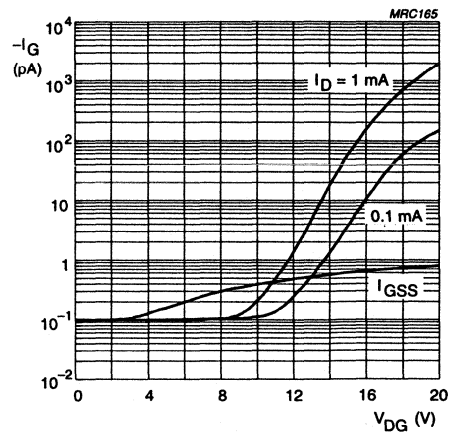
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics.



T_j = 25 °C.

Fig.9 Gate current as a function of drain-gate voltage, typical values.

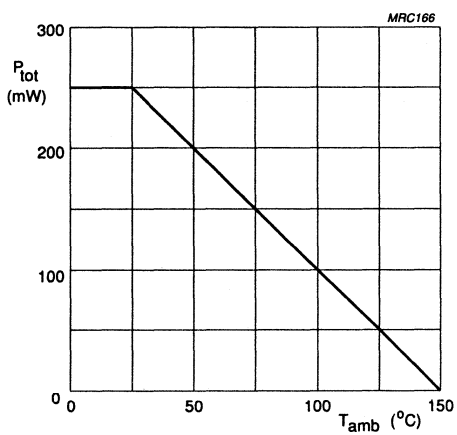
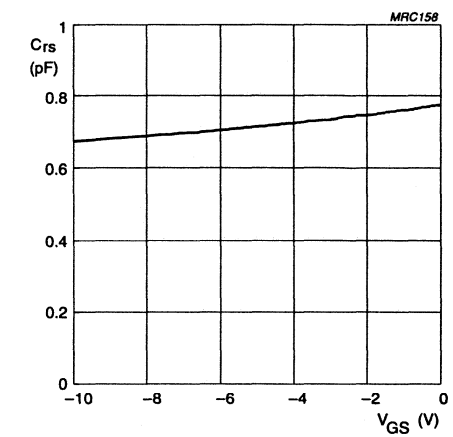
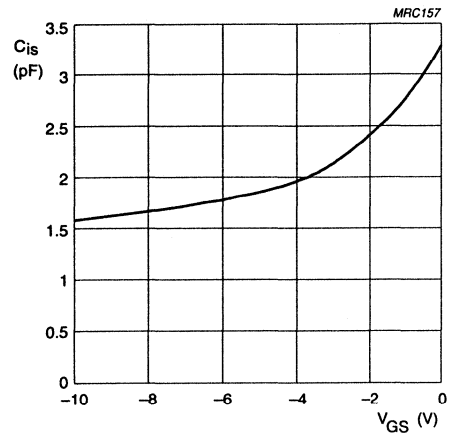


Fig.10 Power derating curve.



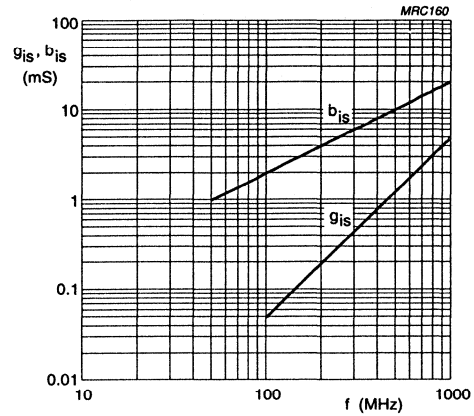
V_{DS} = 15 V; T_j = 25 °C.

Fig.11 Typical feedback capacitance.



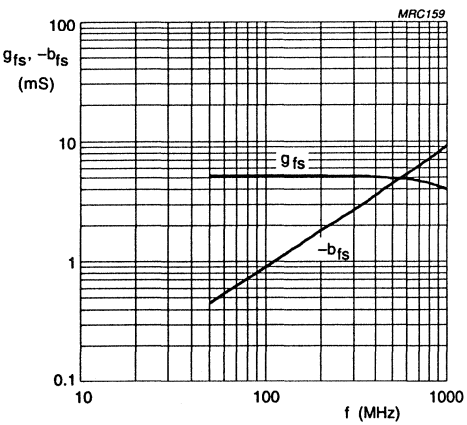
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input capacitance.



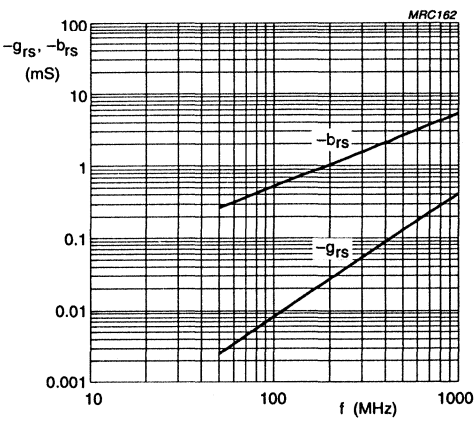
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.13 Common source input conductance.



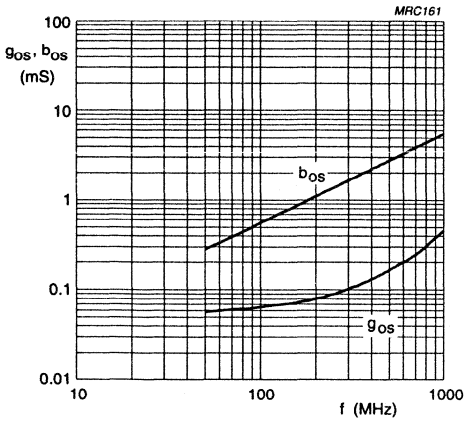
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.14 Common source transfer conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.15 Common source feedback conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.16 Common source output conductance.

N-channel junction FETs PMBFJ108; PMBFJ109; PMBFJ110

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (<8 Ω for PMBFJ108).

DESCRIPTION

Symmetrical N-channel junction FETs in a SOT23 envelope. Intended for use in applications such as analog switches, choppers and commutators and in audio amplifiers.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

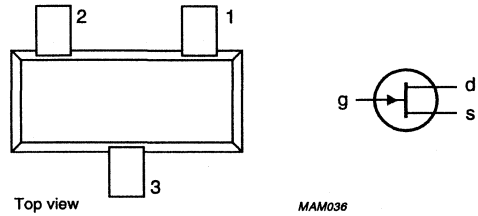


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	drain-drain voltage		–	–25	V
I_G	forward gate current (DC)			50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Notes

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	V_{GS} = −10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	PMBFJ108 PMBFJ109 PMBFJ110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 µA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 µA V_{DS} = 5 V	PMBFJ108 PMBFJ109 PMBFJ110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	PMBFJ108 PMBFJ109 PMBFJ110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PMBFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PMBFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PMBFJ110).

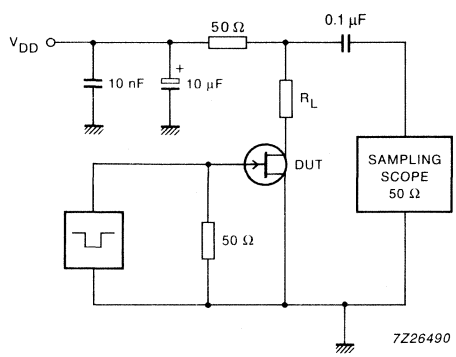


Fig.2 Switching circuit.

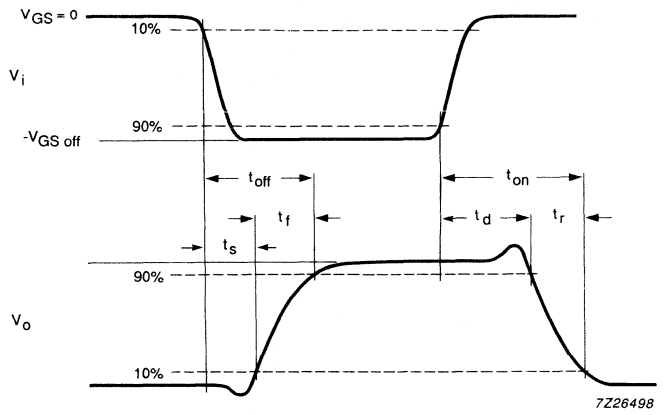


Fig.3 Input and output waveforms.

N-channel junction FETs PMBFJ111; PMBFJ112; PMBFJ113

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (<30 Ω for PMBFJ111).

DESCRIPTION

Symmetrical N-channel junction FETs in a surface mount SOT23 envelope. Intended for use in applications such as analog switches, choppers, commutators, multiplexers and thin and thick film hybrids.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

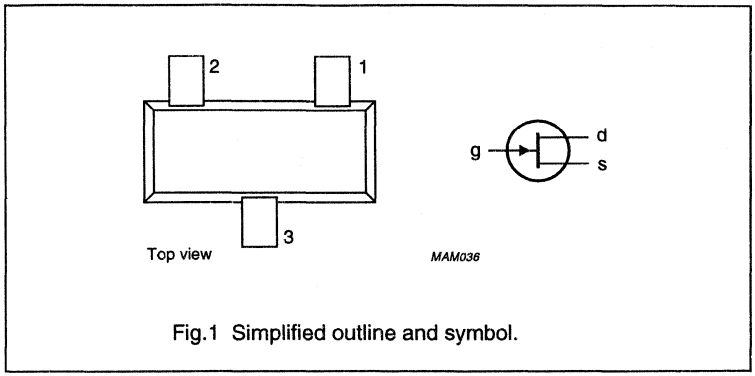


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±40	V
V_{GSO}	gate-source voltage		–	–40	V
V_{GDO}	drain-drain voltage		–	–40	V
I_G	forward gate current (DC)		–	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

$T_j = P(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430	K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500	K/W

Notes

1. Mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Mounted on printed circuit board.

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	1	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	PMBFJ111 PMBFJ112 PMBFJ113	20 5 2	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ µA $V_{DS} = 0$		40	-	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ µA $V_{DS} = 5$ V	PMBFJ111 PMBFJ112 PMBFJ113	3 1 0.5	10 5 3	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	PMBFJ111 PMBFJ112 PMBFJ113	- - -	30 50 100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{iss}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	6	-	pF
		V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	22	28	pF
C_{rss}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	3	-	pF
Switching times (see Fig.2)					
t_r	rise time	note 1	6	-	ns
t_{on}	turn-on time	note 1	13	-	ns
t_f	fall time	note 1	15	-	ns
t_{off}	turn-off time	note 1	35	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 10 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 750 Ω (PMBFJ111);
   $-V_{GS(off)}$ = 7 V, R_L = 1550 Ω (PMBFJ112);
   $-V_{GS(off)}$ = 5 V, R_L = 3150 Ω (PMBFJ113).

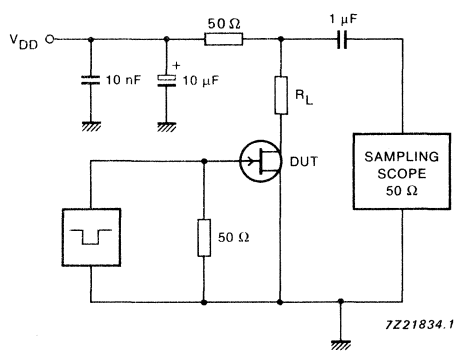


Fig.2 Switching circuit.

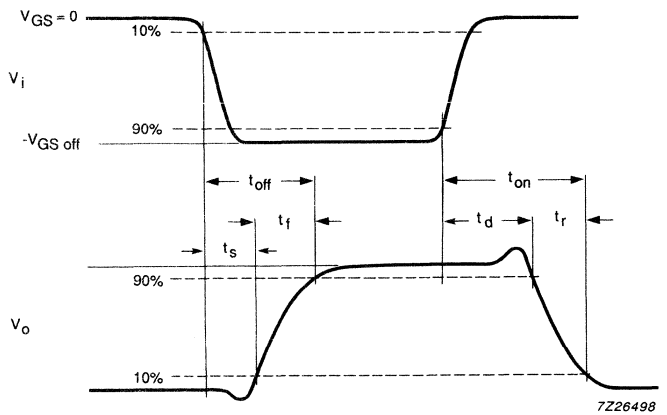


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT-23 envelopes.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30				V
Gate-source voltage	V_{GSO}	max.	30				V
Gate current	$-I_G$	max.	50				mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300				mW
			PMBFJ174	**175**	**176**	**177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

MECHANICAL DATA

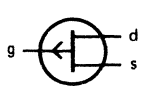
Dimensions in mm

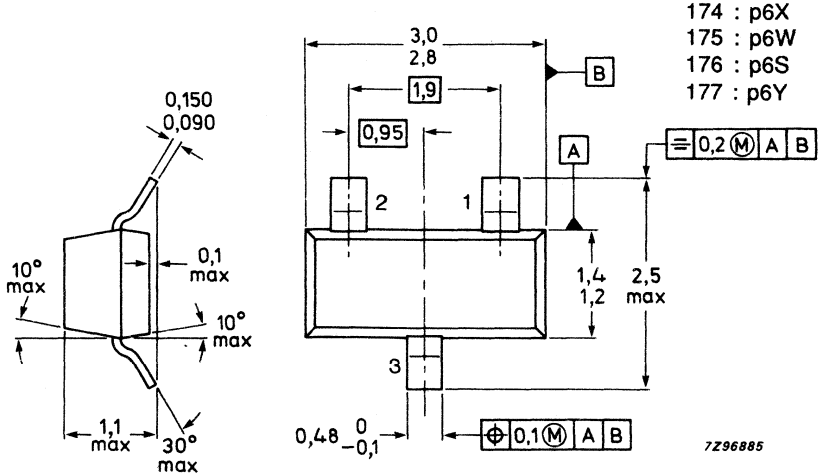
Fig. 1 SOT-23.

Pinning:
1 = Drain
2 = Source
3 = Gate

Marking codes:

174 : p6X
175 : p6W
176 : p6S
177 : p6Y





TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBFJ174	175	176	177	
Gate cut-off current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\,off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
V_{GS} = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
V_{GS} = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
V_{GS} = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)		PMBFJ174		175	176	177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

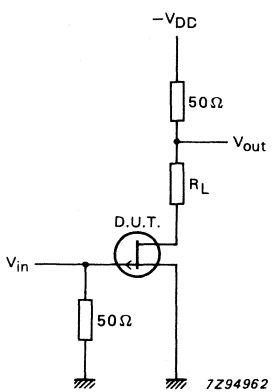


Fig. 2 Switching times test circuit

Rise time input voltage < 1 ns

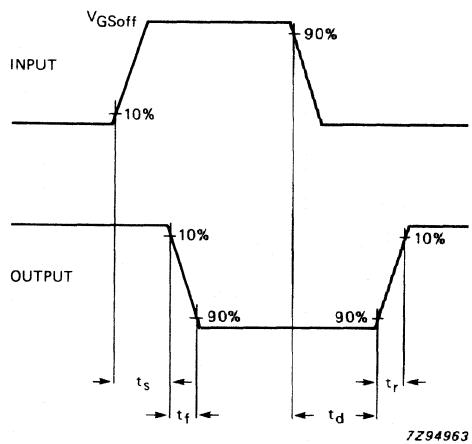


Fig. 3 Input and output waveforms

$t_d + t_r = t_{on}$

$t_s + t_f = t_{off}$

N-channel silicon field-effect transistors

PMBFJ308/309/310

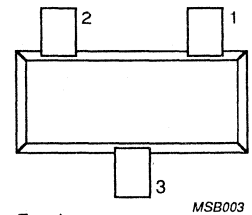
FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT23 envelope. They are intended for use in VHF amplifiers, the AM input stage of car radios, oscillators and mixers.

PIN CONFIGURATION



Marking codes:
PMBFJ308: M08.
PMBFJ309: M09.
PMBFJ310: M10.

Top view

Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	PMBFJ308		12	60	mA
	PMBFJ309		12	30	mA
	PMBFJ310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	PMBFJ308		1	6.5	V
	PMBFJ309		1	4	V
	PMBFJ310		2	6.5	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

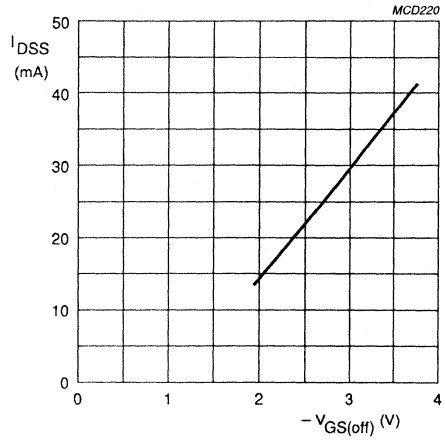
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	25	–		V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	PMBFJ308		12	–	60	mA
	PMBFJ309		12	–	30	mA
	PMBFJ310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	PMBFJ308		1	–	6.5	V
	PMBFJ309		1	–	4	V
	PMBFJ310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\lvert Y_{fs} \rvert$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\lvert Y_{os} \rvert$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

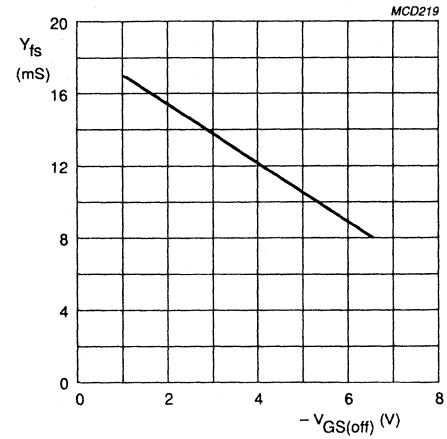
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\overline{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

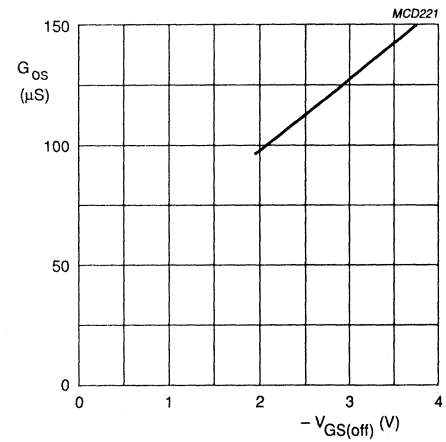
Fig.2 Drain current as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

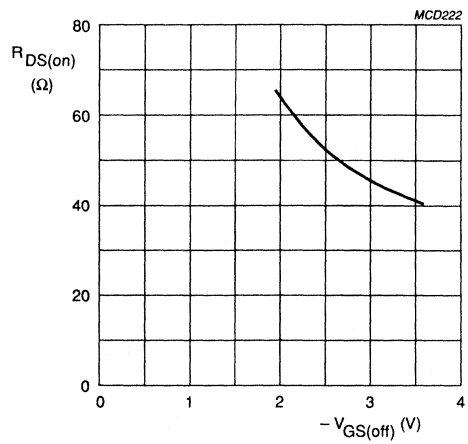
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

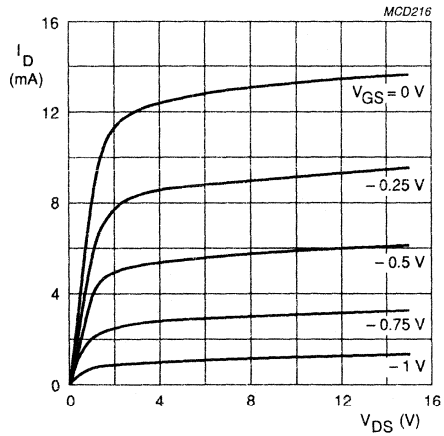
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

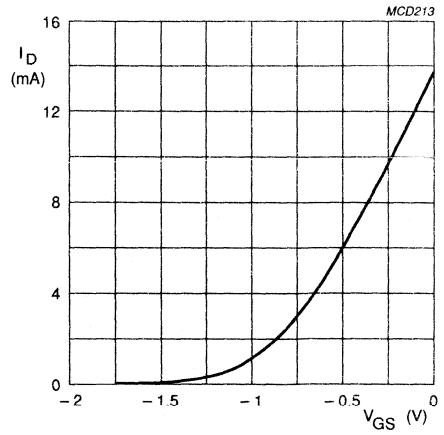
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



PMBFJ308.

T_j = 25 °C.

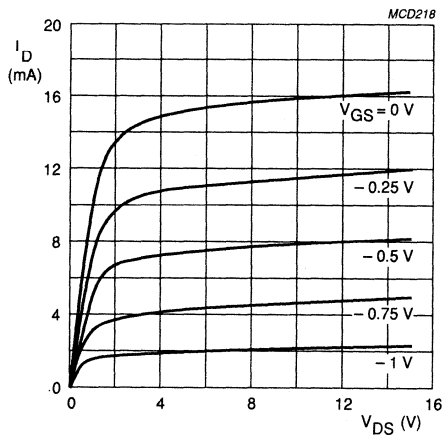
Fig.6 Output characteristics, typical values.



PMBFJ308.

V_{DS} = 10 V; T_j = 25 °C.

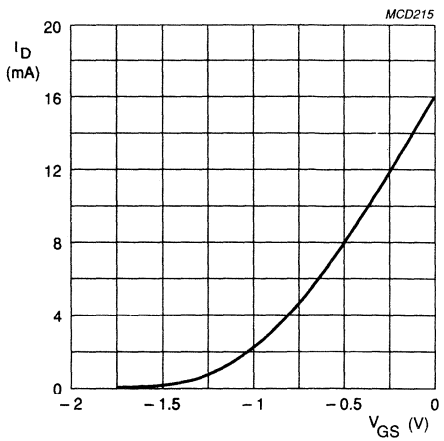
Fig.7 Input characteristics, typical values.



PMBFJ309.

T_j = 25 °C.

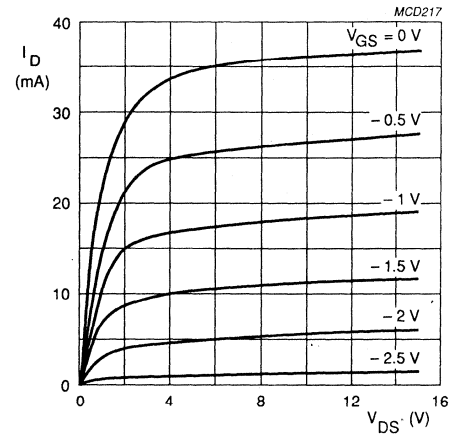
Fig.8 Output characteristics, typical values.



PMBFJ309.

V_{DS} = 10 V; T_j = 25 °C.

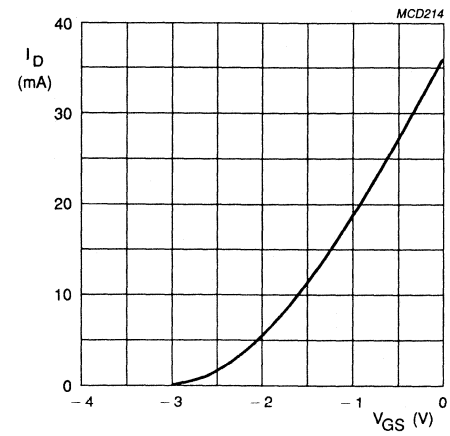
Fig.9 Input characteristics, typical values.



PMBFJ310.

T_j = 25 °C.

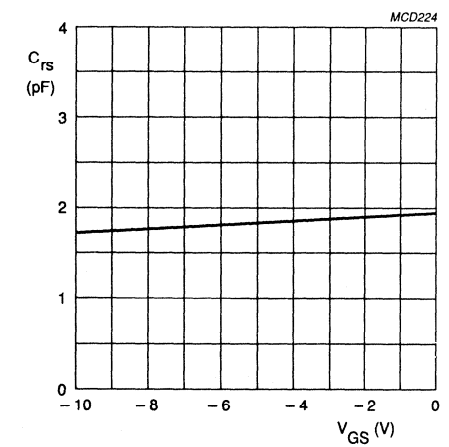
Fig.10 Output characteristics, typical values.



PMBFJ310.

V_{DS} = 10 V; T_j = 25 °C.

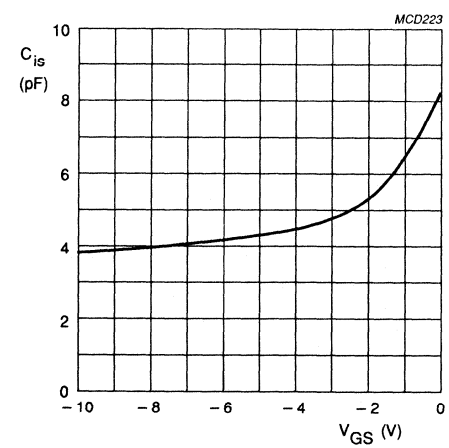
Fig.11 Input characteristics, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

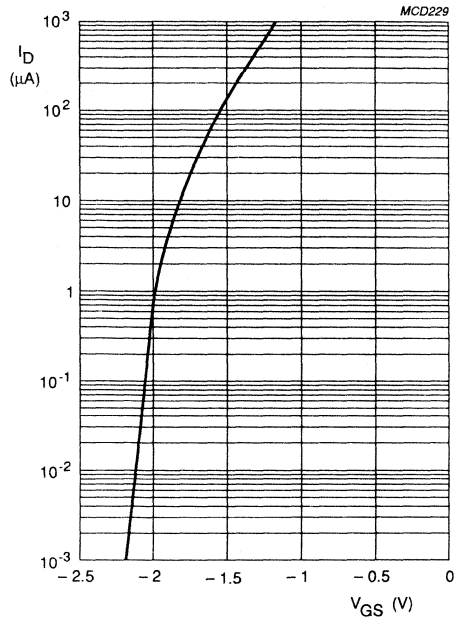
Fig.12 Feedback capacitance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

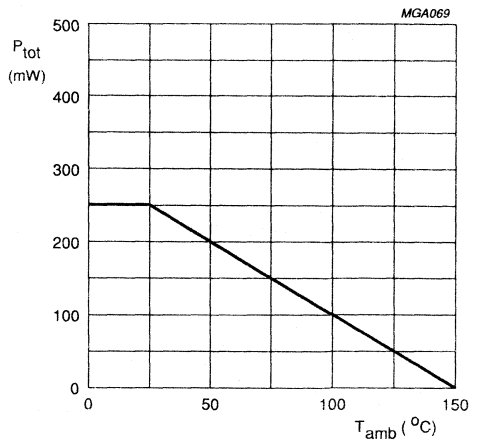
Fig.13 Input capacitance, typical values.



PMBFJ308, 309 & 310.

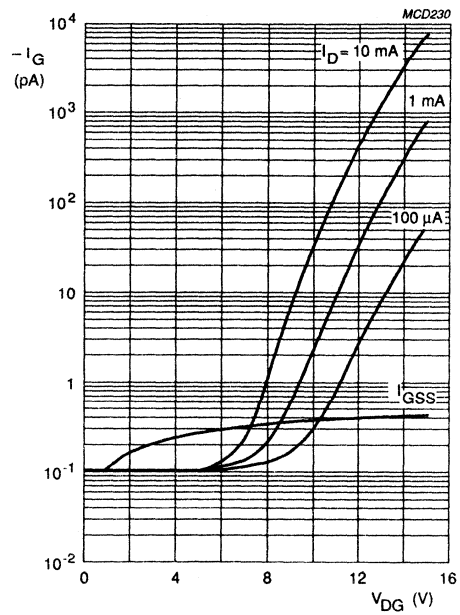
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



PMBFJ308, 309 & 310.

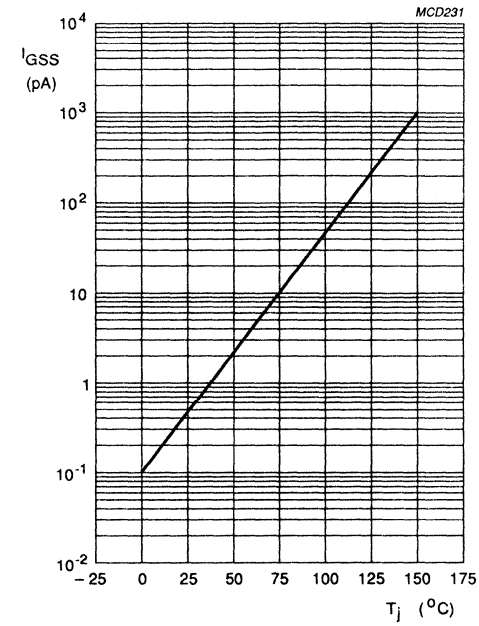
Fig.15 Power derating curve.



PMBFJ308, 309 & 310.

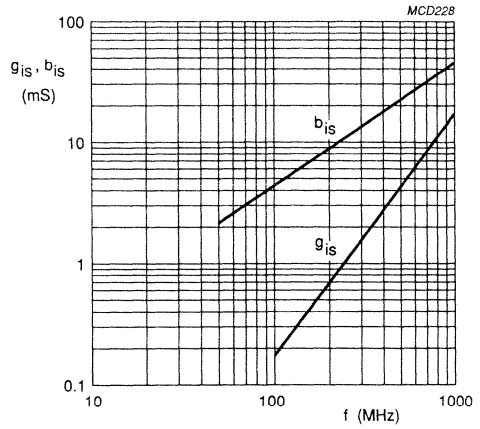
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



PMBFJ308, 309 & 310.

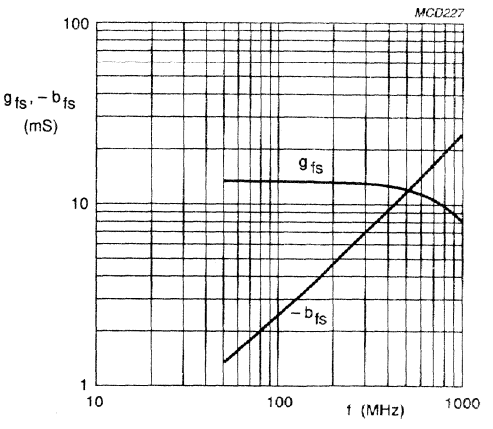
Fig.17 Gate current as a function of junction temperature, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

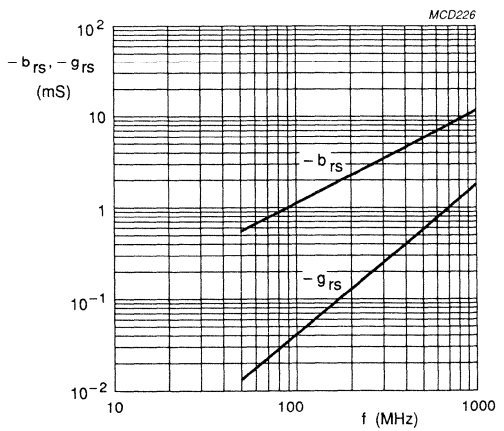
Fig.18 Input admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

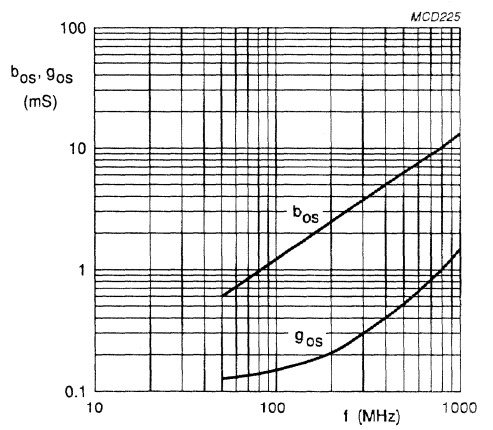
Fig.19 Forward admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		360		mW
			PN4391	PN4392	PN4393	
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4	2	0.5	V
		max.	10	5	3	V
Drain-source on-resistance I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100	Ω

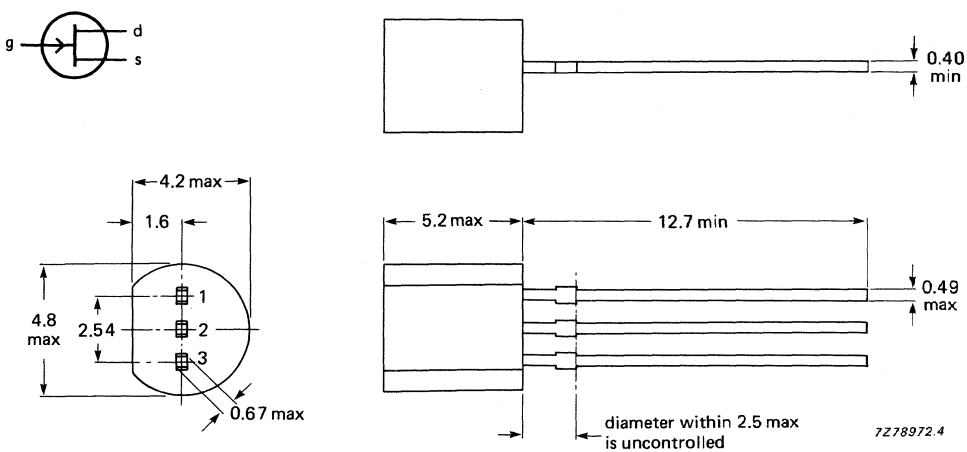
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92.

Pinning

1 = Gate
2 = Source
3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Forward gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	350	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Reverse gate current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	1.0	1.0	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 100 °C	$-I_{GSS}$	max.	200	200	200	nA
Drain cut-off current						
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	max.	1.0			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	max.		1.0		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	max.			1.0	nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.	200			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.		200		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.			200	nA
Drain saturation current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
		max.	150	100	60	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage						
V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4.0	2.0	0.5	V
		max.	10	5.0	3.0	V
Drain-source on-resistance						
I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100	Ω
Drain-source on-voltage						
V_{GS} = 0; I_D = 12 mA	$V_{DS\,on}$	max.	0.4			V
V_{GS} = 0; I_D = 6 mA	$V_{DS\,on}$	max.		0.4		V
V_{GS} = 0; I_D = 3 mA	$V_{DS\,on}$	max.			0.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Drain-source on-resistance						
V_{DS} = 0; V_{GS} = 0; f = 1 kHz; T_a = 25 °C	$R_{DS\,on}$	max.	30	60	100	Ω
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_a = 25 °C	C_{iss}	max.	16	16	16	pF
Feedback capacitance						
V_{DS} = 0; $-V_{GS}$ = 12 V } f = 1 MHz	C_{rss}	max.	5			pF
V_{DS} = 0; $-V_{GS}$ = 7 V } f = 1 MHz	C_{rss}	max.		5		pF
V_{DS} = 0; $-V_{GS}$ = 5 V } f = 1 MHz	C_{rss}	max.			5	pF
Switching times						
test conditions						
V_{DD} = 10 V; V_{GS} = 0 to $V_{GS\,off}$	I_D	=	12	6.0	3.0	mA
	$-V_{GS\,off}$	=	12	7.0	5.0	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	max.	5	5	5	ns
Turn-on time	t_{on}	max.	15	15	15	ns
Fall time	t_f	max.	15	20	30	ns
Turn-off time	t_{off}	max.	20	35	50	ns

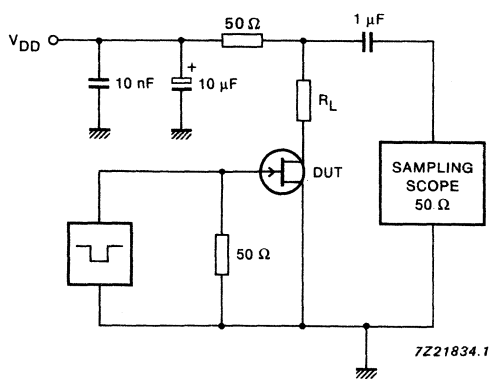


Fig.2 Switching times test circuit.

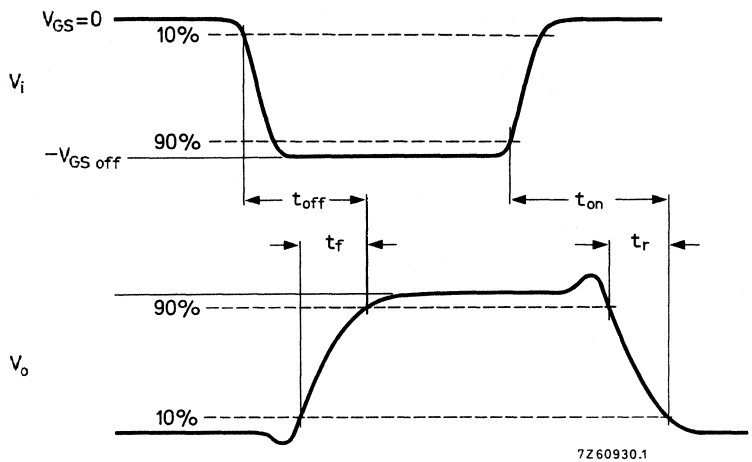


Fig.3 Input and output waveforms.

N-channel field-effect transistor PN4416; PN4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a SOT54 envelope. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT54 (TO-92).

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PN4416		–	30	V
	PN4416A		–	35	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	400	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PN4416		–	–6	V
	PN4416A		–2.5	–6	V
$\lvert Y_{fs} \rvert$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS

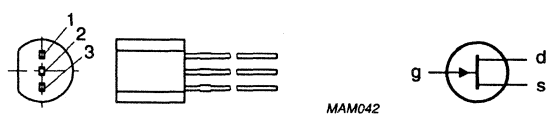


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	PN4416		–	30	V
	PN4416A		–	35	V
V_{GSO}	gate-source voltage				
	PN4416		–	–30	V
	PN4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	PN4416		–	–30	V
	PN4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	350 K/W

Note

1. Mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for drain leads 10 mm².

STATIC CHARACTERISTICS

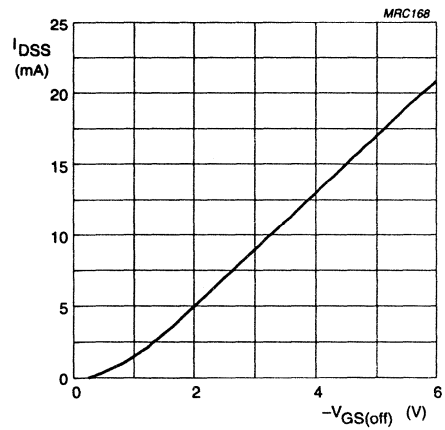
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	PN4416		–30	–	V
	PN4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	PN4416		–	–6	V
	PN4416A		–2.5	–6	V
$\lvert Y_{fs}\rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\lvert Y_{os}\rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	PN4416		–	50	μS
	PN4416A		–	50	μS

DYNAMIC CHARACTERISTICS

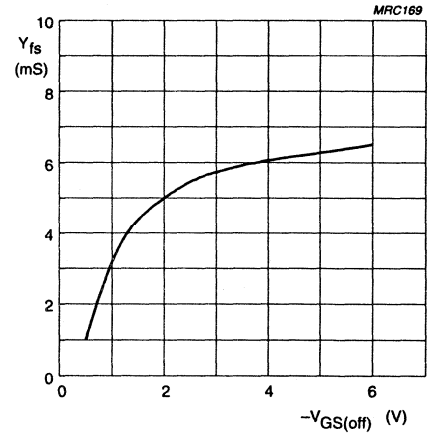
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	µS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	µS
		f = 400 MHz	–	–100	–	µS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	µS
		f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√HZ



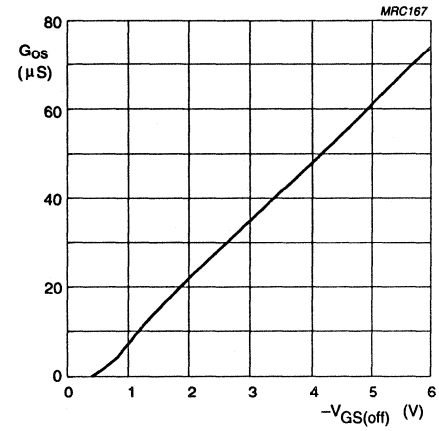
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



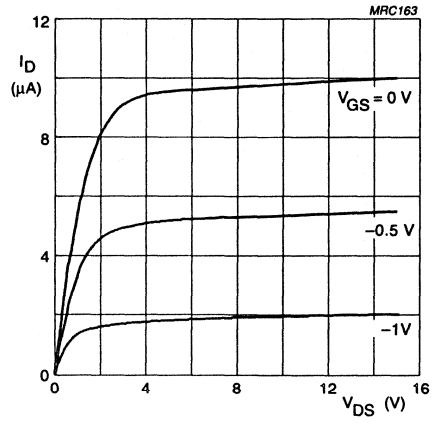
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



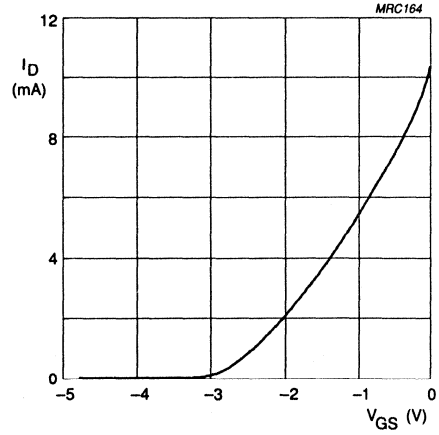
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



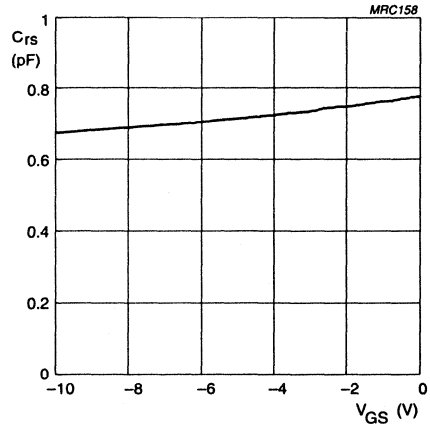
T_j = 25 °C.

Fig.5 Typical output characteristics.



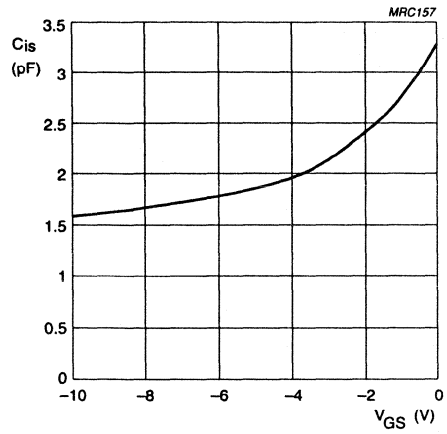
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

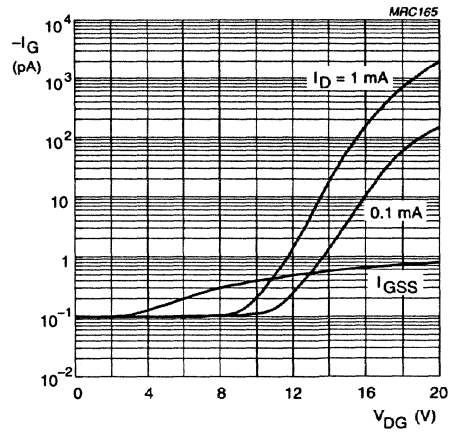


Fig.9 Gate current as a function of drain-gate voltage, typical values.

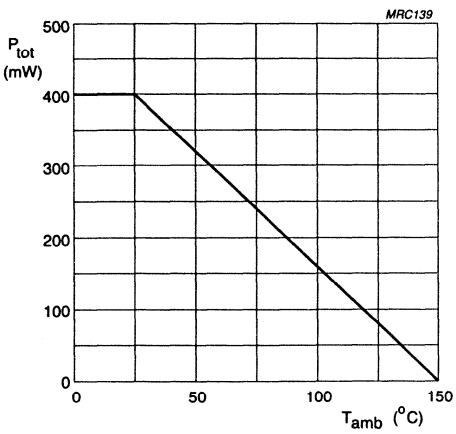
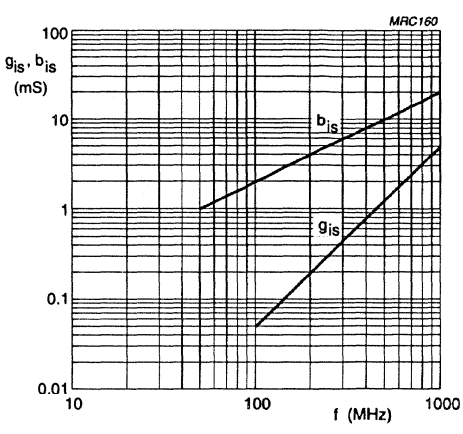
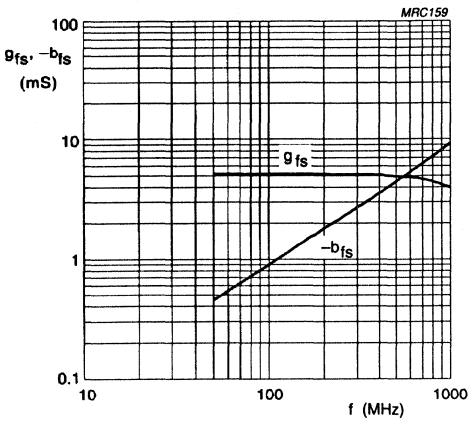


Fig.10 Power derating curve.



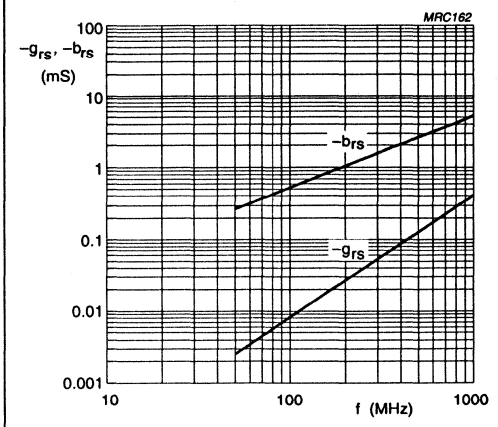
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



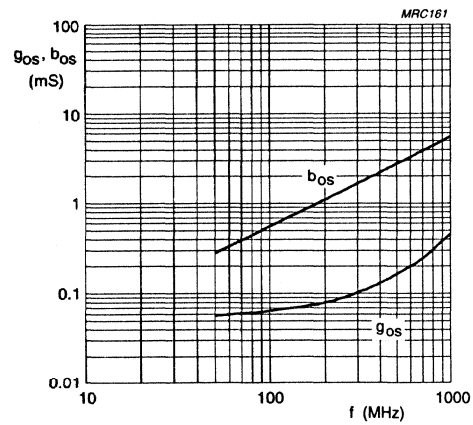
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for PN4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

N-channel junction FETs PZFJ108; PZFJ109; PZFJ110

FEATURES

- High-speed switching
- Interchangeability of drain and source connections
- Low R_{DSon} at zero gate voltage (<8 Ω for PZFJ108).

DESCRIPTION

Symmetrical N-channel junction FETs in a SOT223 envelope. Intended for use in applications such as analog switches, choppers and commutators, as well as in audio amplifiers.

PINNING - SOT223

PIN	DESCRIPTION
1	drain
2	gate
3	source
3	gate

Note

1. Drain and source are interchangeable.

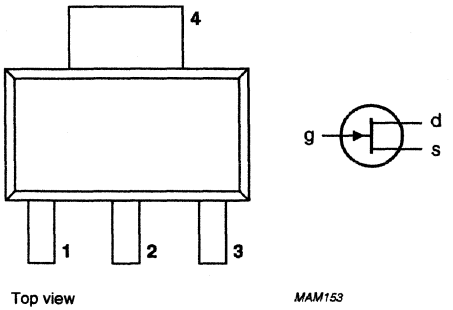


Fig.1 Simplified outline and symbol.

N-channel junction FETs PZFJ108/PZFJ109/PZFJ110

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C (note 1)	-	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy PCB, 40 mm x 40 mm x 1.5 mm. Mounting pad for the gate lead minimum 6 cm^2.

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS} = 10$ V $V_{DS} = 5$ V		-	3	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	PZFJ108 PZFJ109 PZFJ110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ µA $V_{DS} = 0$		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ µA $V_{DS} = 5$ V	PZFJ108 PZFJ109 PZFJ110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	PZFJ108 PZFJ109 PZFJ110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Figs. 2 and 3)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PZFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PZFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PZFJ110).

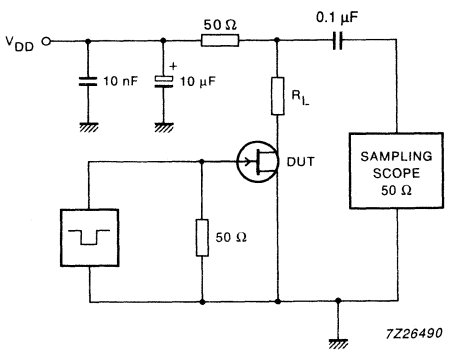


Fig.2 Switching circuit.

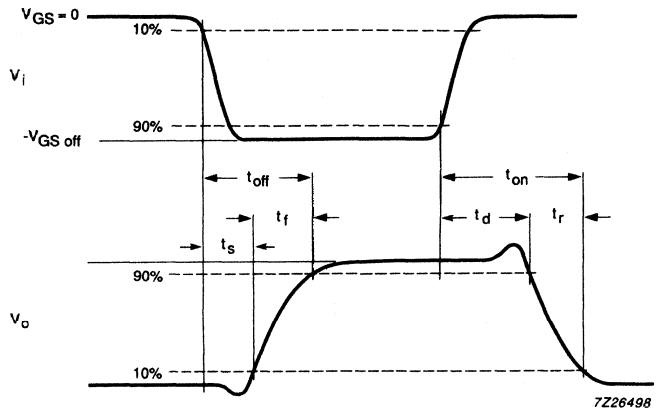


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

FEATURES

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	240	V
V_{GSth}	gate-source threshold voltage	2	V
I_D	drain current (DC)	210	mA
R_{DSon}	drain-source on-state resistance	6	Ω

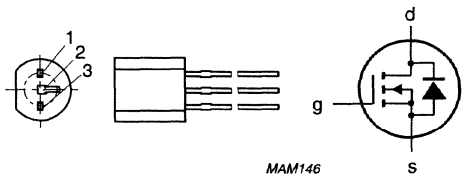


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	40	V
I_D	drain current	DC value	-	210	mA
I_{DM}	drain current	peak value	-	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100$ µA $V_{GS} = 0$	240	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120$ V $V_{GS} = 0$	-	-	10	µA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20$ V	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	$I_D = 1$ mA $V_{DS} = V_{GS}$	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500$ mA $V_{GS} = 10$ V	-	-	6	Ω
$R_{DS(on)}$	drain-source on-resistance	$I_D = 100$ mA $V_{GS} = 2.5$ V	-	-	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$I_D = 300$ mA $V_{DS} = 25$ V	200	400	-	mS
C_{iss}	input capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	65	90	pF
C_{oss}	output capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	20	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	5	10	ns
t_{off}	turn-off time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

VN2406L

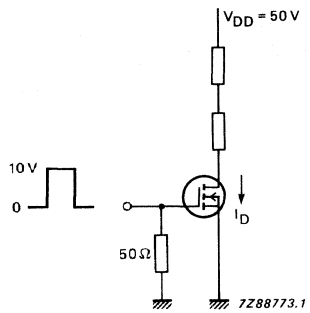


Fig.2 Switching time test circuit.

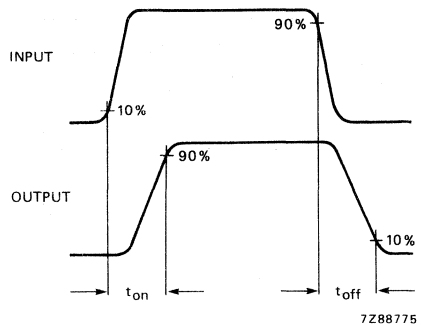


Fig.3 Input and output waveforms.

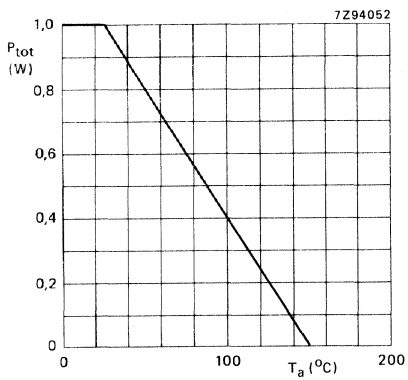


Fig.4 Power derating curve.

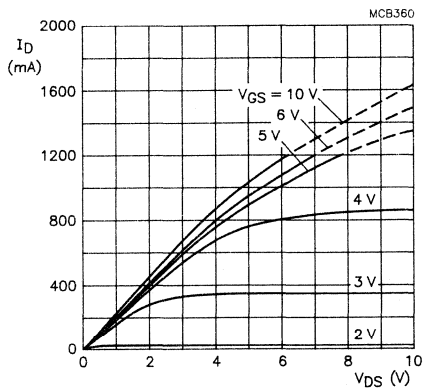


Fig.5 Typical output characteristics; T_j = 25 °C;.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

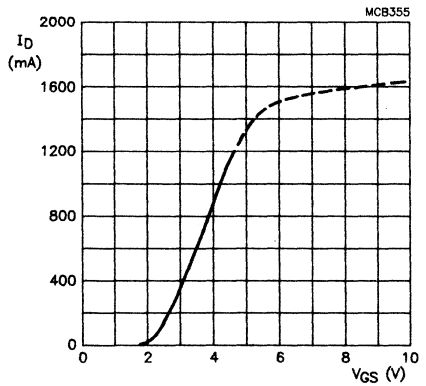


Fig.6 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25 °C;.

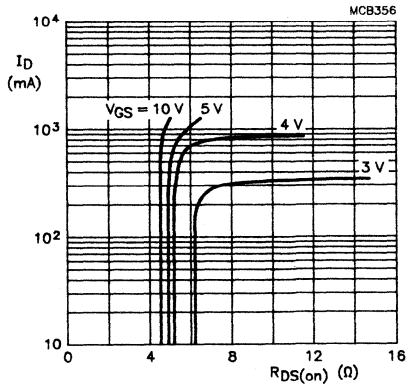


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C;.

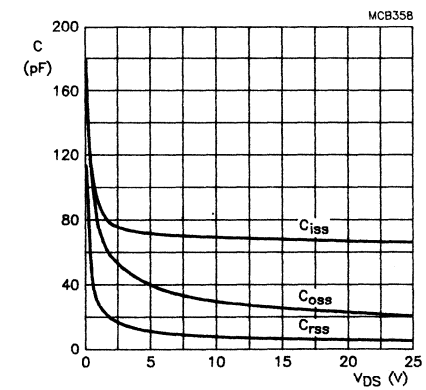


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C;.

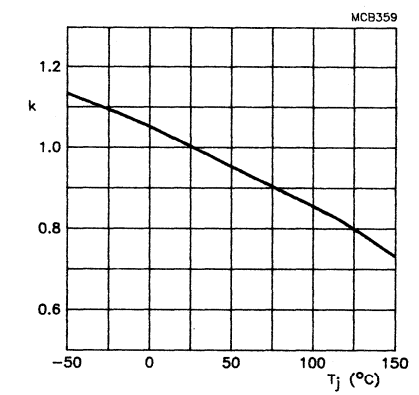


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{+V_{GS(th)} \text{ at } T_j}{+V_{GS(th)} \text{ at } 25\ °C}$$; $V_{GS(th)}$ at 1 mA; typical values.

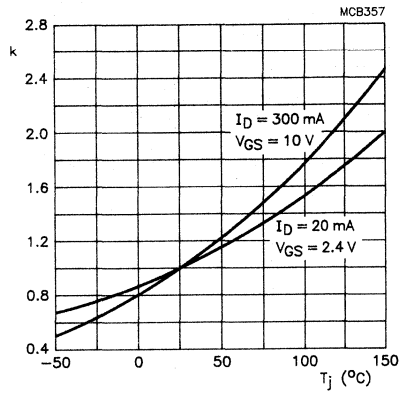


Fig.10 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

FEATURES

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	240	V
V_{GSth}	gate-source threshold voltage	2	V
I_D	drain current (DC)	150	mA
R_{DSon}	drain-source on-state resistance	10	Ω

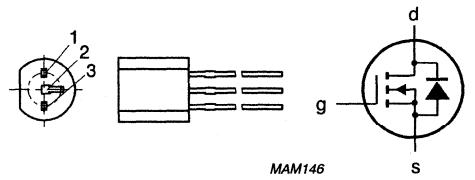


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	40	V
I_D	drain current	DC value	-	150	mA
I_{DM}	drain current	peak value	-	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100$ µA $V_{GS} = 0$	240	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120$ V $V_{GS} = 0$	-	-	10	µA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20$ V	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	$I_D = 1$ mA $V_{DS} = V_{GS}$	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500$ mA $V_{GS} = 10$ V	-	-	10	Ω
$R_{DS(on)}$	drain-source on-resistance	$I_D = 100$ mA $V_{GS} = 2.5$ V	-	-	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$I_D = 300$ mA $V_{DS} = 25$ V	200	400	-	mS
C_{iss}	input capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	65	90	pF
C_{oss}	output capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	20	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	5	10	ns
t_{off}	turn-off time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

VN2410L

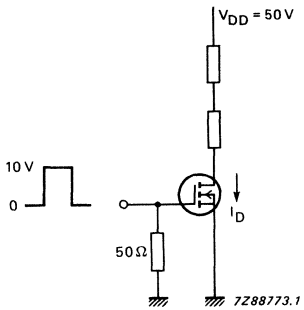


Fig.2 Switching time test circuit.

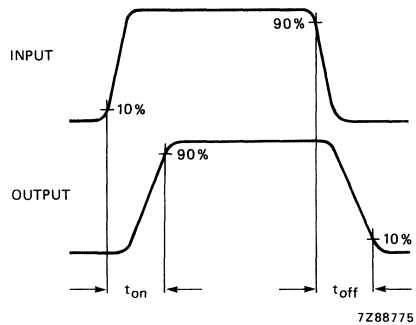


Fig.3 Input and output waveforms.

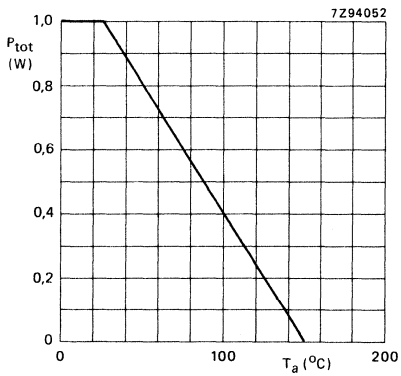


Fig.4 Power derating curve.

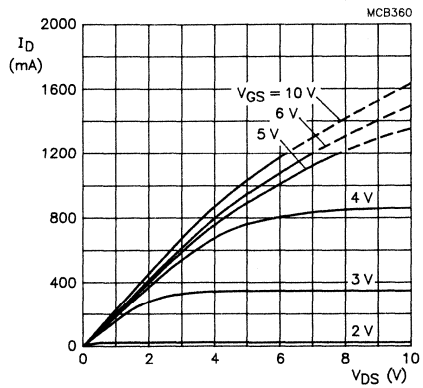


Fig.5 Typical output characteristics; T_j = 25 °C;.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

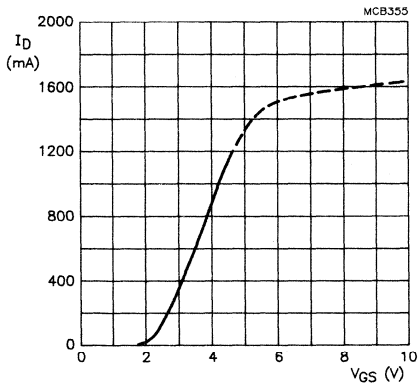


Fig.6 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25 °C;.

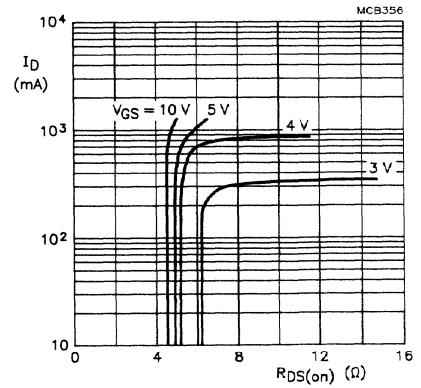


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C;.

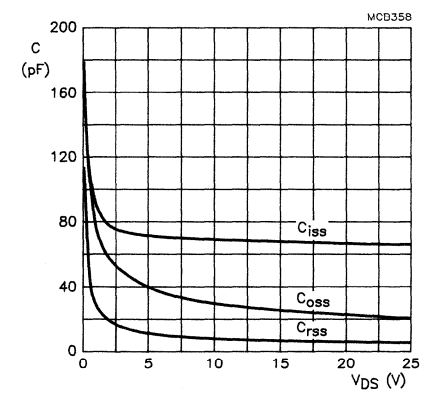


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C;.

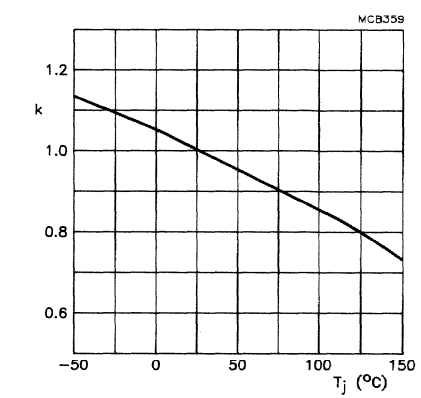


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{+V_{GS(th)} \text{ at } T_j}{+V_{GS(th)} \text{ at } 25\ °C}$$; $V_{GS(th)}$ at 1 mA; typical values.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

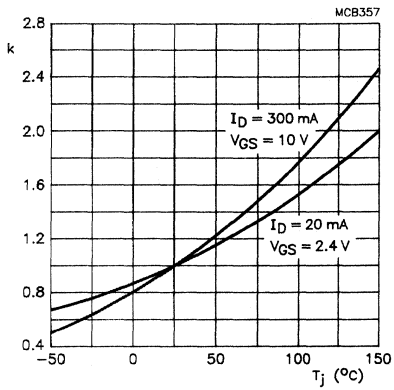


Fig.10 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage		$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C		P_{tot}	max		1.5		W
				2N4091	**2N4092**	**2N4093**	
Drain current							
V_{DS} = 20 V; V_{GS} = 0		I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage			>	5,0	2,0	1,0	V
I_D = 1 nA; V_{DS} = 20 V		$-V_{(P)GS}$	<	10	7,0	5,0	V
Drain-source resistance (on) at f = 1 kHz							
I_D = 0; V_{GS} = 0		$R_{DS\,on}$	<	30	50	80	Ω
Feedback capacitance at f = 1 MHz							
V_{DS} = 0; $-V_{GS}$ = 20 V		C_{rs}	<		5,0		pF
Turn-off time							
V_{DD} = 3,0 V; V_{GS} = 0							
I_D = 6,6 mA; $-V_{GSM}$ = 12 V	**2N4091**	t_{off}	<		40		ns
I_D = 4,0 mA; $-V_{GSM}$ = 8 V	**2N4092**	t_{off}	<		60		ns
I_D = 2,5 mA; $-V_{GSM}$ = 6 V	**2N4093**	t_{off}	<		80		ns

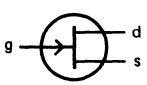
MECHANICAL DATA

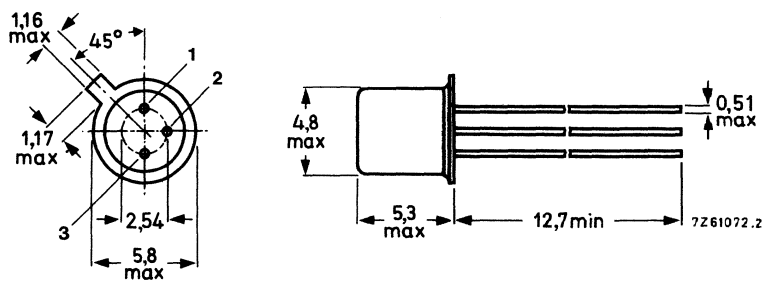
Dimensions in mm

Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate





Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Current				
Forward gate current (DC)	I_G	max.	10	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−55 to	+175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to case in free air	$R_{th\ j\text{-}c}$	=	100	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4091	2N4092	2N4093	
Drain currents						
V_{DG} = 20 V; I_S = 0	I_{DGO}	<	0.2			nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<	0.4			µA
Source current						
V_{SG} = 20 V; I_D = 0	I_{SGO}	<	0.2			nA
Drain cut-off current						
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.2	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 8 V	I_{DSX}	<	–	0.2	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 6 V	I_{DSX}	<	–	–	0.2	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX}	<	0.4	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 8 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.4	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 6 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.4	µA
Gate-source breakdown voltage						
$-I_G$ = 1.0 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Drain current [1]						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V
Drain-source voltages (on)						
I_D = 6.6 mA; V_{GS} = 0	V_{DSon}	<	0.2	–	–	V
I_D = 4.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.2	–	V
I_D = 2.5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.2	V
Drain- source resistance (on)						
I_D = 1.0 mA; V_{GS} = 0	R_{DSon}	<	30	50	80	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	30	50	80	Ω

[1]) Measured under pulsed conditions: $t_p \leq 300$ µs; $\delta \leq 0.03$

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

y-parameters at f = 1 MHz (common source)

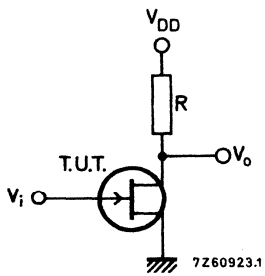
Input capacitance				
V_{DS} = 20 V ; V_{GS} = 0	C_{is}	<	16	pF
Feedback capacitance				
V_{DS} = 0 ; $-V_{GS}$ = 20 V	C_{rs}	<	5	pF

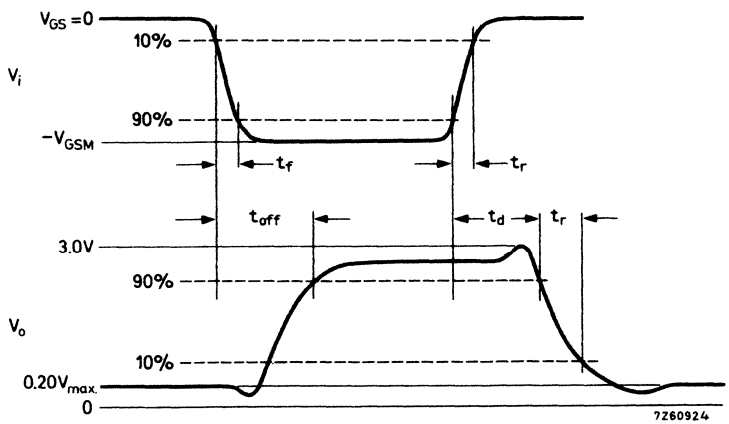
Switching times

V_{DD} = 3,0 V; V_{GS} = 0

			2N4091	2N4092	2N4093	
	I_D	=	6,6	4,0	2,5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:





$$R = \frac{2,8}{I_D}$$

Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	µs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	MΩ
C_i	<	1,7	pF

N-channel junction FETs 2N4220/A; 2N4221/A; 2N4222/A

FEATURES

- High gain in VHF range
- Low receiver noise figure

DESCRIPTION

Symmetrical N-channel junction FETs in a TO-72 envelope. Intended for use as a VHF amplifier and in oscillators and mixers.

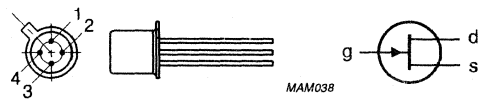


Fig.1 Simplified outline and symbol.

PINNING - TO-72

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	shield lead connected to case

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	30	V
$-V_{GS}$	gate-source voltage		-	30	V
V_{DG}	drain-gate voltage		-	30	V
I_D	drain current		-	15	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	300	mW
T_{stg}	storage temperature range		−65	175	°C
T_j	junction temperature		-	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

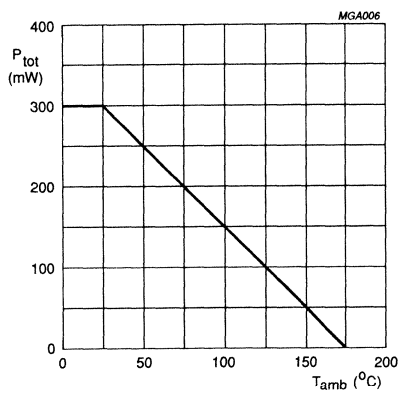


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 10 μA V_{DS} = 0		30	-	-	V
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 15 V V_{DS} = 0		-	-	0.1	nA
		$-V_{GS}$ = 15 V V_{DS} = 0 T_{amb} = 150 °C		-	-	100	nA
I_{DSS}	drain-source current	V_{DS} = 15 V V_{GS} = 0	2N4220/A 2N4221/A 2N4222/A	0.5 2 5	- - -	3 6 15	mA mA mA
$-V_{GS}$	gate-source voltage	V_{DS} = 15 V I_D = 50 μA	2N4220/A	0.5	-	2.5	V
		V_{DS} = 15 V I_D = 200 μA	2N4221/A	1	-	5	V
		V_{DS} = 15 V I_D = 500 μA	2N4222/A	2	-	6	V
$-V_{P(GS)}$	gate-source cut-off voltage	V_{DS} = 15 V I_D = 0.1 nA	2N4220/A 2N4221/A 2N4222/A	- - -	- - -	4 6 8	V V V
$\|g_{fs}\|$	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N4220/A 2N4221/A 2N4222/A	1 2 2.5	- - -	4 5 6	mS mS mS
$\|y_{fs}\|$	transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz		750	-	-	μS
$\|y_{os}\|$	output admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N4220/A 2N4221/A 2N4222/A	- - -	- - -	10 20 40	μS μS μS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	4.5	6	pF
$-C_{rss}$	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	1.2	2	pF
C_{oss}	output capacitance	V_{DS} = 15 V V_{GS} = 0 f = 30 MHz		-	1.5	-	pF
$R_{DS(on)}$	drain-source on resistance	V_{DS} = 0 V_{GS} = 0	2N4220/A 2N4221/A 2N4222/A	- - -	500 400 300	- - -	Ω Ω Ω
F	noise figure	V_{DS} = 15 V V_{GS} = 0 R_S = 1 MΩ f = 100 Hz	2N4220A 2N4221A 2N4222A	-	-	2.5	dB

N-channel junction FETs 2N4340

FEATURES

- Low noise, noise figure < 1 dB
- High off isolation.

DESCRIPTION

Symmetrical N-channel silicon junction field-effect transistor in a TO-18 metal envelope. Intended for use in small-signal audio amplifiers, as a switch in choppers and as a voltage controlled resistor.

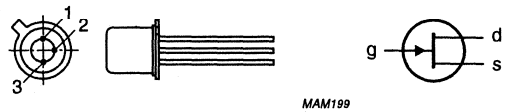


Fig.1 Simplified outline and symbol.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	drain
3	gate

Note

1. Drain and source are interchangeable.

N-channel J-FET 2N4340

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{GD}$	gate-drain voltage		-	50	V
$-V_{GS}$	gate-source voltage		-	50	V
I_G	gate current		-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	300	mW
T_{stg}	storage temperature range		−65	200	°C
T_j	junction temperature		-	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

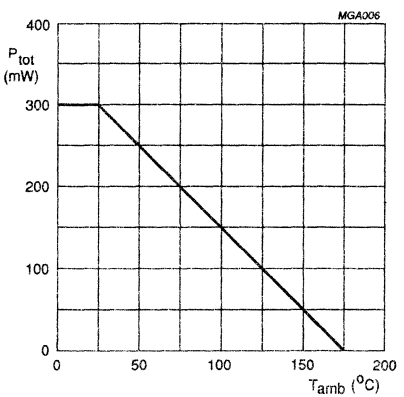


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel J-FET 2N4340

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 $-I_G$ = 1 µA	50	-	-	V
I_{DSS}	drain-source current	V_{GS} = 0 V_{DS} = 15 V	1.2	-	3.6	mA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 5 V V_{DS} = 15 V	-	-	0.05	nA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 30 V	-	-	0.1	nA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 30 V T_{amb} = 150 °C	-	-	0.1	µA
$-V_{P(GS)}$	gate-source cut-off voltage	I_D = 0.1 µA V_{DS} = 15 V	1	-	3	V
$r_{ds(on)}$	drain-source on resistance	V_{DS} = 0 V_{GS} = 0 f = 1 kHz	-	-	1.5	kΩ
g_{fs}	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	1.3	-	3	mS
g_{os}	output conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	-	-	30	µS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	-	7	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	-	3	pF
F	noise figure	V_{GS} = 0 V_{DS} = 15 V R_G = 1 MΩ f = 1 kHz B = 200 Hz	-	-	1	dB

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.		1.5		W
			2N4391	**2N4392**	**2N4393**	
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage		>	4,0	2,0	0,5	V
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	<	10	5,0	3,0	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz						
V_{DS} = 0; $-V_{GS}$ = 12 V **2N4391**						
V_{DS} = 0; $-V_{GS}$ = 7 V **2N4392**	C_{rs}	<	3,5	3,5	3,5	pF
V_{DS} = 0; $-V_{GS}$ = 5 V **2N4393**						
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSoff}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6,0 mA; $-V_{GSoff}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3,0 mA; $-V_{GSoff}$ = 5 V	t_{off}	<	–	–	50	ns

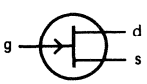
MECHANICAL DATA

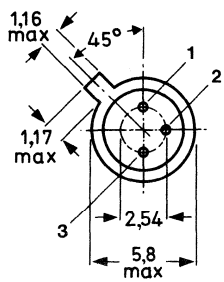
Dimensions in mm

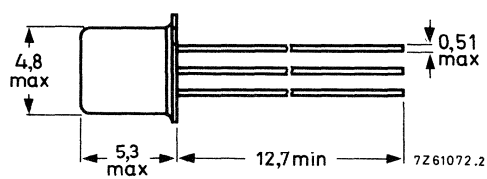
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to +175		°C
Junction temperature	T_j	max.	175	°C
From junction to case in free air	$R_{th\ j\text{-}c}$	=	100	K/W

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off current

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$ <	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$ <	0.2	µA

Drain cut-off current

		2N4391	2N4392	2N4393	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX} <	0.1	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 7 V	I_{DSX} <	–	0.1	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 5 V	I_{DSX} <	–	–	0.1	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX} <	0.2	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 7 V; T_{amb} = 150 °C	I_{DSX} <	–	0.2	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 5 V; T_{amb} = 150 °C	I_{DSX} <	–	–	0.2	µA

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

			2N4391	2N4392	2N4393	
Drain currents (note 1)						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.4	–	V
I_D = 3.0 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	–	pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	–	pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5	pF

Note

1. measured under pulsed conditions: t_p = 100 μs; δ = 0.01

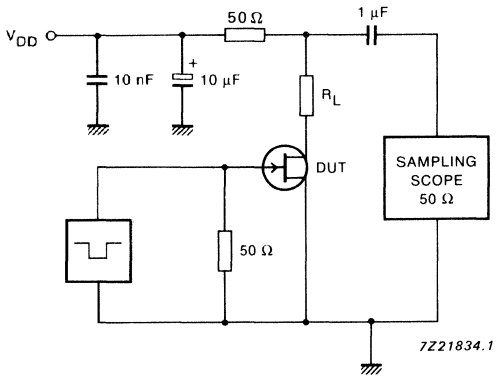
CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

Switching times

V_{DD} = 10 V; V_{GS} = 0

		2N4391	2N4392	2N4393	
I_D	=	12	6.0	3.0	mA
$-V_{GSoff}$	=	12	7	5	V
R_L	=	750	1550	3150	Ω
Rise time t_r	<	5	5	5	ns
Turn on time t_{on}	<	15	15	15	ns
Fall time t_f	<	15	20	30	ns
Turn off time t_{off}	<	20	35	50	ns

Test circuit:

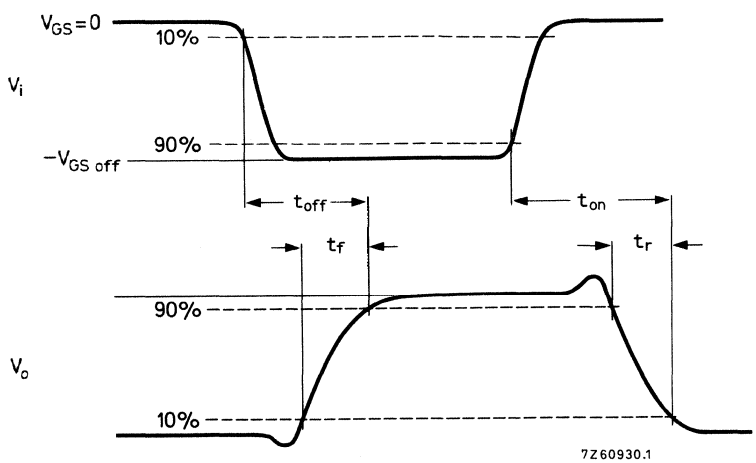


Pulse generator:

t_r	<	0.5 ns
t_f	<	0.5 ns
t_p	=	100 µs
δ	=	0.01

Oscilloscope:

R_i = 50 Ω



N-channel field-effect transistor 2N4416; 2N4416A

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel symmetrical silicon junction FETs in a TO-72 envelope, with shield connected to the case. These devices are intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - TO-72.

PIN	DESCRIPTION
1	source
2	drain
3	gate
4	shield

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N4416		–	–6	V
	2N4416A		–2.5	–6	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	4.5	7.5	mS

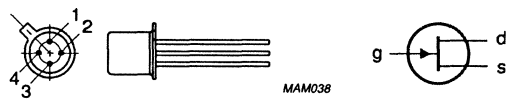


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
V_{GSO}	gate-source voltage				
	2N4416		–	–30	V
	2N4416A		–	–35	V
V_{GDO}	gate-drain voltage				
	2N4416		–	–30	V
	2N4416A		–	–35	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+175	°C
T_j	junction temperature		–	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	590 K/W

Note

1. Mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm².

STATIC CHARACTERISTICS

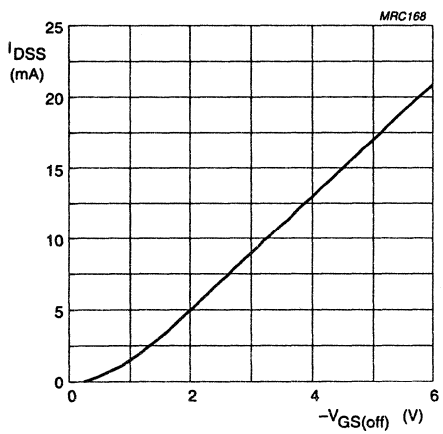
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA			
	2N4416		–30	–	V
	2N4416A		–35	–	V
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–0.1	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0	5	15	mA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N4416		–	–6	V
	2N4416A		–2.5	–6	V
$\lvert Y_{fs}\rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	4.5	7.5	mS
$\lvert Y_{os}\rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N4416		–	50	μS
	2N4416A		–	50	μS

DYNAMIC CHARACTERISTICS

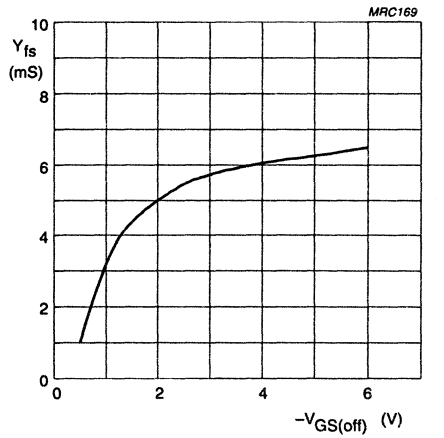
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	4	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	0.8	pF
g_{is}	common source input conductance	f = 100 MHz	–	–	100	µS
		f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance	f = 100 MHz	–	5.2	–	mS
		f = 400 MHz	4	5	–	mS
g_{rs}	common source feedback conductance	f = 100 MHz	–	–8	–	µS
		f = 400 MHz	–	–100	–	µS
g_{os}	common source output conductance	f = 100 MHz	–	–	75	µS
		f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√HZ



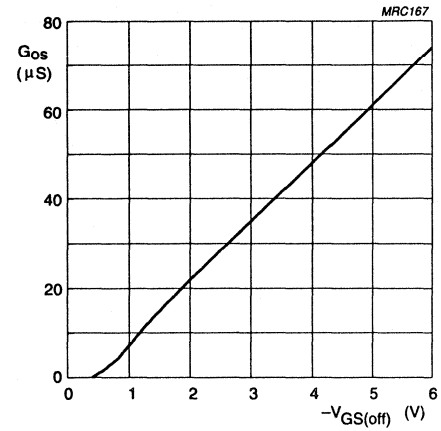
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage; typical values.



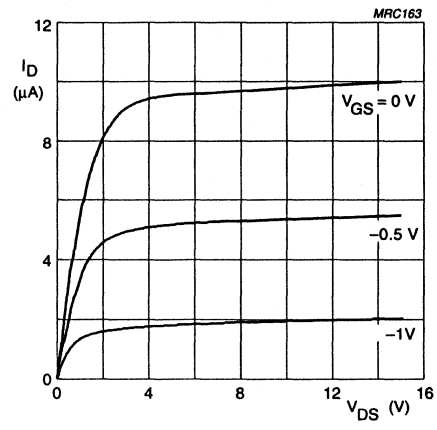
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage; typical values.



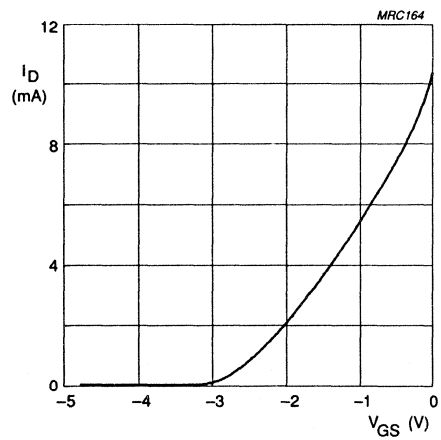
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Common source output conductance as a function of gate-source cut-off voltage; typical values.



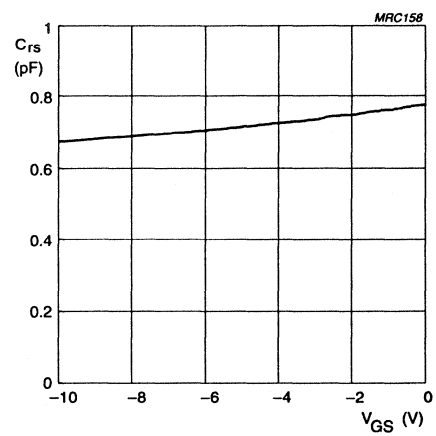
T_j = 25 °C.

Fig.5 Typical output characteristics.



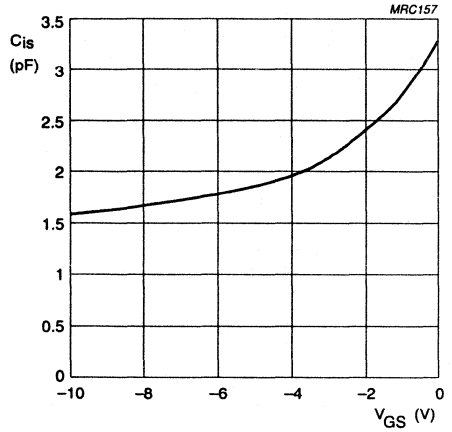
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Typical input characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input capacitance.

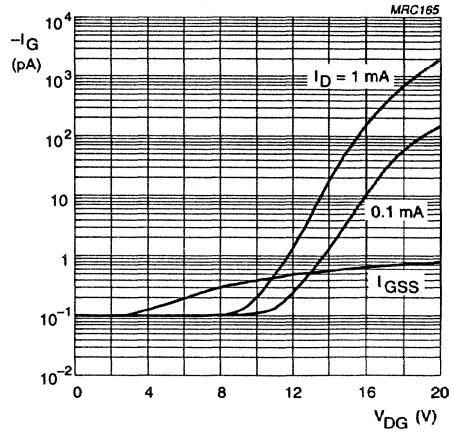


Fig.9 Gate current as a function of drain-gate voltage, typical values.

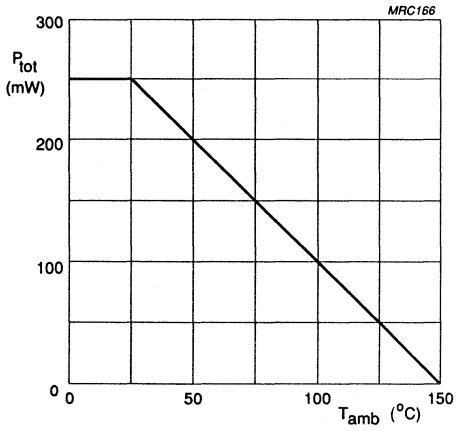
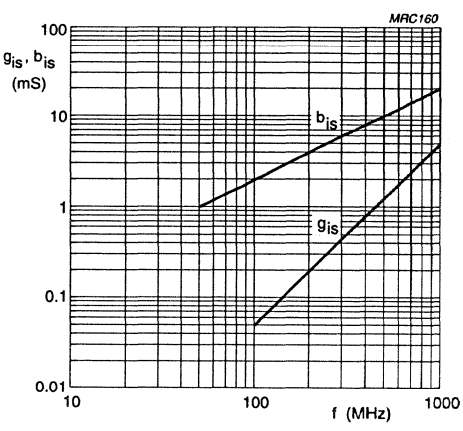
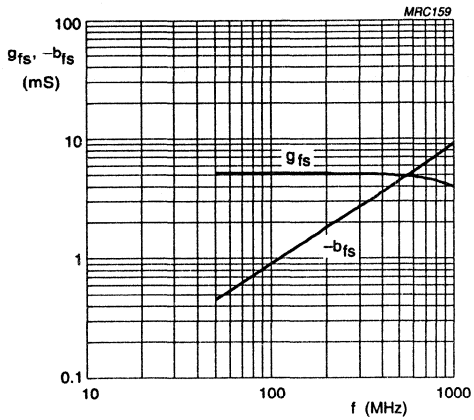


Fig.10 Power derating curve.



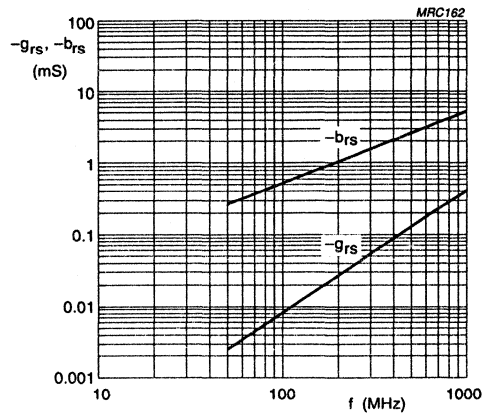
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.11 Common source input conductance; typical values.



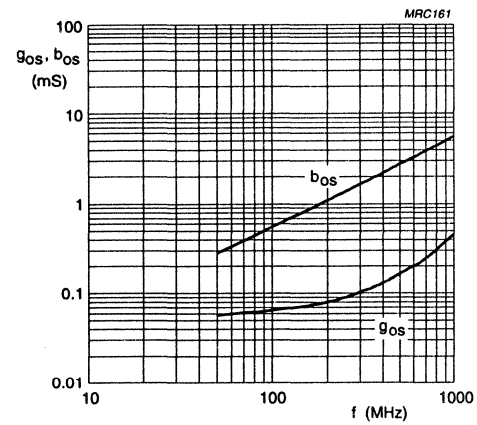
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Common source transfer conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source feedback conductance; typical values.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common source output conductance; typical values.

SPICE parameters for 2N4416

September 1992; version 1.0.

1	VTO = −3.553	V
2	BETA = 792.6	μA/V²
3	LAMBDA = 18.46	m/V
4	RD = 7.671	Ω
5	RS = 7.671	Ω
6	IS = 333.4	aA
7	CGSO = 2.920	pF
8	CGDO = 2.261	pF
9	PB = 1.090	V
10 (note 1)	FC = 500.0	m

Note

1. Parameter not extracted; default value.

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	**2N4856 to 2N4858**	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to T_{amb} = 25 °C		P_{tot}	max.		360		mW
				2N4856 2N4859	**2N4857 2N4860**	**2N4858 2N4861**	
Drain current V_{DS} = 15 V; V_{GS} = 0		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage I_D = 0,5 nA; V_{DS} = 15 V		$-V_{(P)GS}$	>	4	2	0,8	V
			<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0		$R_{DS\,on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V		C_{rs}	<		8		pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0							
I_D = 20 mA; $-V_{GSM}$ = 10 V	**2N4856; 2N4859**	t_{off}	<		25		ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	**2N4857; 2N4860**	t_{off}	<		50		ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	**2N4858; 2N4861**	t_{off}	<		100		ns

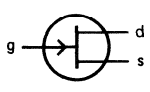
MECHANICAL DATA

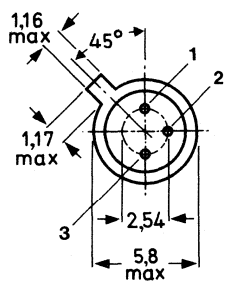
Dimensions in mm

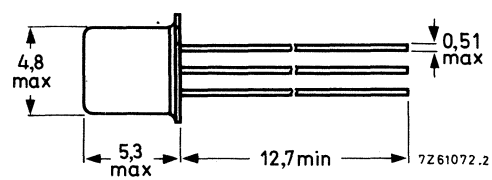
Fig. 1 TO-18

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Gate current (d.c.)	I_G	max.	50		mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300		mW
Storage temperature range	T_{stg}	−65 to	+175		^oC
Junction temperature	T_j	max.	175		^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	490	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0.5	–	µA
$-V_{GS}$ = 15 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	–	0.5	µA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	<	0.25	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 10 V; T_{amb} = 150 °C	I_{DSX}	<	0.5	0.5	µA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1]						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

			2N4856 2N4857	2N4859 2N4860	
Gate-source breakdown voltage					
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$		40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	0.75	–	–	V
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	0.50	–	V
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\,on}$	<	25	40	60	Ω

[1]) measured under pulsed conditions: t_p = 100 ms; $\delta \leq 0.1$

y-parameters (common source)
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz

Input capacitance	C_{is}	<	18	pF
Feedback capacitance	C_{rs}	<	8	pF

Switching times (see Figs 2 and 3)
V_{DD} = 10 V; V_{GS} = 0

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current	I_D	=	20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

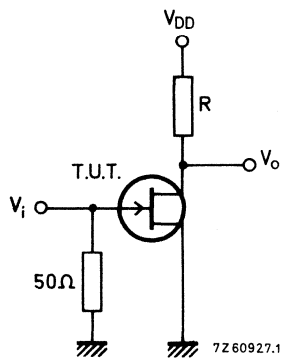


Fig. 2 Switching times test circuit.

	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
R =	464	953	1910	Ω

Pulse generator:
$t_r \leqslant$ 1 ns
$t_f \leqslant$ 1 ns
δ = 0,02
Z_o = 50 Ω

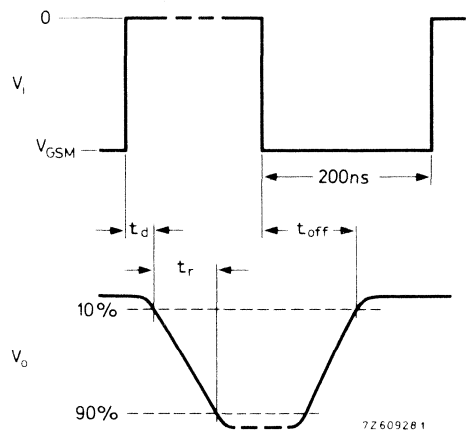


Fig. 3 Input and output waveforms.

Oscilloscope:
$t_r \leqslant$ 0,75 ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2,5 pF

P-channel junction FET 2N5116

FEATURES

- P-channel complement of 2N4393
- Short sample and hold aperture time

DESCRIPTION

P-channel junction FET in a TO-18 metal envelope. Intended for applications as an analog switch on commutators and choppers and as an integrator reset switch.

Fig.1 Simplified outline and symbol.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	gate
3	drain

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{GD}	gate-drain voltage		-	30	V
V_{GS}	gate-source voltage		-	30	V
$-I_G$	gate current		-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	500	mW
T_{stg}	storage temperature range		–65	200	°C
T_j	junction temperature		-	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

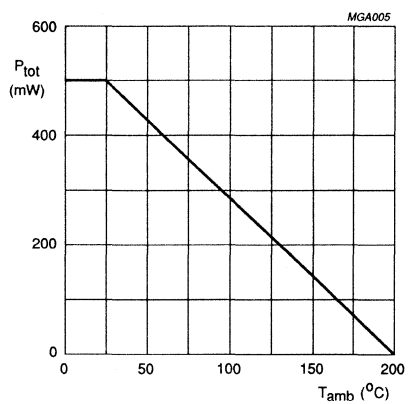


Fig.2 Total power dissipation as a function of ambient temperature.

P-channel J-FET 2N5116

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 I_G = 1 µA	30	-	V
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0	-	0.5	nA
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0 T_{amb} = 150 °C	-	1	µA
$-I_{DSX}$	drain cut-off current	V_{GS} = 5 V $-V_{DS}$ = 15 V	-	0.5	nA
$-I_{DSX}$	drain cut-off current	V_{GS} = 5 V $-V_{DS}$ = 15 V T_{amb} = 150 °C	-	1	µA
$-I_{DSS}$	drain current	V_{GS} = 0 $-V_{DS}$ = 15 V	5	25	mA
$-V_{GS}$	gate-source voltage	$-I_G$ = 1 mA V_{DS} = 0	-	1	V
$V_{P(GS)}$	gate-source cut-off voltage	$-V_{DS}$ = 15 V $-I_D$ = 1 nA	1	4	V
$-V_{(DS)on}$	drain-source on voltage	V_{GS} = 0 $-I_D$ = 3 mA	-	0.6	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 0 $-I_D$ = 1 mA	-	150	Ω
$r_{ds(on)}$	drain-source on resistance	V_{GS} = 0 I_D = 0 f = 1 kHz	-	150	Ω
C_{iss}	input capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz	-	27	pF
C_{rss}	feedback capacitance	V_{DS} = 0 V_{GS} = 5 V f = 1 MHz	-	7	pF
Switching times					
t_d	delay time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	25	ns
t_r	rise time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	35	ns
$t_{d(off)}$	delay time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	20	ns
t_f	fall time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	60	ns

P-channel junction FETs 2N5460; 2N5461; 2N5462

DESCRIPTION

P-channel silicon junction FET in a TO-92 plastic envelope. Intended for use as an analog switch and an amplifier.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	drain
3	source

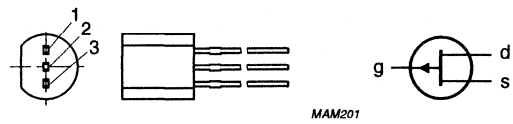


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	40	V
V_{GS}	gate-source voltage		-	40	V
$-I_G$	gate current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 40$ °C	-	310	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	355	K/W

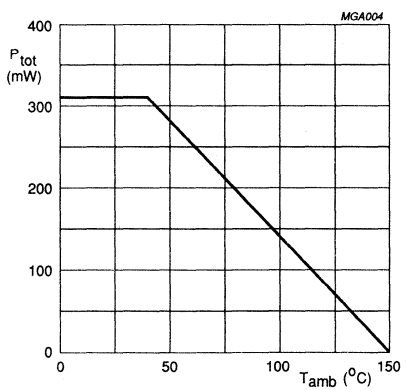


Fig.2 Total power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0		-	5	nA
		V_{GS} = 20 V V_{DS} = 0 T_{amb} = 100 °C		-	1	µA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 15 V V_{GS} = 0	2N5460 2N5461 2N5462	1 2 4	5 9 16	mA mA mA
V_{GS}	gate-source voltage	$-I_D$ = 0.1 mA $-V_{DS}$ = 15 V	2N5460	0.5	4	V
V_{GS}	gate-source voltage	$-I_D$ = 0.2 mA $-V_{DS}$ = 15 V	2N5461	0.8	4.5	V
V_{GS}	gate-source voltage	$-I_D$ = 0.4 mA $-V_{DS}$ = 15 V	2N5462	1.5	6	V
$V_{P(GS)}$	gate-source cut-off voltage	$-I_D$ = 1 µA $-V_{DS}$ = 15 V	2N5460 2N5461 2N5462	0.75 1 1.8	6 7.5 9	V V V
$\|y_{fs}\|$	transfer admittance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 kHz	2N5460 2N5461 2N5462	1 1.5 2	4 5 6	mS mS mS
$\|y_{os}\|$	output admittance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 kHz		-	75	µS
C_{iss}	input capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz		-	7	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz		-	2	pF
NF	noise figure	$-V_{DS}$ = 15 V V_{GS} = 0 f = 100 Hz B = 1 Hz		-	2.5	dB

N-channel field-effect transistors 2N5484; 2N5485; 2N5486

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

N-channel, symmetrical, silicon junction FETs in a SOT54 (TO-92) envelope, intended for use in VHF/UHF amplifiers, oscillators and mixers.

PINNING - SOT54 (TO-92)

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		1	5	mA
	2N5485		4	10	mA
	2N5486		8	20	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	400	mW
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N5484		−0.3	−3	V
	2N5485		−0.5	−4	V
	2N5486		−2	−6	V
$\lvert Y_{fs} \rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz			
	2N5484		3	6	mS
	2N5485		3.5	7	mS
	2N5486		4	8	mS

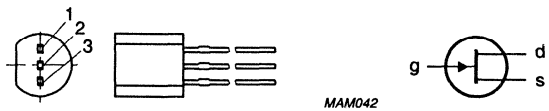


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	25	V
V_{GSO}	gate-source voltage		–	–25	V
V_{GDO}	gate-drain voltage		–	–25	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	400	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	350 K/W

Note

1. Device mounted on a printed circuit board; maximum lead length 3 mm; mounting pad for drain lead minimum 10 mm x 10 mm.

STATIC CHARACTERISTICS

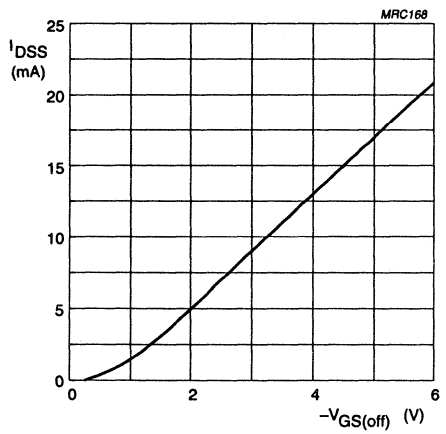
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; I_G = –1 μA	–25	–	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		1	5	mA
	2N5485		4	10	mA
	2N5486		8	20	mA
I_{GSS}	reverse gate leakage current	V_{DS} = 0; V_{GS} = –15 V	–	–1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	1	V
$V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 nA			
	2N5484		–0.3	–3	V
	2N5485		–0.5	–4	V
	2N5486		–2	–6	V
$\lvert Y_{fs}\rvert$	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		3	6	mS
	2N5485		3.5	7	mS
	2N5486		4	8	mS
$\lvert Y_{os}\rvert$	common source output admittance	V_{DS} = 15 V; V_{GS} = 0			
	2N5484		–	50	μS
	2N5485		–	60	μS
	2N5486		–	75	μS

DYNAMIC CHARACTERISTICS

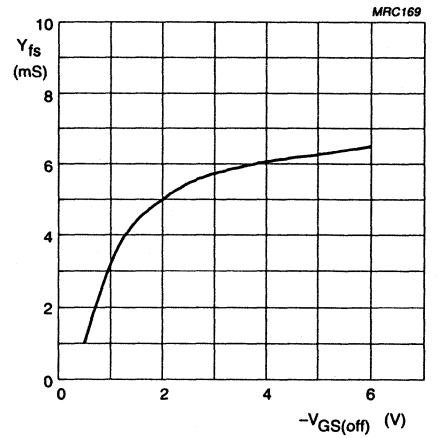
T_j = 25 °C; V_{DS} = 15 V; V_{GS} = 0

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	f = 1 MHz	–	–	5	pF
C_{os}	output capacitance	f = 1 MHz	–	–	2	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	–	1	pF
g_{is}	common source input conductance					
	2N5484	f = 100 MHz	100	–	–	µS
	2N5485; 2N5486	f = 400 MHz	–	–	1	mS
g_{fs}	common source transfer conductance					
	2N5484	f = 100 MHz	2.5	–	–	mS
	2N5485	f = 400 MHz	3	–	1	mS
	2N5486	f = 400 MHz	3.5	–	1	mS
g_{os}	common source output conductance					
	2N5484	f = 100 MHz	–	–	75	µS
	2N5485; 2N5486	f = 400 MHz	–	–	100	µS
V_n	equivalent input noise voltage	f = 100 Hz	–	5	–	nV/√Hz



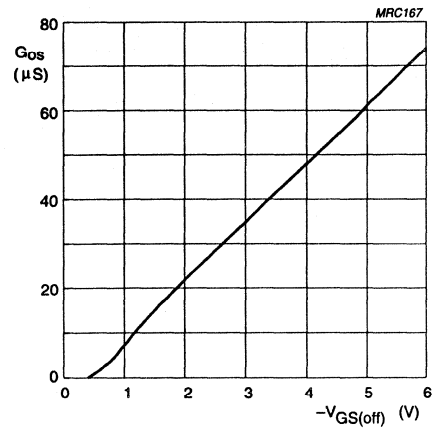
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.2 Drain current as a function of gate-source cut-off voltage.



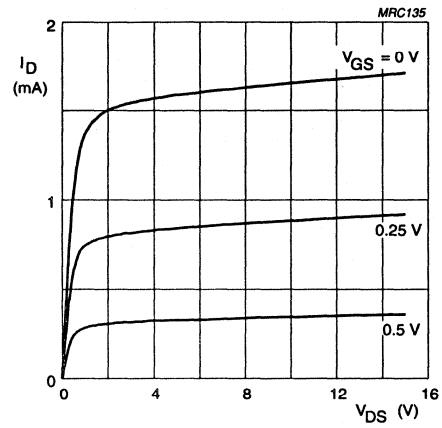
V_{DS} = 15 V; T_j = 25 °C; typical values.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



V_{DS} = 15 V; T_j = 25 °C; typical values.

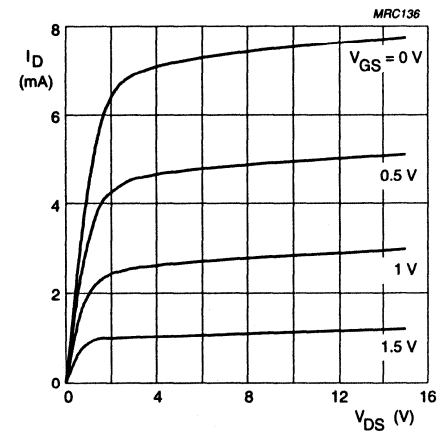
Fig.4 Common source output conductance as a function of gate-source cut-off voltage.



2N5484

T_j = 25 °C.

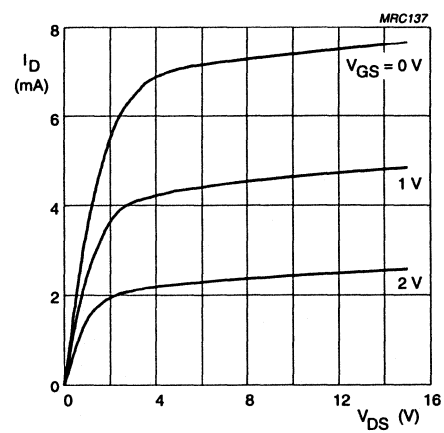
Fig.5 Typical output characteristics.



2N5485

T_j = 25 °C.

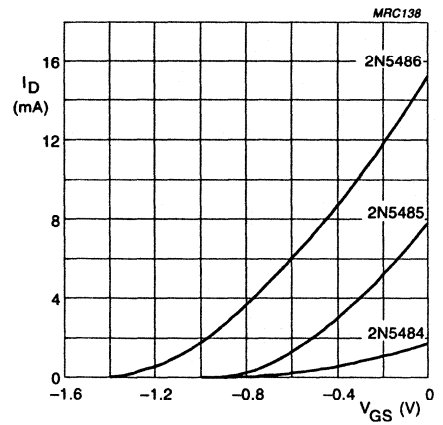
Fig.6 Typical output characteristics.



2N5486

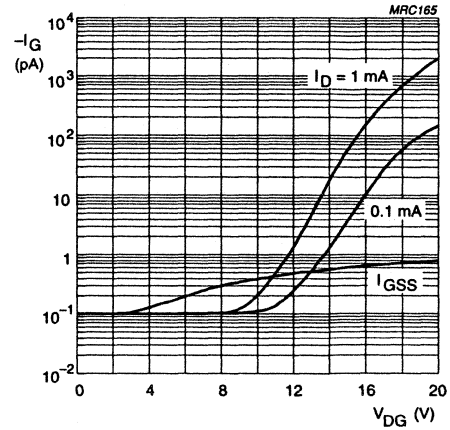
T_j = 25 °C.

Fig.7 Typical output characteristics.



V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Typical input characteristics.



T_j = 25 °C.

Fig.9 Gate current as a function of drain-gate voltage, typical values.

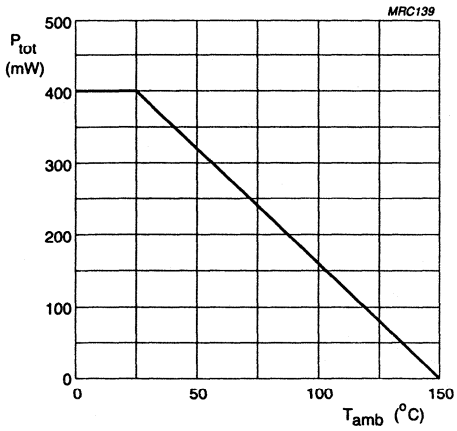
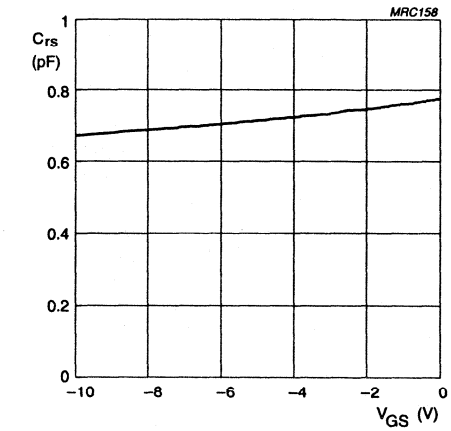
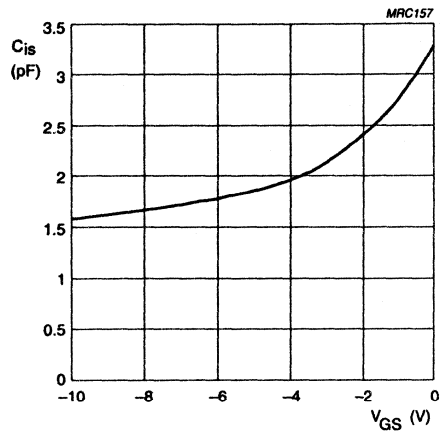


Fig.10 Power derating curve.



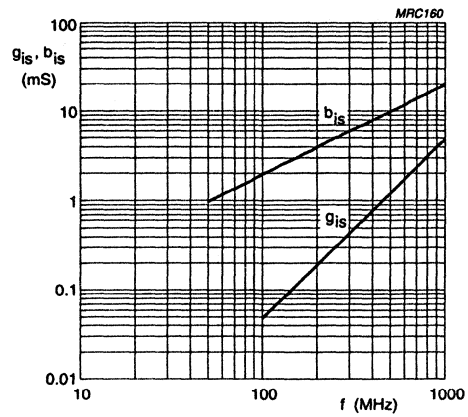
V_{DS} = 15 V; T_j = 25 °C.

Fig.11 Typical feedback capacitance.



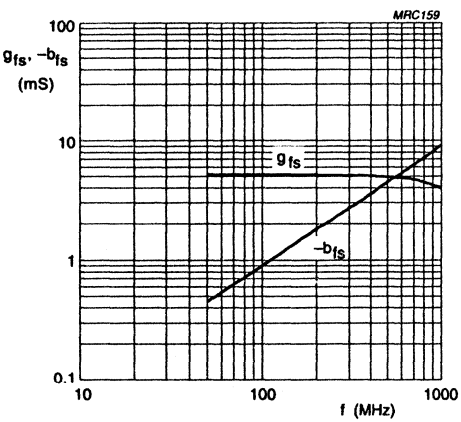
V_{DS} = 15 V; T_j = 25 °C.

Fig.12 Typical input capacitance.



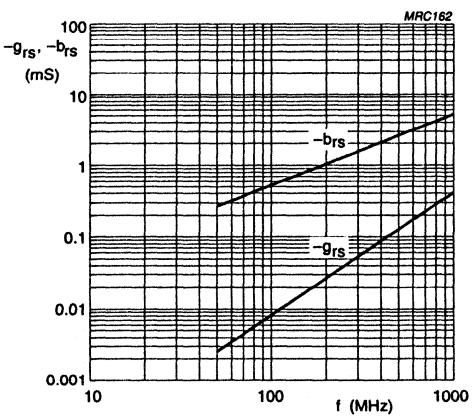
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.13 Common source input conductance.



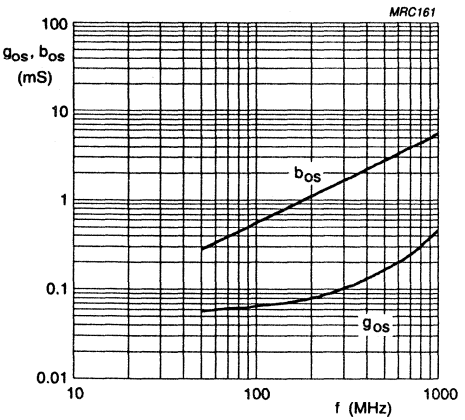
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.14 Common source transfer conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.15 Common source feedback conductance.



V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C; typical values.

Fig.16 Common source output conductance.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

2N7000
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

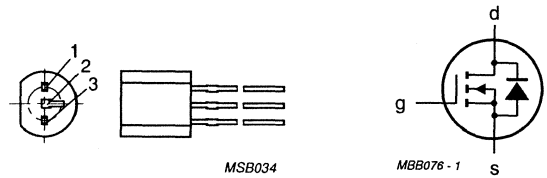


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

2N7000

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	280	mA
I_{DM}	drain current	peak value	–	1.3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

N-channel enhancement mode vertical D-MOS transistor

2N7000

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns

N-channel enhancement mode vertical D-MOS transistor

2N7000

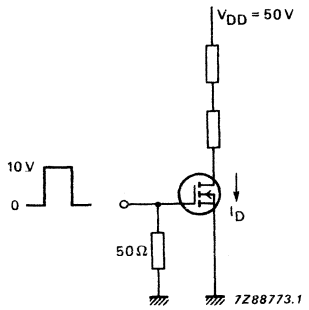


Fig.2 Switching time test circuit.

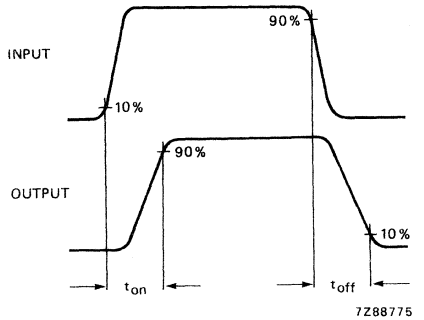


Fig.3 Input and output waveforms.

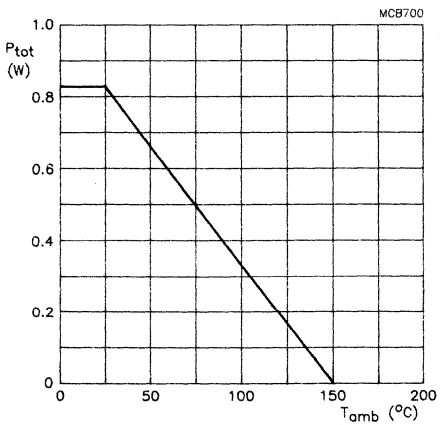


Fig.4 Power derating curve.

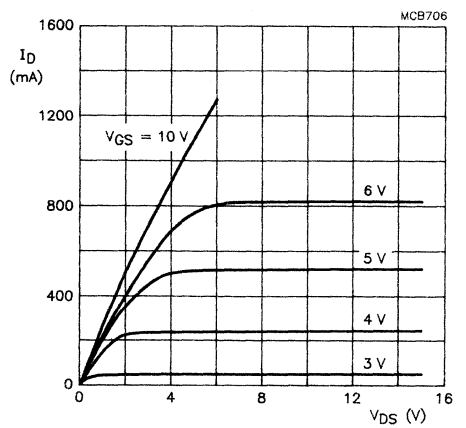


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

2N7000

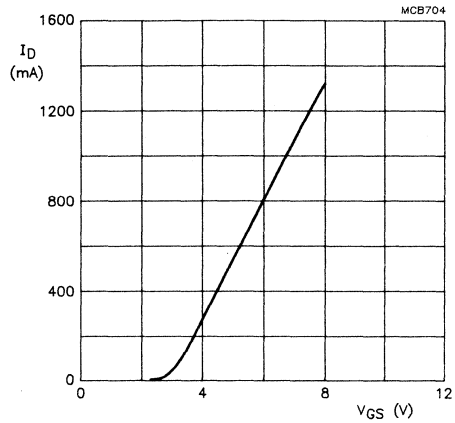


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

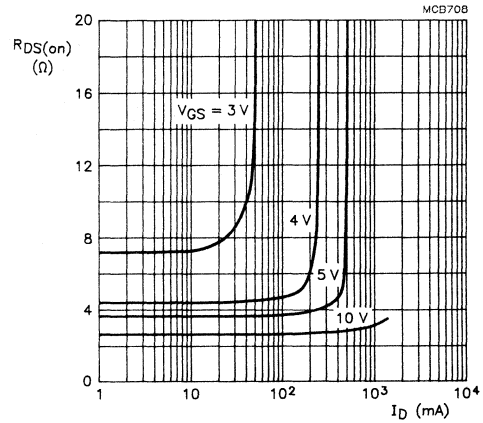


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

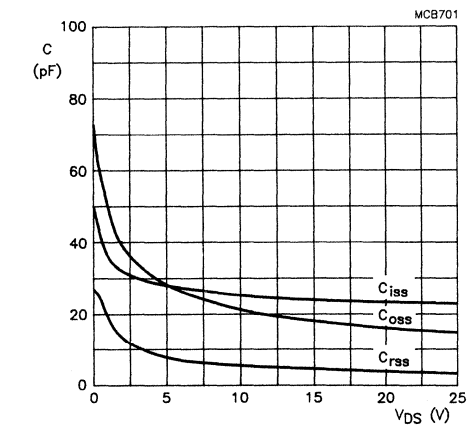
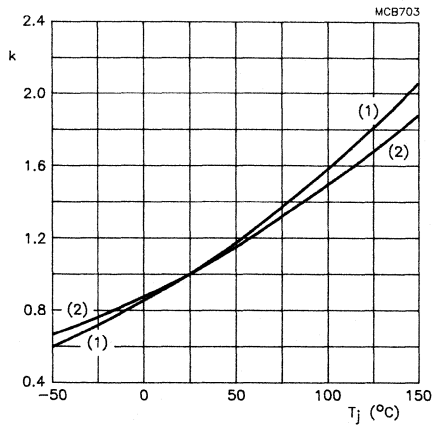


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

2N7000



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\,°C}$; typical $R_{DS(on)}$.

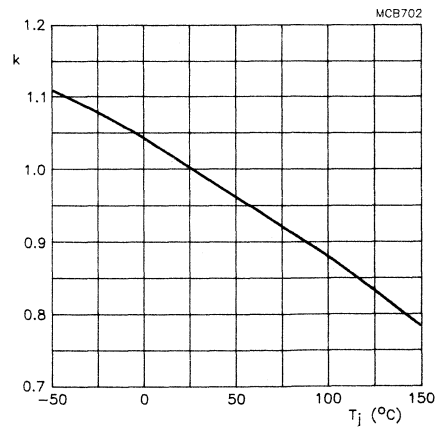


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,°C}$; typical $V_{GS(th)}$ at 1 mA.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1995

2N7002
N-channel vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

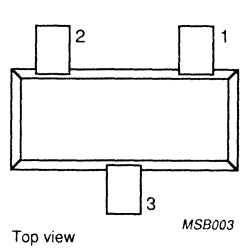
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION



Top view

Marking code: 702

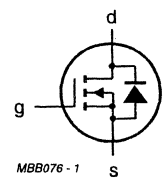


Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor

2N7002

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1) (note 2)	 – –	 300 250	 mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring 10 x 8 x 0.7 mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring 10 x 8 x 0.7 mm.
2. Mounted on a printed circuit board.

N-channel vertical D-MOS transistor

2N7002

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	15	ns

N-channel vertical D-MOS transistor

2N7002

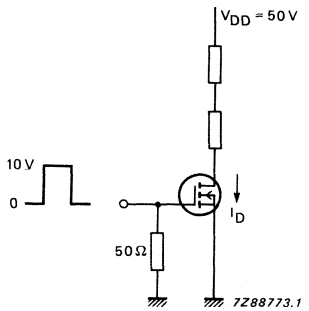


Fig.2 Switching time test circuit.

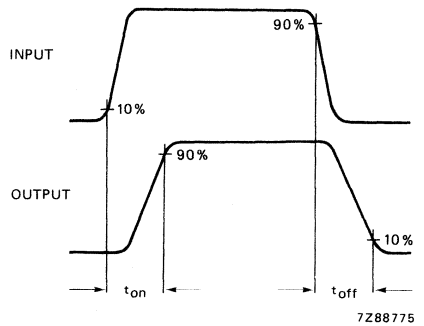
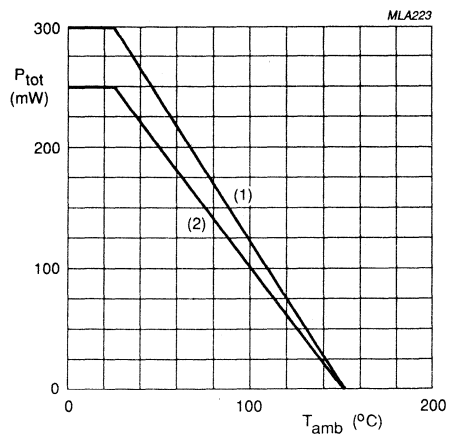


Fig.3 Input and output waveforms.



(1) On ceramic substrate.
(2) On printed circuit board.

Fig.4 Power derating curve.

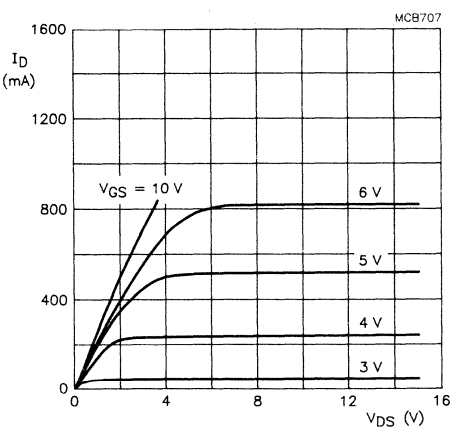


Fig.5 Typical output characteristics; T_j = 25 °C.

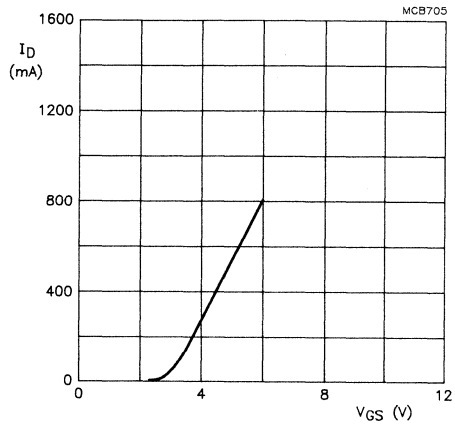


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

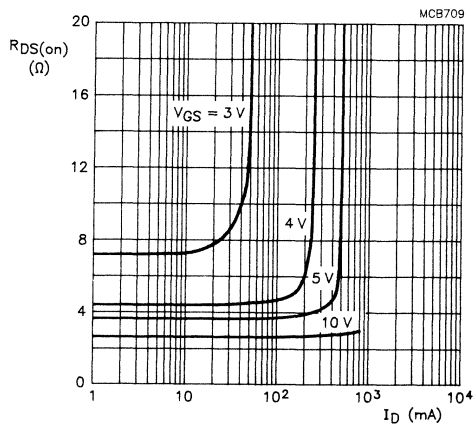


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

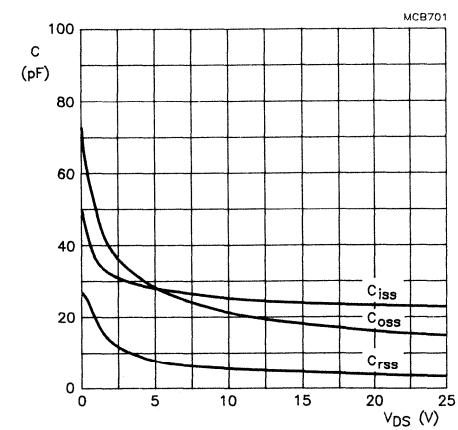
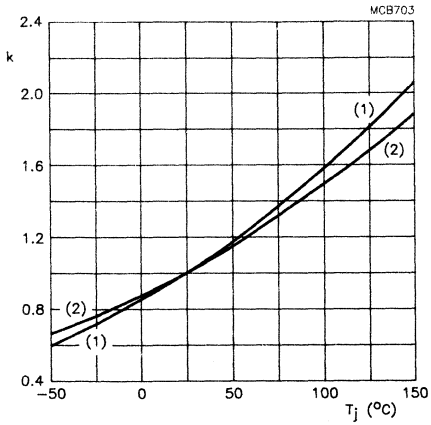


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$.

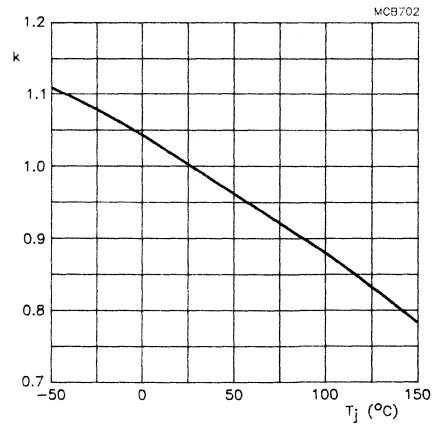
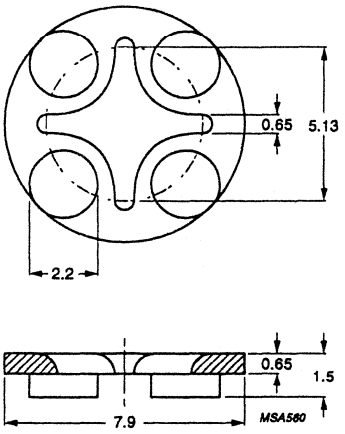


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

ACCESSORIES

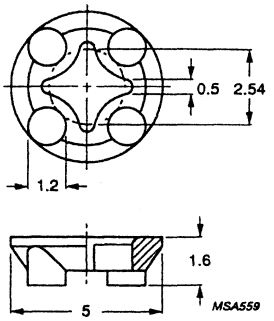
MECHANICAL DATA



Dimensions in mm.

Maximum permissible temperature: 100 °C.

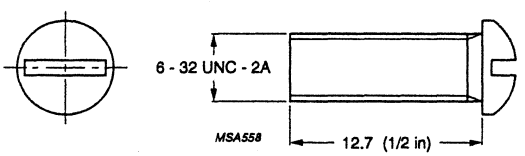
Fig.1 Distance disc 56245 for TO-5 or TO-39; insulating material.



Dimensions in mm.

Maximum permissible temperature: 100 °C.

Fig.2 Distance disc 56246 for TO-18 or TO-72; insulating material.

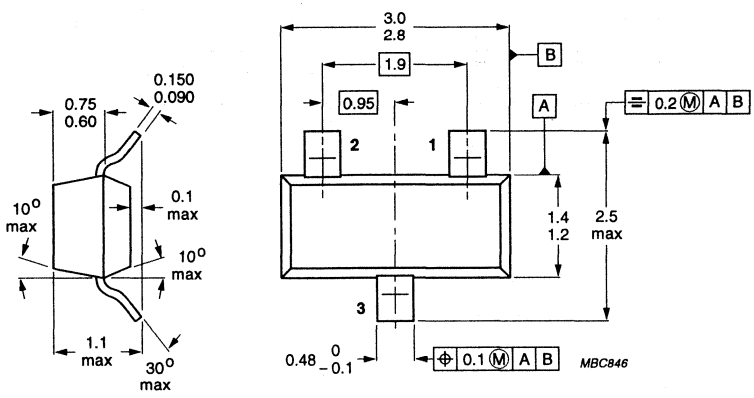


Dimensions in mm.

Available under type number 56396 or 12NC code number 9390 298 10xx0, upon request.

Fig.3 Round head screw 6-32 UNC-2A.

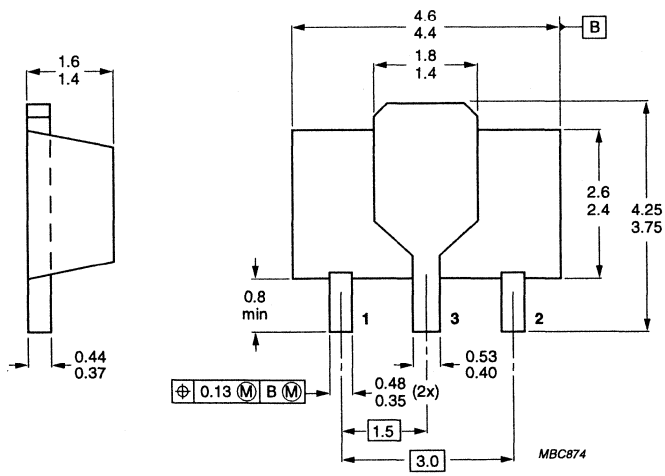
PACKAGE OUTLINES



TOP VIEW

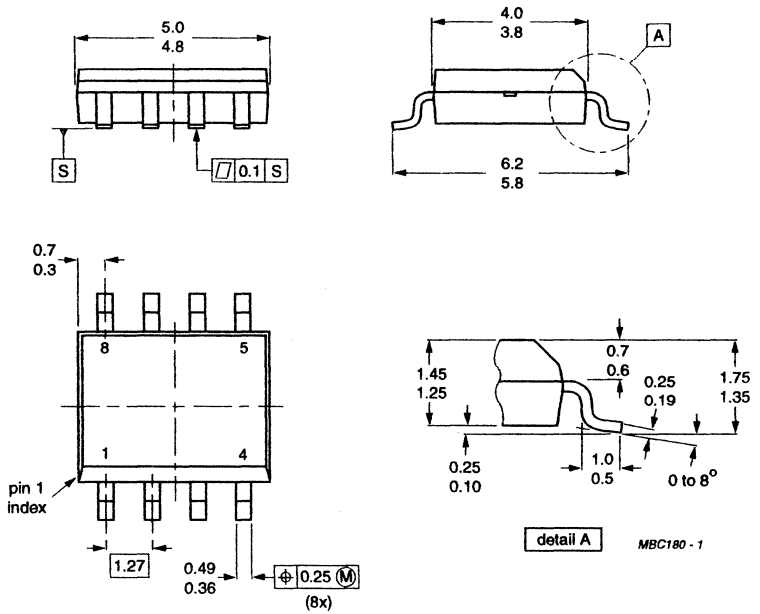
Dimensions in mm.

Fig.1 SOT23.



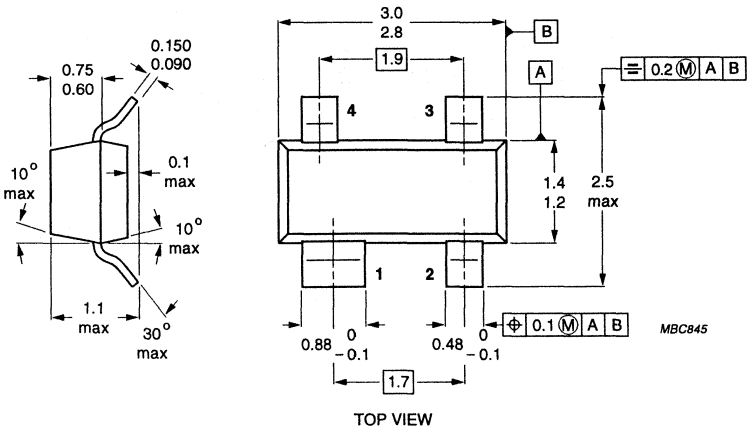
Dimensions in mm.

Fig.2 SOT89



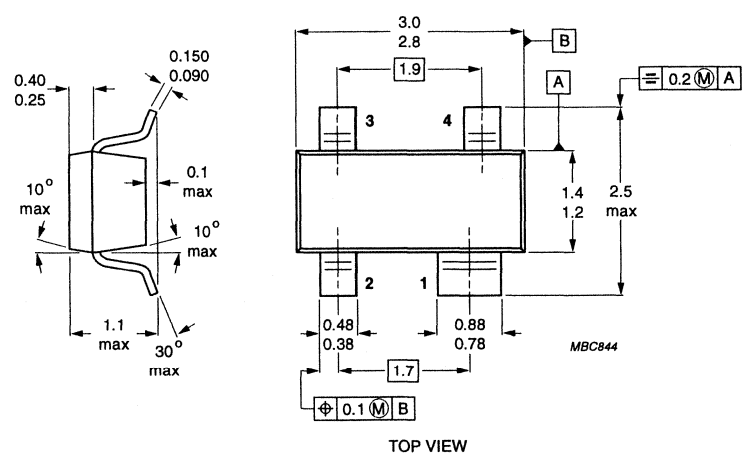
Dimensions in mm.

Fig.3 Plastic small outline package; 8 leads; body width 3.9 mm; SO8 (SOT96-1).



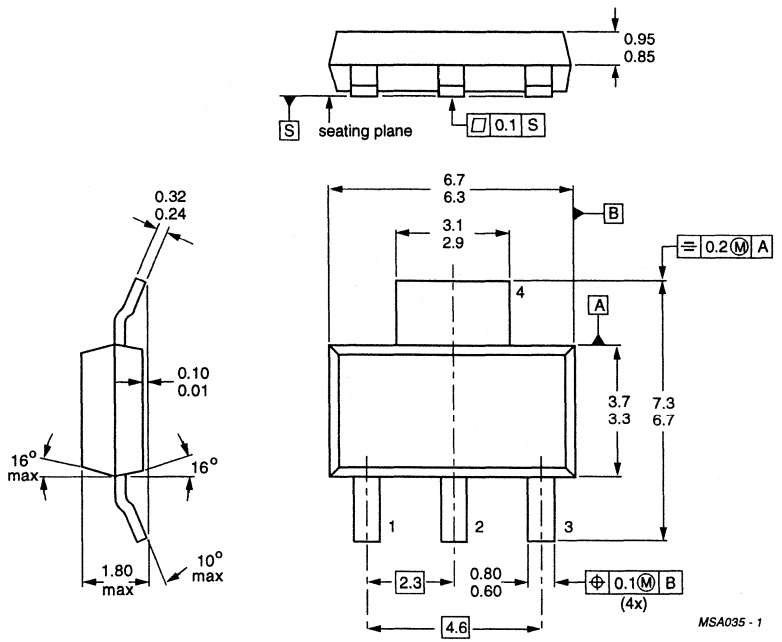
Dimensions in mm.

Fig.4 SOT143.



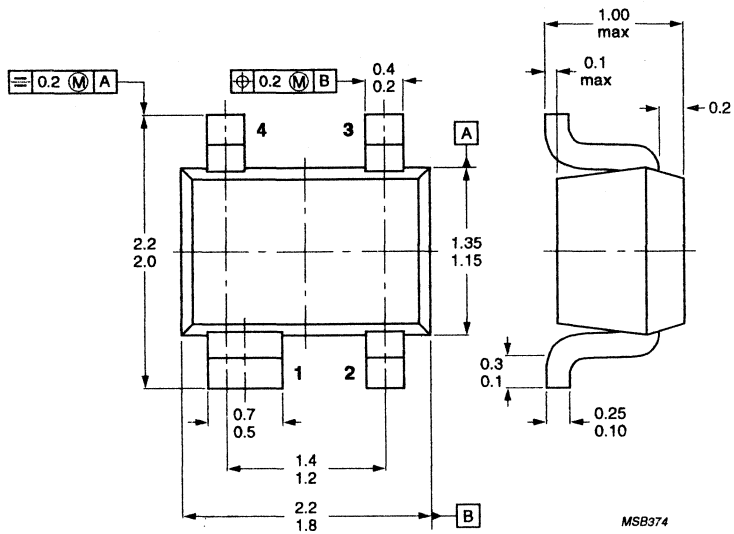
Dimensions in mm.

Fig.5 SOT143R.



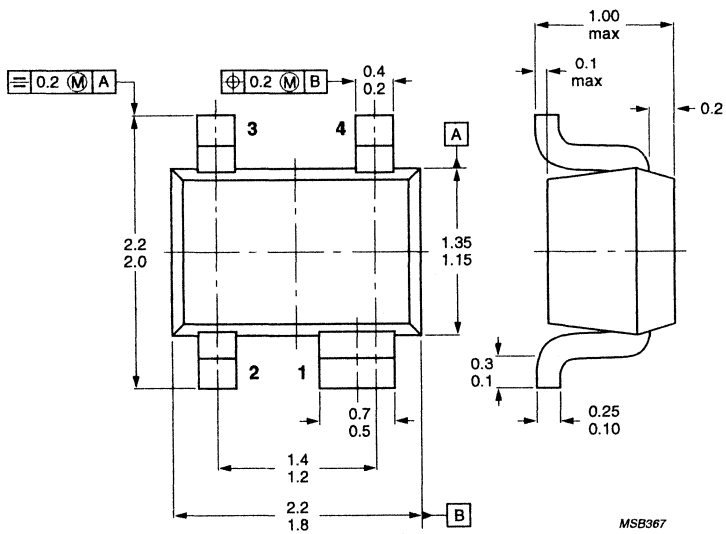
Dimensions in mm.

Fig.6 SOT223.



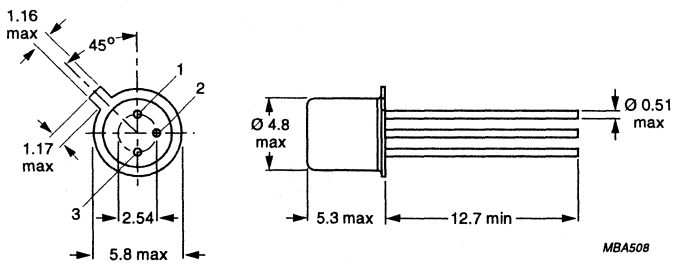
Dimensions in mm.

Fig.7 SOT343.



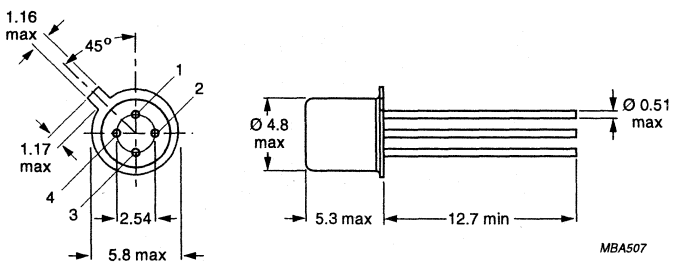
Dimensions in mm.

Fig.8 SOT343R.



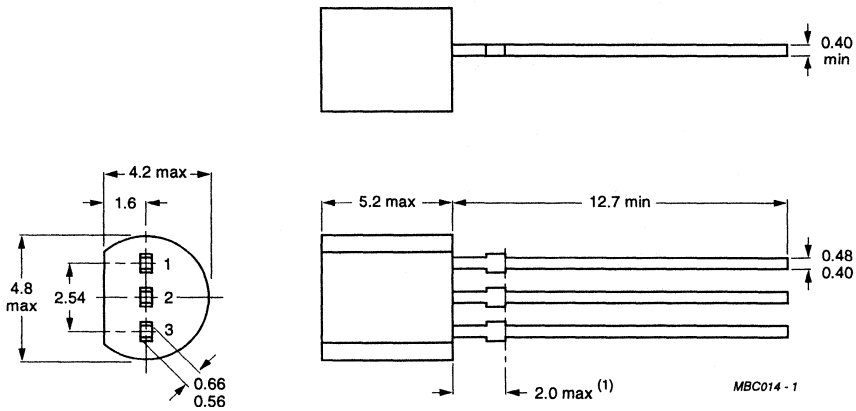
Dimensions in mm.

Fig.9 TO-18.



Dimensions in mm.

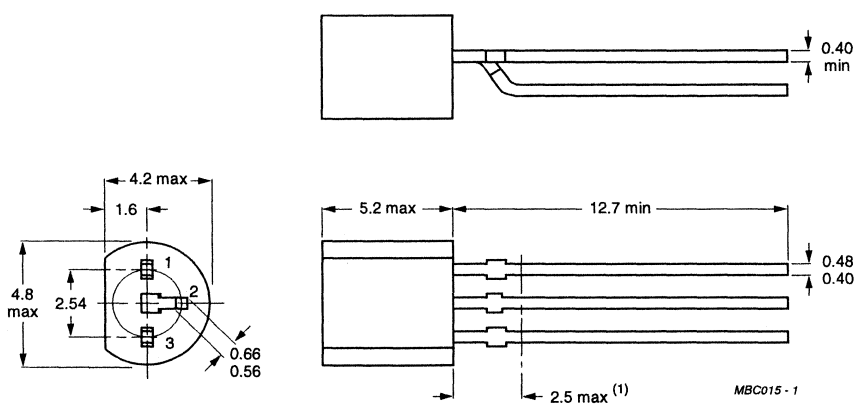
Fig.10 TO-72.



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

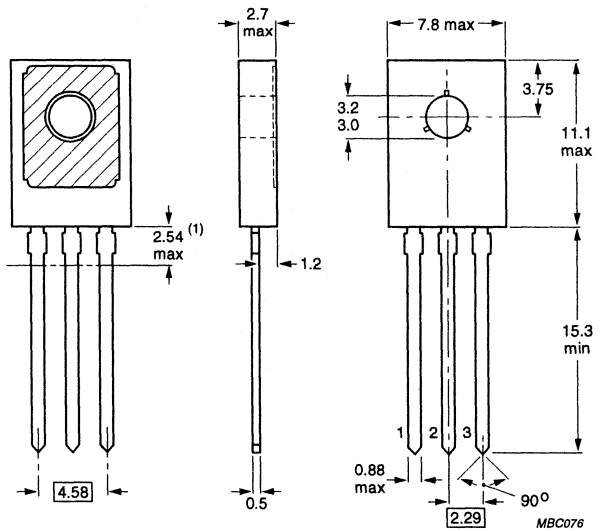
Fig.11 TO-92 in-line (SOT54).



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.12 TO-92 variant (SOT54).



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled.

Fig.13 TO-126 (SOT32).

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Data handbook system

DATA HANDBOOK SYSTEM

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